

MN103004J / 04K / F04K

Type	MN103004J / 04K / F04K	
Command ROM (×64-Bit)	192 KB / 128 KB / 256 KB (Flash)	
Data RAM (×32-Bit)	4 KB / 10 KB / 12 KB	
Minimum Instruction Execution Time	MN103004J / 04K: MN103004J / 04K: MN1030F04K:	30 ns (at 2.2 V, 33 MHz) 25 ns (at 3.0 V, 40 MHz) 36 ns (at 3.0 V, 28 MHz, 40 MHz (under development))
Interrupts	• RESET • IRQ × 8 • NMI × 1 • Timer × 22 • Input Capture × 14 • PWM × 4 • SIF × 16 • DMAC × 4 • WDT • A/D • System error	
Timer Counter	Timer Counter 0 to 3: 32-Bit × 1 (Interval Timer, Event Count, Toggle Output, Interrupt, A/D Conversion Trigger) Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source Underflow of Timer Counter 0, 1, 2, 3 Timer Counter 4 to 7: 32-Bit × 1 (Interval Timer, Event Count, Toggle Output, Interrupt, Clock Source for Serial I/F, Generation of Timer Synchronous Output Timing) Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source Underflow of Timer Counter 4, 5, 6, 7 Timer Counter 8 to B: 32-Bit × 1 (Interval Timer, Event Count, Toggle Output, Interrupt, Clock Source for Serial I/F, Generation of Timer Synchronous Output Timing) Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter Interrupt Source Underflow of Timer Counter 8, 9, A, B * Each of Timer Counters 0 to 3, 4 to 7, and 8 to B can be Changed to an 8-, 16-, or 24-Bit Timer Counter Timer Counter 10 to 13: 16-Bit × 4 (Interval Timer, Event Count, Toggle Output, Interrupt, DMA Start) Clock Source IOCLK, IOCLK/8, IOCLK/32, External Clock Input, Underflow of Timer Counter 0, 1, 2 Interrupt Source Underflow of Timer Counter 10, 11, 12, 13 Timer Counter 14, 15: 16-Bit × 2 (Interval Timer, Event Count, Toggle Output, PMW Output, Interrupt, Input Capture (2 Lines), One-Shot Output, External Trigger Start, Generation of Timer Synchronous Output Timing, DMA Start) Clock Source IOCLK, IOCLK/8, External Clock Input (2 Lines), Underflow of Timer Counter 0, 1, 2-Phase Encode Interrupt Source Overflow of Timer 14, 15, Underflow of Timer 14, 15, Coincidence of Compare Register with Binary Counter or at Capture Watchdog Timer: 16- to 25-Bit × 1ch	
DMA Controller	Number of Channels 2 Unit of Transfer 8/16/32 bits Max Transfer Cycles 65535 Starting Factor External Interrupt, Timer Factor, PNM Factor, Serial Transmission/Reception Factor, A/D Conversion finish, Software Factor Transfer Method 2-Bus Cycle Transfer Addressing Modes Fixed, Increment, Decrement Transfer Modes Word Transfer, Burst Transfer, Intermittent Transfer	
Serial Interface	Serial 0, 1: 7-, 8-Bit × 2 (Clock Synchronous Mode, Start-Stop Synchronous Mode, I²C Mode) Serial 2: 7-, 8-Bit × 1 (Start-Stop Synchronous Mode) Serial 3 to 7: 7-, 8-Bit × 5 (Clock Synchronous Mode) Clock Source (Clock Synchronous Mode, Start-Stop Synchronous Mode) IOCLK, Underflow of Timer Counter, External Clock (I²C Mode) IOCLK, Underflow of Timer Counter	

I/O Pins	I/O	155	• Common use 137
	Input	16	• Common use 16
A/D Inputs 10-Bit × 16ch			
PWM 12-, 14-Bit resolution × 4ch (dedicated), 16-Bit resolution × 2ch (Common with Timer)			
ICR 28-Bit × 13ch + 16-Bit × 4ch (Common with Timer)			
OCR 16-Bit × 4ch (Common with Timer)			
Timer Synchronous Output 4-Bit (Synchronous Output) × 2ch			
Package QFP208-P-2828A (MN103004J / 04K / F04K), FLGA239-C-1313 (MN103004K / F04K)			

Electrical Characteristics

MN103004J / 04K

Supply Current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating Supply Current	IDD1	VDDH, VDDB, VDD, PVDD, AVDD = 3.0 V VI = VDDH (VDDB) or VSS At internal = 40 MHz Output released			150	mA
Supply current at stopping	IDD4	VDD, PVDD, AVDD = 3.6 V VI = VDDH (VDDB) or VSS Fosc = Oscillation stopped Output released			150*	μA

*FLGA239-C-1313 (Ta = -20 °C to +85 °C)

A/D Conversion Performance

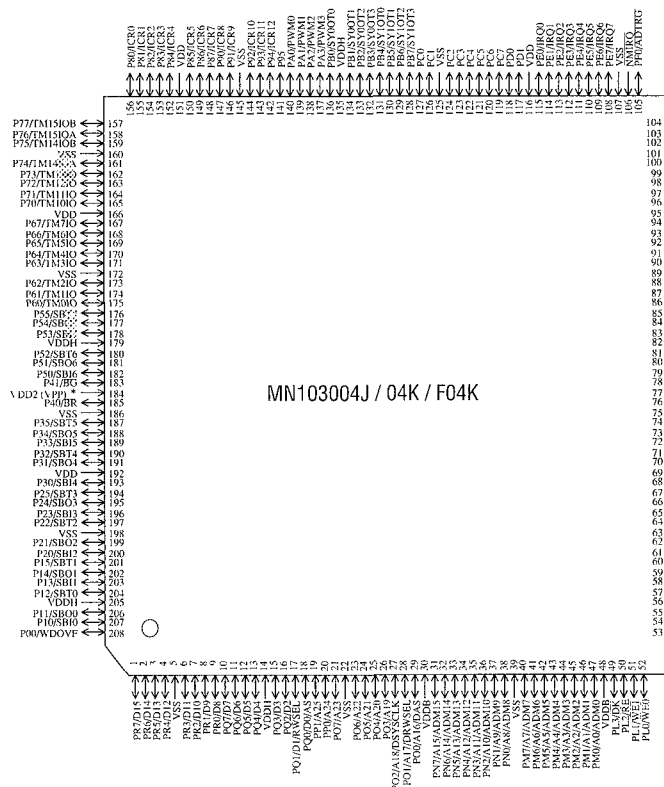
Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Resolution					10	Bits
A/D conversion absolute Error		VREF+ = 3.0 V A/D conversion clock = 5 MHz			±7	LSB
A/D conversion relative Error					±5	LSB
A/D conversion time			2.8			μs

(Ta = -20 °C to +85 °C, AVDD = 3.0 V, AVSS = 0.0 V)

Support Tool

In-Circuit Emulator	PX-ICE103004
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Pin Assignment

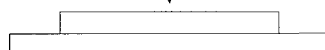


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QFP208-P-2828A

* VDD2 for MN103004K or MN103004J and VPP for MN1030E04K

Perspective

[illegible]

FLGA239-C-1313

B * H2 is VDD2 for MN103004K and VPP for MN1030F04K