

TMUX1204 5-V, 4:1, General Purpose Analog Multiplexer

1 Features

- Rail to rail operation
- Bidirectional signal path
- 1.8 V Logic compatible
- Fail-safe logic
- Low on-resistance: 5 Ω
- Wide supply range: 1.08 V to 5.5 V
- -40°C to +125°C Operating temperature
- Low supply current: 10 nA
- Transition time: 14 ns
- Break-before-make switching
- ESD protection HBM: 2000 V

2 Applications

- Analog and digital multiplexing or demultiplexing
- Motor drives
- Building automation
- Barcode scanner
- Analog input module
- Power delivery
- Smoke detectors
- Video surveillance
- Thermal imaging camera
- Electronic point of sale
- Appliances
- Consumer audio

3 Description

The TMUX1204 is a modern complementary metal-oxide semiconductor (CMOS) analog multiplexer (MUX) in a 4:1 single-ended (1-channel) configuration. The TMUX1204 works with a single supply (1.08 V to 5.5 V) which allows for use in a broad array of applications from personal electronics to building automation systems. A low supply current of 10 nA enables use in portable applications.

All logic inputs have 1.8 V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

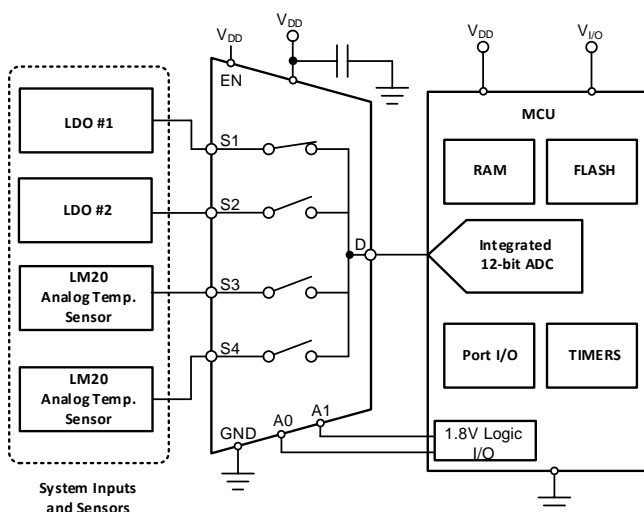
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX1204	VSSOP (10) (DGS)	3.00 mm x 3.00 mm
	USON (10) (DQA) ⁽²⁾	2.50 mm x 1.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

(2) Product preview

Application Example



TMUX1204 Block Diagram

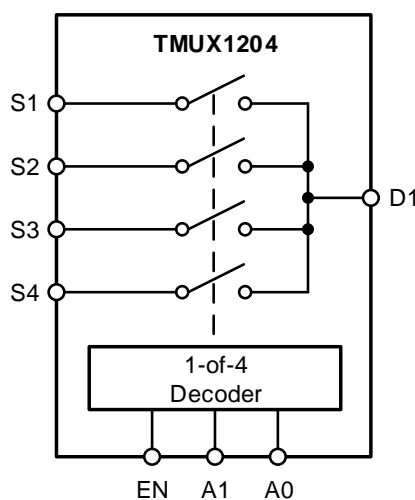


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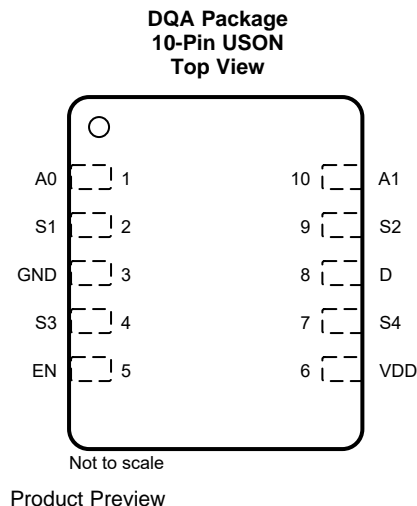
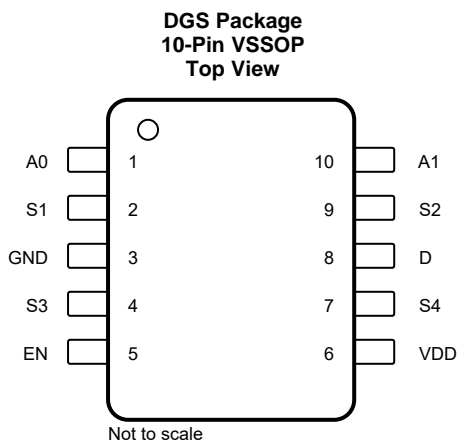
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2019	*	preliminary release.

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	DGS, DQA		
A0	1	I	Address line 0. Controls the switch configuration as shown in Table 1 .
S1	2	I/O	Source pin 1. Can be an input or output.
GND	3	P	Ground (0 V) reference
S3	4	I/O	Source pin 3. Can be an input or output.
EN	5	I	Active high logic enable. When this pin is low, all switches are turned off. When this pin is high, the A[1:0] logic inputs determine which switch is turned on.
VDD	6	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V_{DD} and GND.
S4	7	I/O	Source pin 4. Can be an input or output.
D	8	I/O	Drain pin. Can be an input or output.
S2	9	I/O	Source pin 2. Can be an input or output.
A1	10	I	Address line 1. Controls the switch configuration as shown in Table 1 .

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾ ⁽³⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	-0.5	6	V
V _{SEL} or V _{EN}	Logic control input pin voltage (EN, A0, A1)	-0.5	6	V
I _{SEL} or I _{EN}	Logic control input pin current (EN, A0, A1)	-30	30	mA
V _S or V _D	Source or drain voltage (Sx, D)	-0.5	V _{DD} +0.5	V
I _S or I _D (CONT)	Source or drain continuous current (Sx, D)	-30	30	mA
T _{stg}	Storage temperature	-65	150	°C
T _J	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{DD}	Positive power supply voltage	1.08		5.5	V
V _S or V _D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V _{DD}	V
V _{SEL} or V _{EN}	Logic control input pin voltage (EN, A0, A1)	0		5.5	V
T _A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX1204		UNIT
		DGS (VSSOP)	DQA (USON)	
		10 PINS	10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	193.9	173.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	83.1	99.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	116.5	73.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	22.0	8.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	114.6	73.0	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics ($V_{DD} = 5\text{ V} \pm 10\%$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C	5			Ω
			-40°C to +85°C			7	Ω
			-40°C to +125°C			9	Ω
ΔR_{ON}	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C	0.15			Ω
			-40°C to +85°C			1	Ω
			-40°C to +125°C			1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C	1.5			Ω
			-40°C to +85°C			2	Ω
			-40°C to +125°C			3	Ω
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	$V_{DD} = 5\text{ V}$ Switch Off $V_D = 4.5\text{ V} / 1.5\text{ V}$ $V_S = 1.5\text{ V} / 4.5\text{ V}$ Refer to Off-Leakage Current	25°C	± 75			nA
			-40°C to +85°C	-150		150	nA
			-40°C to +125°C	-175		175	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	$V_{DD} = 5\text{ V}$ Switch Off $V_D = 4.5\text{ V} / 1.5\text{ V}$ $V_S = 1.5\text{ V} / 4.5\text{ V}$ Refer to Off-Leakage Current	25°C	± 200			nA
			-40°C to +85°C	-500		500	nA
			-40°C to +125°C	-750		750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 5\text{ V}$ Switch On $V_D = V_S = 4.5\text{ V} / 1.5\text{ V}$ Refer to On-Leakage Current	25°C	± 200			nA
			-40°C to +85°C	-500		500	nA
			-40°C to +125°C	-750		750	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		-40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C	± 0.005			μA
I_{IH} I_{IL}	Input leakage current		-40°C to +125°C			± 0.10	μA
C_{IN}	Logic input capacitance		25°C	1			pF
C_{IN}	Logic input capacitance		-40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C	0.01			μA
			-40°C to +125°C			2	μA

(1) When V_S is 4.5 V, V_D is 1.5 V or when V_S is 1.5 V, V_D is 4.5 V.

Electrical Characteristics ($V_{DD} = 5\text{ V} \pm 10\%$) (continued)

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	$V_S = 3\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Transition Time	25°C	14			ns
			–40°C to +85°C			21	ns
			–40°C to +125°C			22	ns
t_{OPEN} (BBM)	Break before make time	$V_S = 3\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Break-Before-Make	25°C	8			ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{\text{ON(EN)}}$	Enable turn-on time	$V_S = 3\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	14			ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			20	ns
$t_{\text{OFF(EN)}}$	Enable turn-off time	$V_S = 3\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	5			ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			20	ns
Q_C	Charge Injection	$V_S = 1\text{ V}$ $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C		±9		pC
O_{ISO}	Off Isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Off Isolation	25°C		–62		dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Off Isolation	25°C		–42		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Crosstalk	25°C		–62		dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Crosstalk	25°C		–42		dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Bandwidth	25°C		125		MHz
C_{SOFF}	Source off capacitance	$f = 1\text{ MHz}$	25°C		13		pF
C_{DOFF}	Drain off capacitance	$f = 1\text{ MHz}$	25°C		38		pF
C_{SON} C_{DON}	On capacitance	$f = 1\text{ MHz}$	25°C		42		pF

6.6 Electrical Characteristics ($V_{DD} = 3.3\text{ V} \pm 10\%$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C		9		Ω
			-40°C to +85°C			15	Ω
			-40°C to +125°C			17	Ω
ΔR_{ON}	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C		0.15		Ω
			-40°C to +85°C			1	Ω
			-40°C to +125°C			1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C		3		Ω
			-40°C to +85°C			5	Ω
			-40°C to +125°C			6	Ω
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	$V_{DD} = 3.3\text{ V}$ Switch Off $V_D = 3\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 3\text{ V}$ Refer to Off-Leakage Current	25°C		± 75		nA
			-40°C to +85°C		-150	150	nA
			-40°C to +125°C		-175	175	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	$V_{DD} = 3.3\text{ V}$ Switch Off $V_D = 3\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 3\text{ V}$ Refer to Off-Leakage Current	25°C		± 200		nA
			-40°C to +85°C		-500	500	nA
			-40°C to +125°C		-750	750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 3.3\text{ V}$ Switch On $V_D = V_S = 3\text{ V} / 1\text{ V}$ Refer to On-Leakage Current	25°C		± 200		nA
			-40°C to +85°C		-500	500	nA
			-40°C to +125°C		-750	750	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		-40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		± 0.005		μA
I_{IH} I_{IL}	Input leakage current		-40°C to +125°C			± 0.10	μA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		-40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.01		μA
			-40°C to +125°C			1.3	μA

(1) When V_S is 3 V, V_D is 1 V or when V_S is 1 V, V_D is 3 V.

Electrical Characteristics ($V_{DD} = 3.3\text{ V} \pm 10\%$) (continued)

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	$V_S = 2\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Transition Time	25°C	14			ns
			–40°C to +85°C			25	ns
			–40°C to +125°C			25	ns
t_{OPEN} (BBM)	Break before make time	$V_S = 2\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Break-Before-Make	25°C	8			ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{\text{ON(EN)}}$	Enable turn-on time	$V_S = 2\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	14			ns
			–40°C to +85°C			25	ns
			–40°C to +125°C			25	ns
$t_{\text{OFF(EN)}}$	Enable turn-off time	$V_S = 2\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	7			ns
			–40°C to +85°C			13	ns
			–40°C to +125°C			13	ns
Q_C	Charge Injection	$V_S = 1\text{ V}$ $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C		± 7		pC
O_{ISO}	Off Isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Off Isolation	25°C		–62		dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Off Isolation	25°C		–42		dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Crosstalk	25°C		–62		dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Crosstalk	25°C		–42		dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Bandwidth	25°C		125		MHz
C_{SOFF}	Source off capacitance	$f = 1\text{ MHz}$	25°C		13		pF
C_{DOFF}	Drain off capacitance	$f = 1\text{ MHz}$	25°C		38		pF
C_{SON} C_{DON}	On capacitance	$f = 1\text{ MHz}$	25°C		42		pF

6.7 Electrical Characteristics ($V_{DD} = 1.8\text{ V} \pm 10\%$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C		40		Ω
			-40°C to +85°C			80	Ω
			-40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C		0.15		Ω
			-40°C to +85°C			1.5	Ω
			-40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	$V_{DD} = 1.98\text{ V}$ Switch Off $V_D = 1.8\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 1.8\text{ V}$ Refer to Off-Leakage Current	25°C		± 75		nA
			-40°C to +85°C		-150	150	nA
			-40°C to +125°C		-175	175	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	$V_{DD} = 1.98\text{ V}$ Switch Off $V_D = 1.8\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 1.8\text{ V}$ Refer to Off-Leakage Current	25°C		± 200		nA
			-40°C to +85°C		-500	500	nA
			-40°C to +125°C		-750	750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 1.98\text{ V}$ Switch On $V_D = V_S = 1.8\text{ V} / 1\text{ V}$ Refer to On-Leakage Current	25°C		± 200		nA
			-40°C to +85°C		-500	500	nA
			-40°C to +125°C		-750	750	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		-40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		± 0.005		μA
			-40°C to +125°C			± 0.10	μA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		-40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C		0.005		μA
			-40°C to +125°C			0.95	μA

(1) When V_S is 1.8 V, V_D is 1 V or when V_S is 1 V, V_D is 1.8 V.

Electrical Characteristics ($V_{DD} = 1.8\text{ V} \pm 10\%$) (continued)

 at $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Transition Time	25°C	28			ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
t_{OPEN} (BBM)	Break before make time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Break-Before-Make	25°C	16			ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{\text{ON(EN)}}$	Enable turn-on time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	28			ns
			–40°C to +85°C			48	ns
			–40°C to +125°C			48	ns
$t_{\text{OFF(EN)}}$	Enable turn-off time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	16			ns
			–40°C to +85°C			27	ns
			–40°C to +125°C			27	ns
Q_C	Charge Injection	$V_S = 1\text{ V}$ $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C	–2			pC
O_{ISO}	Off Isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Off Isolation	25°C	–62			dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Off Isolation	25°C	–42			dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Crosstalk	25°C	–62			dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Crosstalk	25°C	–42			dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Bandwidth	25°C	125			MHz
C_{SOFF}	Source off capacitance	$f = 1\text{ MHz}$	25°C	13			pF
C_{DOFF}	Drain off capacitance	$f = 1\text{ MHz}$	25°C	38			pF
C_{SON} C_{DON}	On capacitance	$f = 1\text{ MHz}$	25°C	42			pF

6.8 Electrical Characteristics ($V_{DD} = 1.2\text{ V} \pm 10\%$)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C	70			Ω
			-40°C to +85°C			105	Ω
			-40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to On-Resistance	25°C	0.15			Ω
			-40°C to +85°C			1.5	Ω
			-40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾	$V_{DD} = 1.32\text{ V}$ Switch Off $V_D = 1.2\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 1.2\text{ V}$ Refer to Off-Leakage Current	25°C	± 75			nA
			-40°C to +85°C	-150		150	nA
			-40°C to +125°C	-175		175	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾	$V_{DD} = 1.32\text{ V}$ Switch Off $V_D = 1.2\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 1.2\text{ V}$ Refer to Off-Leakage Current	25°C	± 200			nA
			-40°C to +85°C	-500		500	nA
			-40°C to +125°C	-750		750	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 1.32\text{ V}$ Switch On $V_D = V_S = 1.2\text{ V} / 1\text{ V}$ Refer to On-Leakage Current	25°C	± 200			nA
			-40°C to +85°C	-500		500	nA
			-40°C to +125°C	-750		750	nA
LOGIC INPUTS (EN, A0, A1)							
V_{IH}	Input logic high		-40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		-40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C	± 0.005			μA
			-40°C to +125°C			± 0.10	μA
C_{IN}	Logic input capacitance		25°C	1			pF
C_{IN}	Logic input capacitance		-40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V or 5.5 V	25°C	0.005			μA
			-40°C to +125°C			0.8	μA

(1) When V_S is 1 V, V_D is 1.2 V or when V_S is 1.2 V, V_D is 1 V.

Electrical Characteristics ($V_{DD} = 1.2\text{ V} \pm 10\%$) (continued)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Transition Time	25°C	60			ns
			–40°C to +85°C		210		ns
			–40°C to +125°C		210		ns
t_{OPEN} (BBM)	Break before make time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to Break-Before-Make	25°C	28			ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$t_{\text{ON(EN)}}$	Enable turn-on time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	60			ns
			–40°C to +85°C		190		ns
			–40°C to +125°C		190		ns
$t_{\text{OFF(EN)}}$	Enable turn-off time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$, $C_L = 15\text{ pF}$ Refer to $t_{\text{ON(EN)}}$ and $t_{\text{OFF(EN)}}$	25°C	45			ns
			–40°C to +85°C		150		ns
			–40°C to +125°C		150		ns
Q_C	Charge Injection	$V_S = 1\text{ V}$ $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ Refer to Charge Injection	25°C	± 2			pC
O_{ISO}	Off Isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Off Isolation	25°C	–62			dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Off Isolation	25°C	–42			dB
X_{TALK}	Crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to Crosstalk	25°C	–62			dB
		$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to Crosstalk	25°C	–42			dB
BW	Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ Refer to Bandwidth	25°C	125			MHz
C_{SOFF}	Source off capacitance	$f = 1\text{ MHz}$	25°C	13			pF
C_{DOFF}	Drain off capacitance	$f = 1\text{ MHz}$	25°C	38			pF
C_{SON} C_{DON}	On capacitance	$f = 1\text{ MHz}$	25°C	42			pF

6.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

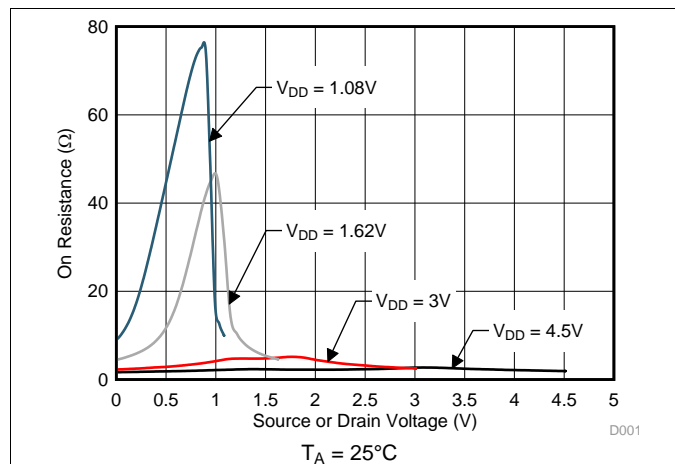


Figure 1. On-Resistance vs Source or Drain Voltage

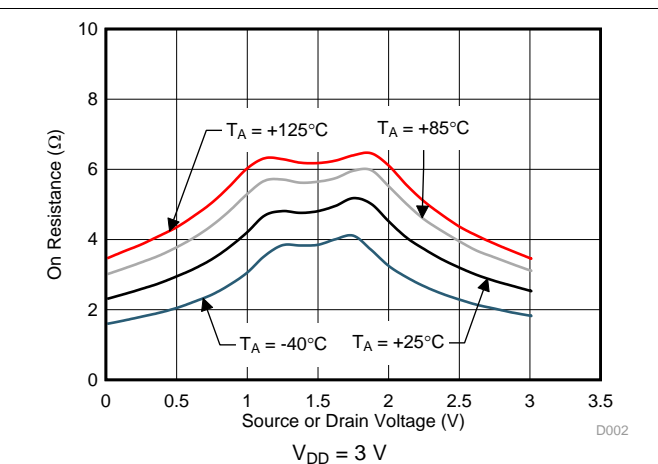


Figure 2. On-Resistance vs Source or Drain Voltage

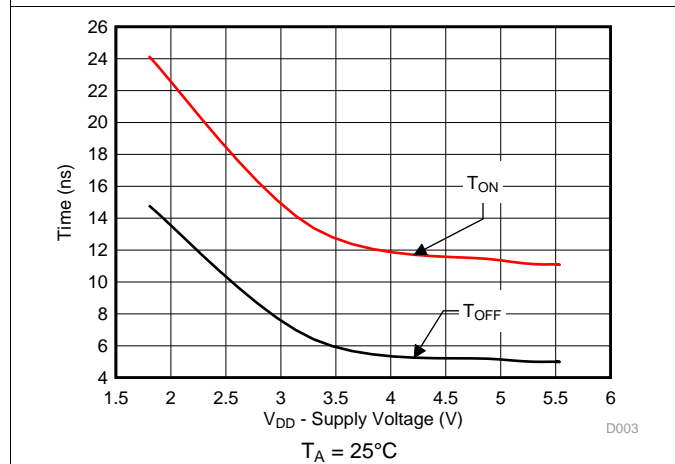


Figure 3. T_{ON} (EN) and T_{OFF} (EN) vs Supply Voltage

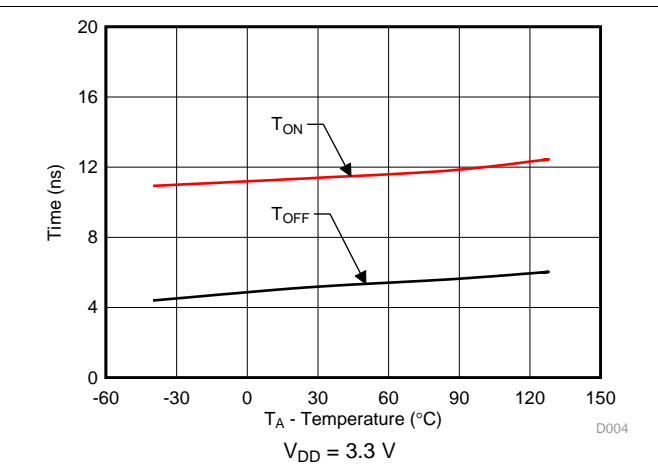


Figure 4. T_{ON} (EN) and T_{OFF} (EN) vs Temperature

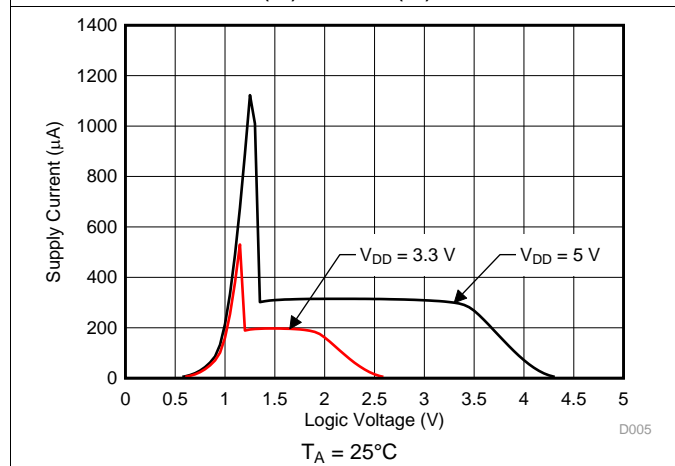


Figure 5. Supply Current vs Logic Voltage

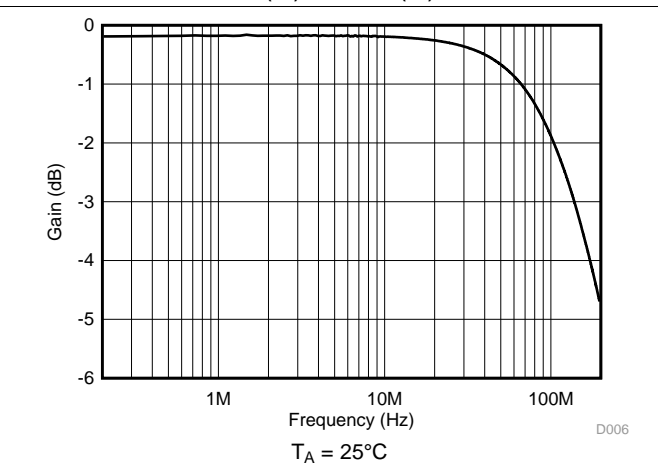


Figure 6. Frequency Response

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 7. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

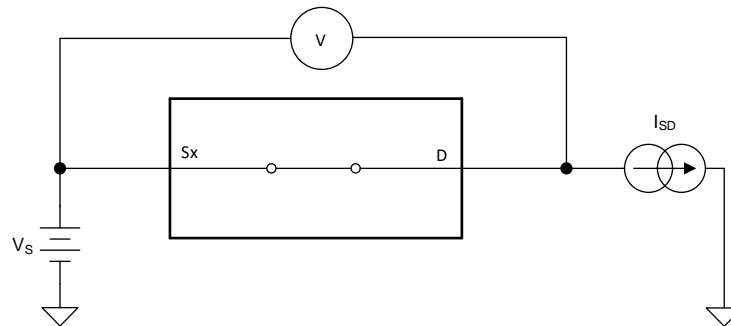


Figure 7. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 8.

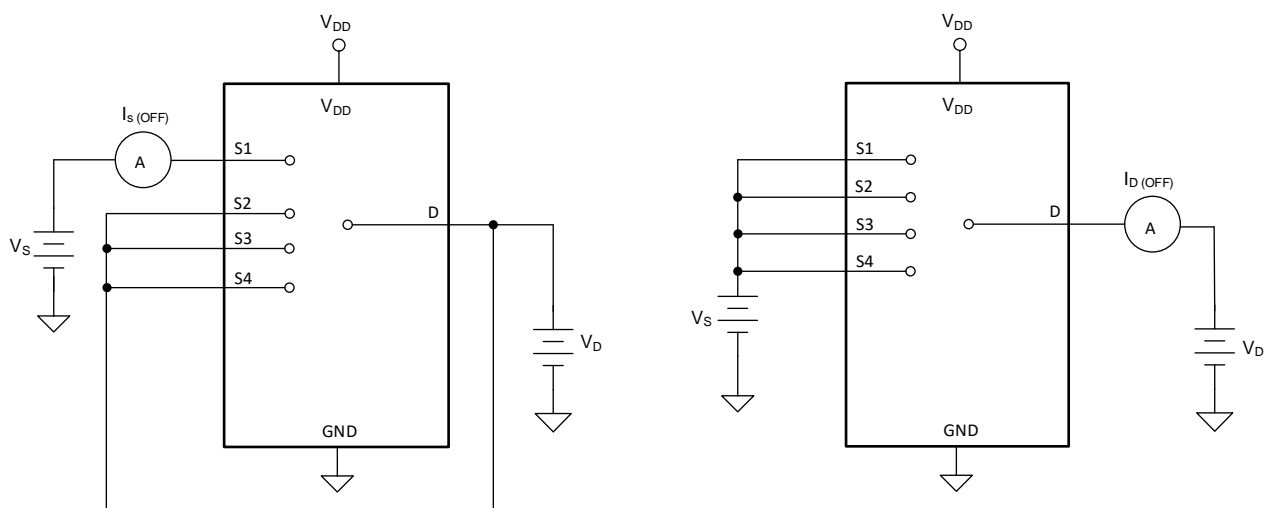


Figure 8. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 9 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

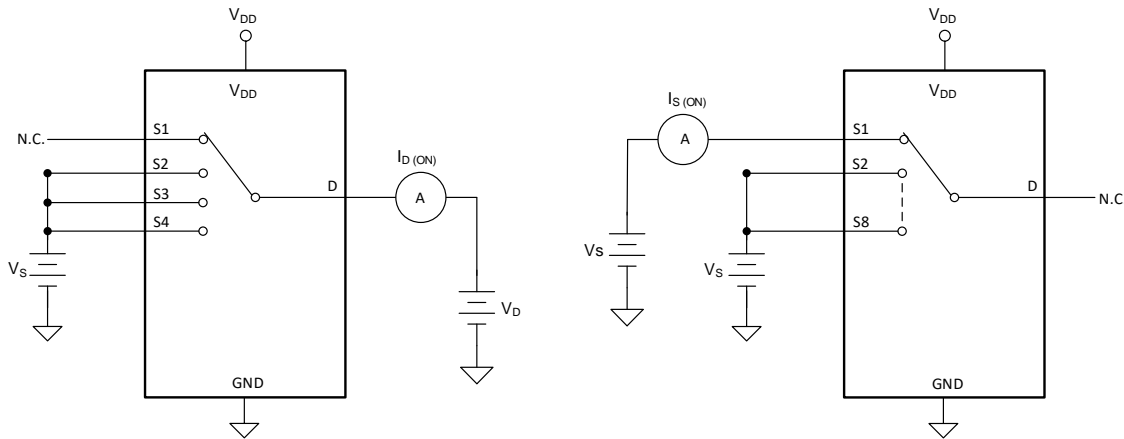


Figure 9. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the address signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 10 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

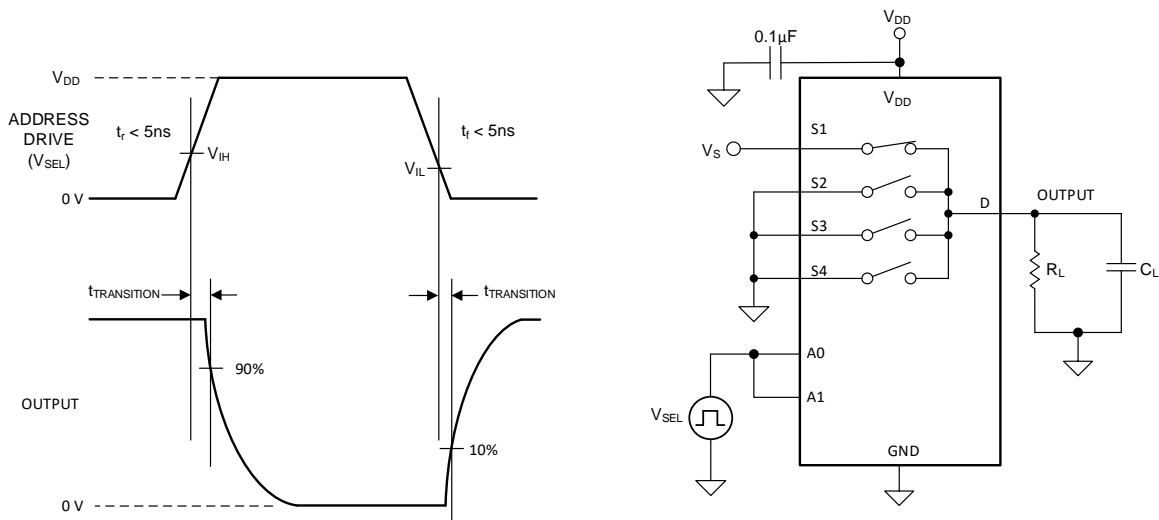


Figure 10. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 11 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

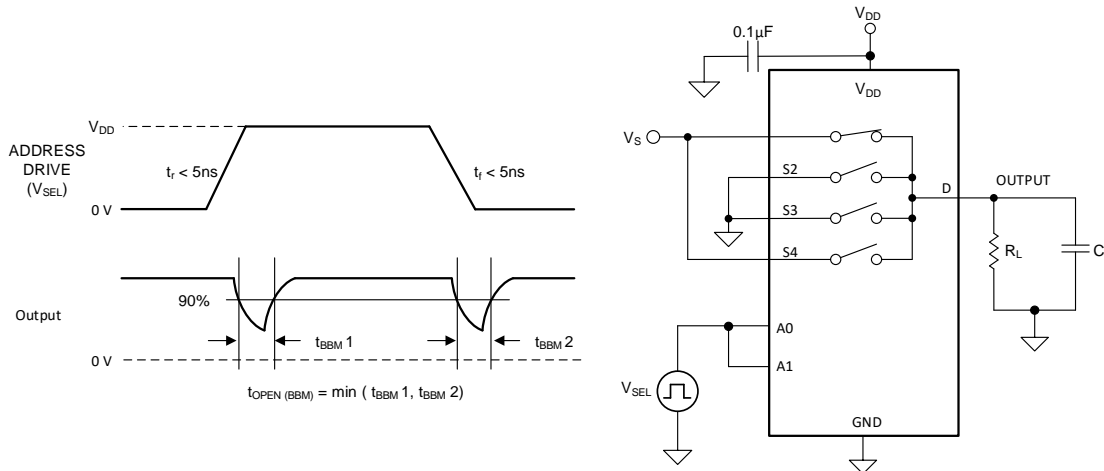


Figure 11. Break-Before-Make Delay Measurement Setup

7.6 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 10% after the enable has risen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 12 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 12 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

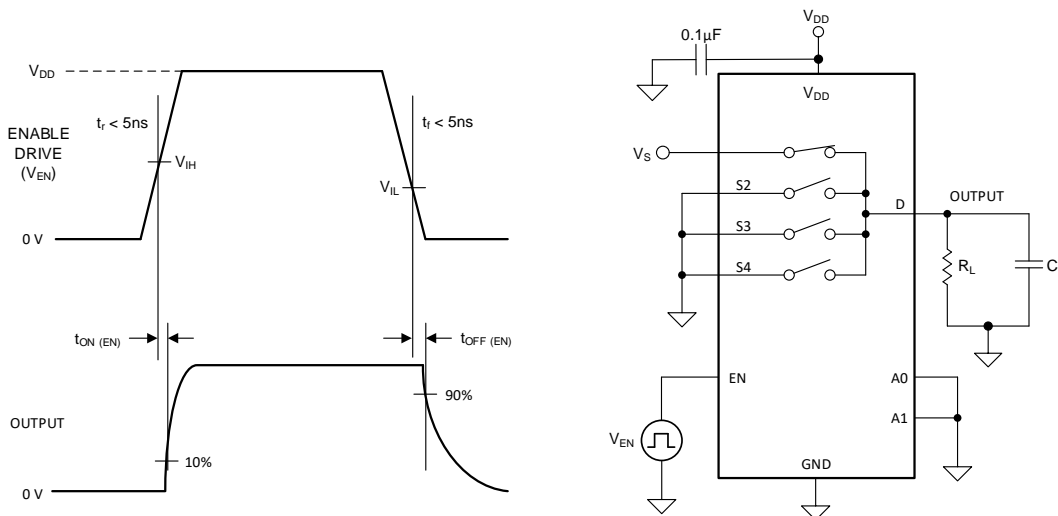


Figure 12. Turn-On and Turn-Off Time Measurement Setup

7.7 Charge Injection

The TMUX1204 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C . Figure 13 shows the setup used to measure charge injection from source (S_x) to drain (D).

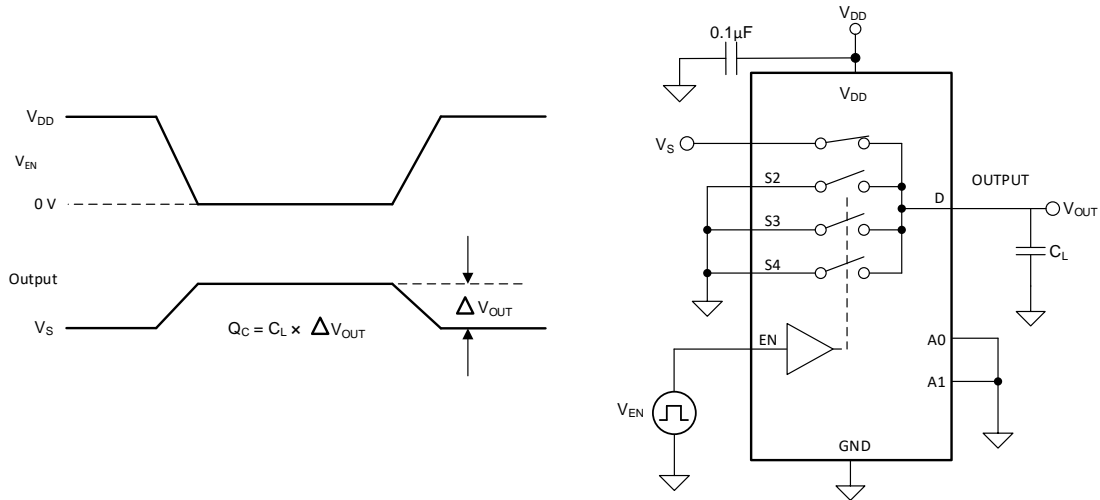


Figure 13. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (S_x) of an off-channel. Figure 14 shows the setup used to measure, and the equation used to calculate off isolation.

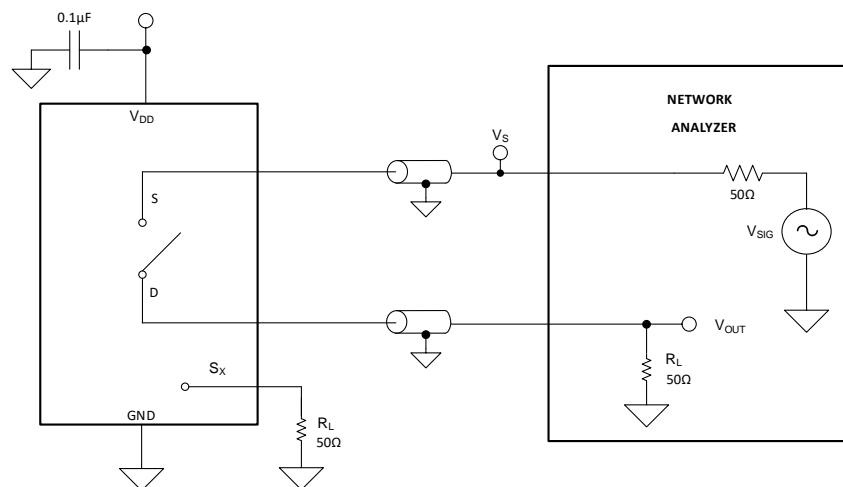


Figure 14. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{OUT}}{V_S} \right)$$

(1)

7.9 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. [Figure 15](#) shows the setup used to measure, and the equation used to calculate crosstalk.

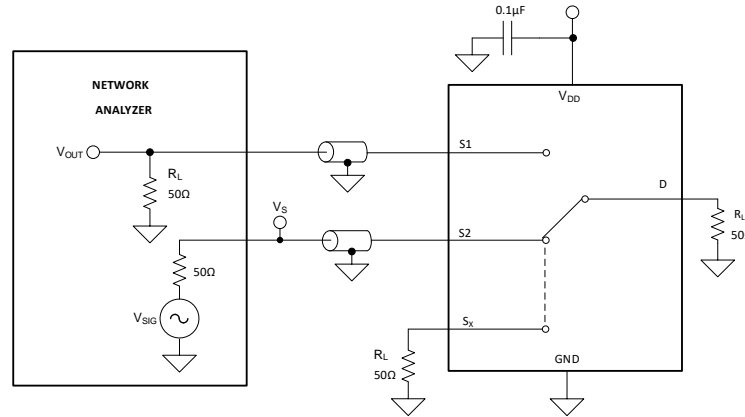


Figure 15. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_{\text{S}}} \right) \tag{2}$$

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. [Figure 16](#) shows the setup used to measure bandwidth.

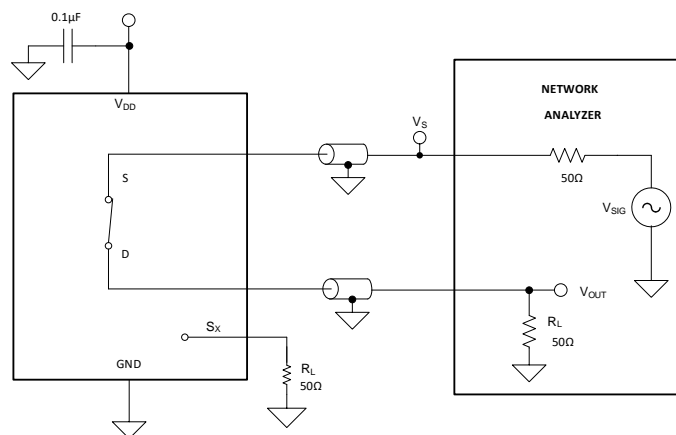


Figure 16. Bandwidth Measurement Setup

8 Detailed Description

8.1 Functional Block Diagram

The TMUX1204 is a 4:1, single-ended (1-ch.), mux. Each channel is turned on or turned off based on the state of the address lines and the enable pin.

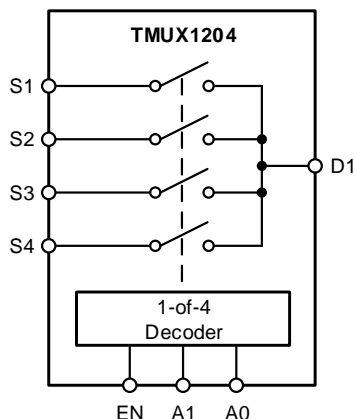


Figure 17. TMUX1204 Functional Block Diagrams

8.2 Feature Description

8.2.1 Bidirectional Operation

The TMUX1204 conducts equally well from source (S_x) to drain (D) or from drain (D) to source (S_x). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.2.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1204 ranges from GND to V_{DD} .

8.2.3 1.8 V Logic Compatible Inputs

The TMUX1204 has 1.8-V logic compatible control for all logic control inputs. The logic input thresholds scale with supply but still provide 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allows the TMUX1204 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#)

8.2.4 Fail-Safe Logic

The TMUX1204 supports Fail-Safe Logic on the control input pins (EN, A0, A1) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1204 to be ramped to 5.5 V while $V_{DD} = 0$ V. Additionally, the feature enables operation of the TMUX1204 with $V_{DD} = 1.2$ V while allowing the select pins to interface with a logic level of another device up to 5.5 V.

8.3 Device Functional Modes

When the EN pin of the TMUX1204 is pulled high, one of the switches is closed based on the state of the address lines. When the EN pin is pulled low, all the switches are in an open state irrespective of the state of the address lines. The EN pin can be connected to V_{DD} (as high as 5.5 V).

8.4 Truth Tables

and [Table 1](#) show the truth tables for the TMUX1204, respectively.

Table 1. TMUX1204 Truth Table

EN	A1	A0	Selected Channel Connected To Drain (D) Pin
0	X ⁽¹⁾	X ⁽¹⁾	All channels are off
1	0	0	Channel S1
1	0	1	Channel S2
1	1	0	Channel S3
1	1	1	Channel S4

(1) X denotes *don't care*.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX12xx family offers good system performance across a wide operating supply (1.08V to 5.5V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/O rails. Additionally, the control input pins support Fail-Safe Logic which allows for operation up to 5.5V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features make the TMUX12xx a family of general purpose multiplexers and switches that can reduce system complexity, board size, and overall system cost.

9.2 Typical Application

One useful application to take advantage of the TMUX1204 features is multiplexing various signals into an ADC that is integrated into a MCU. Utilizing an integrated ADC in a MCU allows a system to minimize cost with a potential tradeoff of system performance when compared to an external ADC. The multiplexer allows for multiple inputs/sensors to be monitored with a single ADC pin of the device, which is critical in systems with limited I/O.

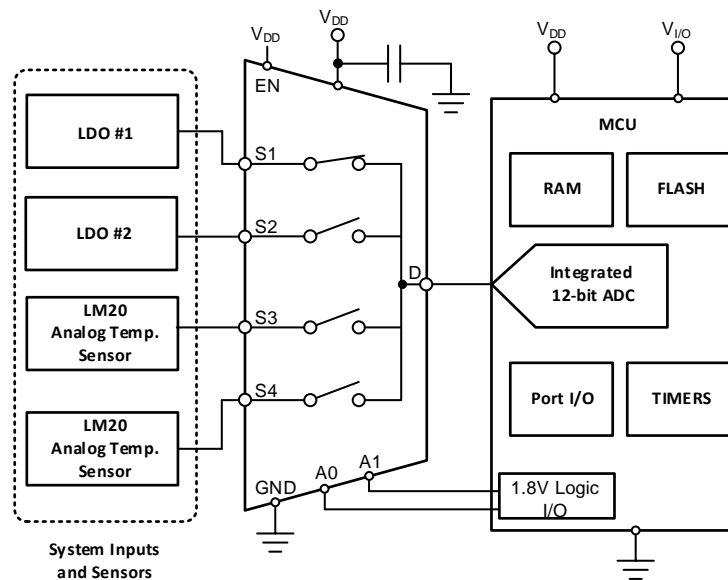


Figure 18. Multiplexing Signals to Integrated ADC

9.3 Design Requirements

For this design example, use the parameters listed in [Table 2](#).

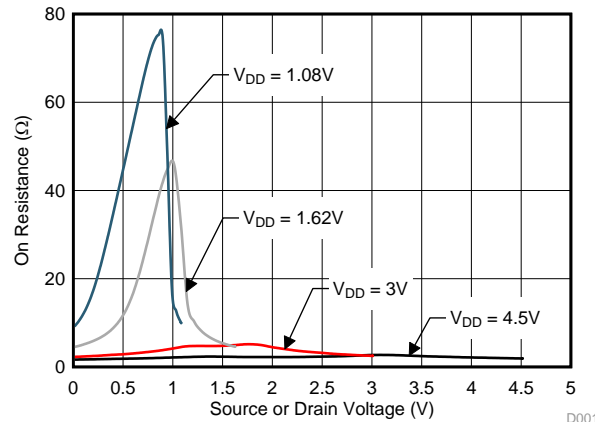
Table 2. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5.0 V
I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible

9.4 Detailed Design Procedure

The TMUX1204 can be operated without any external components except for the supply decoupling capacitors. If the parts desired power-up state is disabled, the enable pin should have a weak pull-down resistor and be controlled by the MCU via GPIO. All inputs being muxed to the ADC of the MCU must fall within the recommend operating conditions of the TMUX1204 including signal range and continuous current. For this design with a supply of 5 V the signal range can be 0 V to 5 V and the max continuous current can be 30 mA.

9.5 Application Curve



$T_A = 25^\circ\text{C}$

Figure 19. On-Resistance vs Source or Drain Voltage

10 Power Supply Recommendations

The TMUX1204 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 20 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

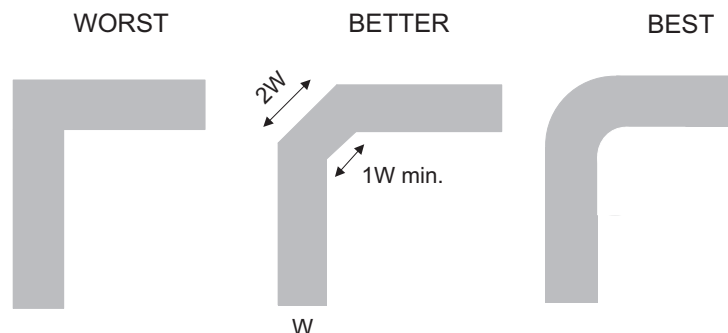


Figure 20. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 21 illustrates an example of a PCB layout with the TMUX1204. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1- μF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

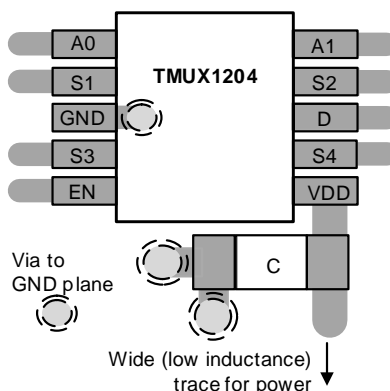


Figure 21. TMUX1204 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Texas Instruments, [Simplifying Design with 1.8 V logic Muxes and Switches](#).

Texas Instruments, [QFN/SON PCB Attachment](#).

Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#).

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1204DGSR	PREVIEW	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1F6	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

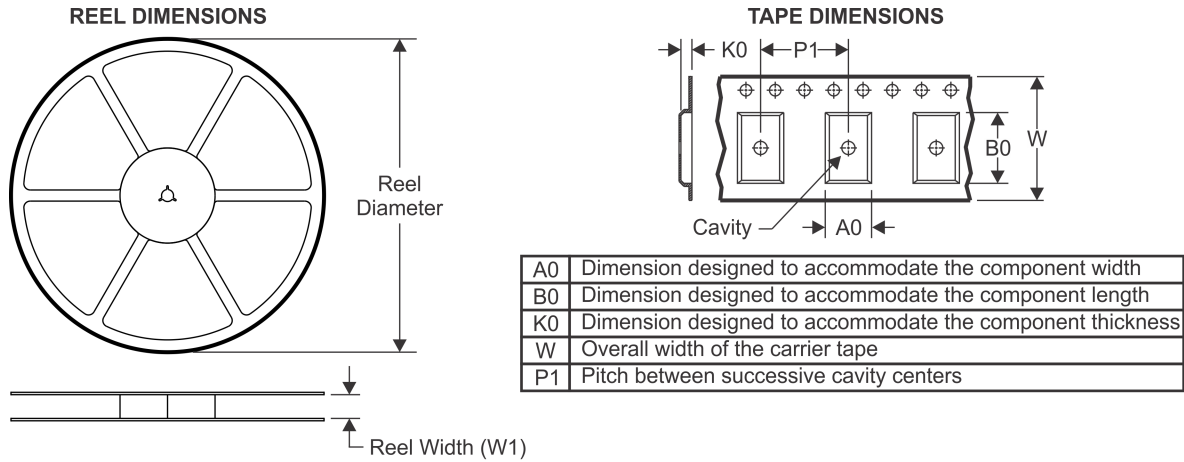
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1204DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1204DGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

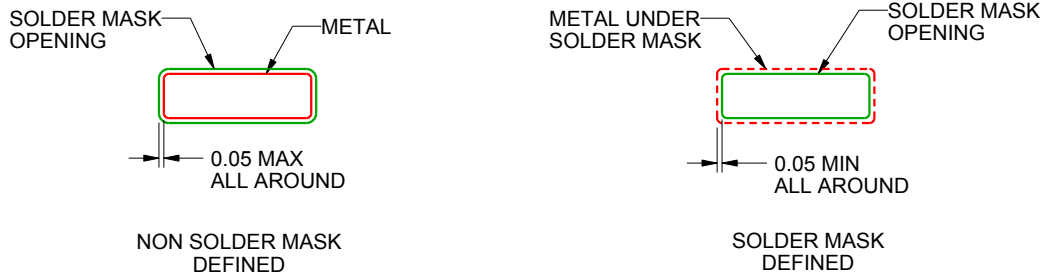
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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