DATA SHEET

74LVC1G19
1-of-2 decoder/demultiplexer

Product specification
Supersedes data of 2003 Sep 01

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Philips
Semiconductors

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1-of-2 decoder/demultiplexer 74LVC1G19

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC1G19 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Input can be driven from either 3.3 V or 5 V devices. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G19 is a 1-of-2 decoder/demultiplexer with a common output enable. The 74LVC1G19 buffers the data on input pin E and passes it either to output pin 1Y or 2Y, depending on whether the state of the select input pin A is LOW or HIGH, respectively.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay input A to output nY	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	4.0	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.5	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	2.8	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.5	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω	1.8	ns
C_I	input capacitance		2.5	pF
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; notes 1 and 2	18.9	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = number of inputs switching;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT	
E	**A**	**1Y**	**2Y**
L	L	L	H
L	H	H	L
H	L	H	H
H	H	H	H

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	**PINS**	**PACKAGE**	**MATERIAL**	**CODE**	**MARKING**
74LVC1G19GW	–40 °C to +125 °C	6	SC-88	plastic	SOT363	VY
74LVC1G19GV	–40 °C to +125 °C	6	SC-74	plastic	SOT457	V19
74LVC1G19GM	–40 °C to +125 °C	6	XSON6	plastic	SOT886	VY

PINNING

PIN	SYMBOL	DESCRIPTION
1	A	data input
2	GND	ground (0 V)
3	E	data input
4	2Y	data output
5	V_{CC}	supply voltage
6	1Y	data output

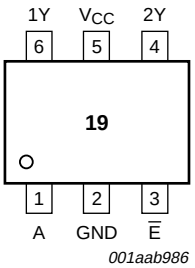
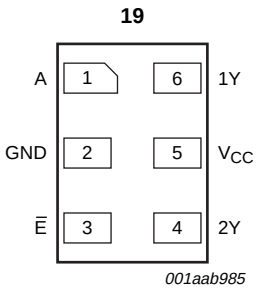


Fig.1 Pin configuration SC-88 and SC-74.



Transparent top view

Fig.2 Pin configuration XSON6.

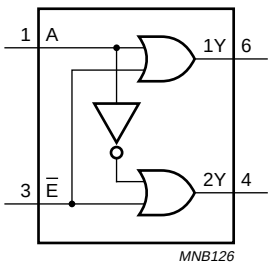


Fig.3 Logic symbol.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	–	±50	mA
V_O	output voltage	active mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		Power-down mode; notes 1 and 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	0.07	0.45	V
		I_O = 8 mA	2.3	–	0.12	0.3	V
		I_O = 12 mA	2.7	–	0.17	0.4	V
		I_O = 24 mA	3.0	–	0.33	0.55	V
		I_O = 32 mA	4.5	–	0.39	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 μA	1.65 to 5.5	V_{CC} – 0.1	–	–	V
		I_O = –4 mA	1.65	1.2	1.54	–	V
		I_O = –8 mA	2.3	1.9	2.15	–	V
		I_O = –12 mA	2.7	2.2	2.50	–	V
		I_O = –24 mA	3.0	2.3	2.62	–	V
		I_O = –32 mA	4.5	3.8	4.11	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	±0.1	±5	μA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V	0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A	2.3 to 5.5	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.70	V
		I_O = 8 mA	2.3	–	–	0.45	V
		I_O = 12 mA	2.7	–	–	0.60	V
		I_O = 24 mA	3.0	–	–	0.80	V
		I_O = 32 mA	4.5	–	–	0.80	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 μA	1.65 to 5.5	V_{CC} – 0.1	–	–	V
		I_O = –4 mA	1.65	0.95	–	–	V
		I_O = –8 mA	2.3	1.7	–	–	V
		I_O = –12 mA	2.7	1.9	–	–	V
		I_O = –24 mA	3.0	2.0	–	–	V
		I_O = –32 mA	4.5	3.4	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	–	±20	μA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V	0	–	–	±20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A	2.3 to 5.5	–	–	5000	μA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

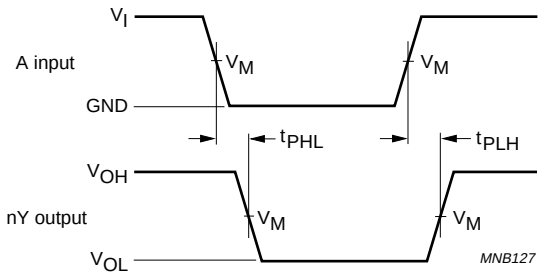
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay input A to output nY	see Figs 4 and 5	1.65 to 1.95	1.0	4.0	10.5	ns
			2.3 to 2.7	0.5	2.5	6.2	ns
			2.7	1.0	2.8	6.5	ns
			3.0 to 3.6	0.5	2.5	5.2	ns
			4.5 to 5.5	0.5	1.8	3.9	ns
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay input A to output nY	see Figs 4 and 5	1.65 to 1.95	1.0	–	13.1	ns
			2.3 to 2.7	0.5	–	7.7	ns
			2.7	0.5	–	8.1	ns
			3.0 to 3.6	0.5	–	6.0	ns
			4.5 to 5.5	0.5	–	5.0	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

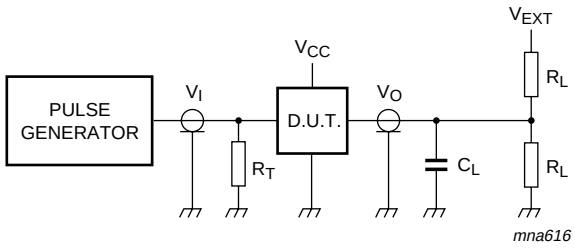
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.4 The input A to output nY propagation delays.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Definitions for test circuit:

R_L = Load resistor.

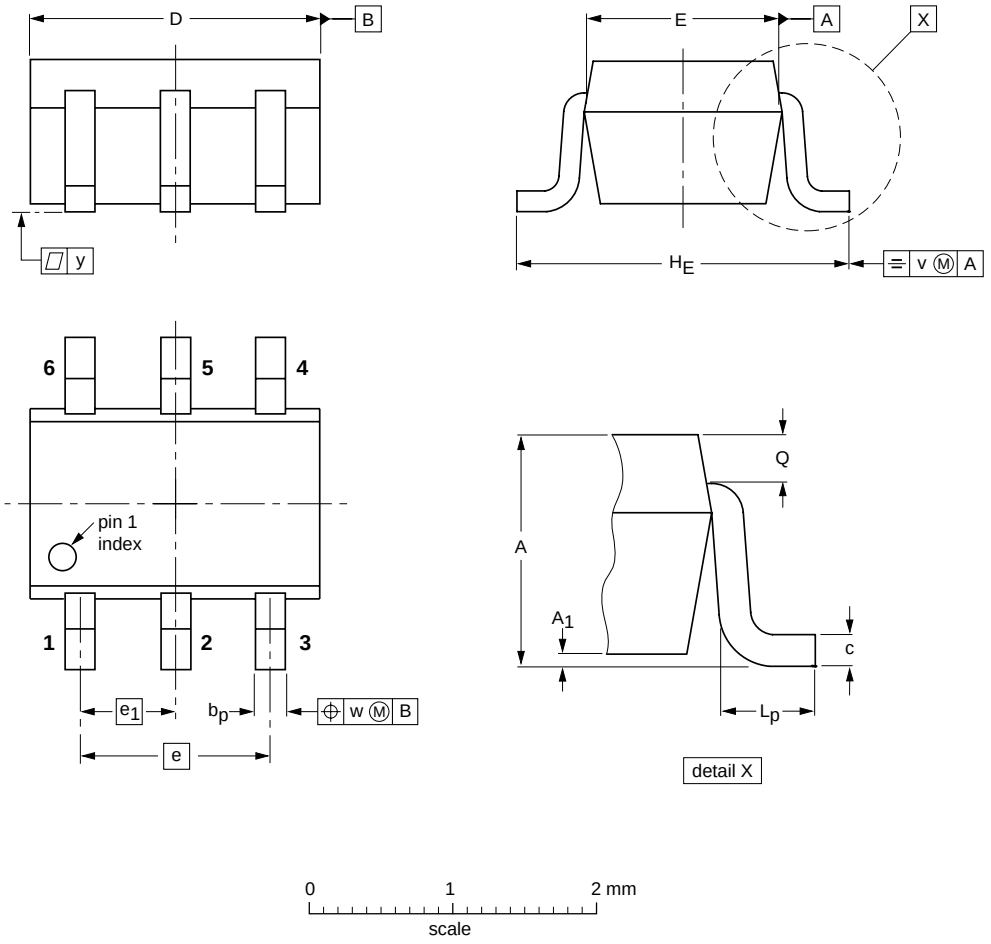
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.5 Load circuitry for switching times.

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads **SOT363**

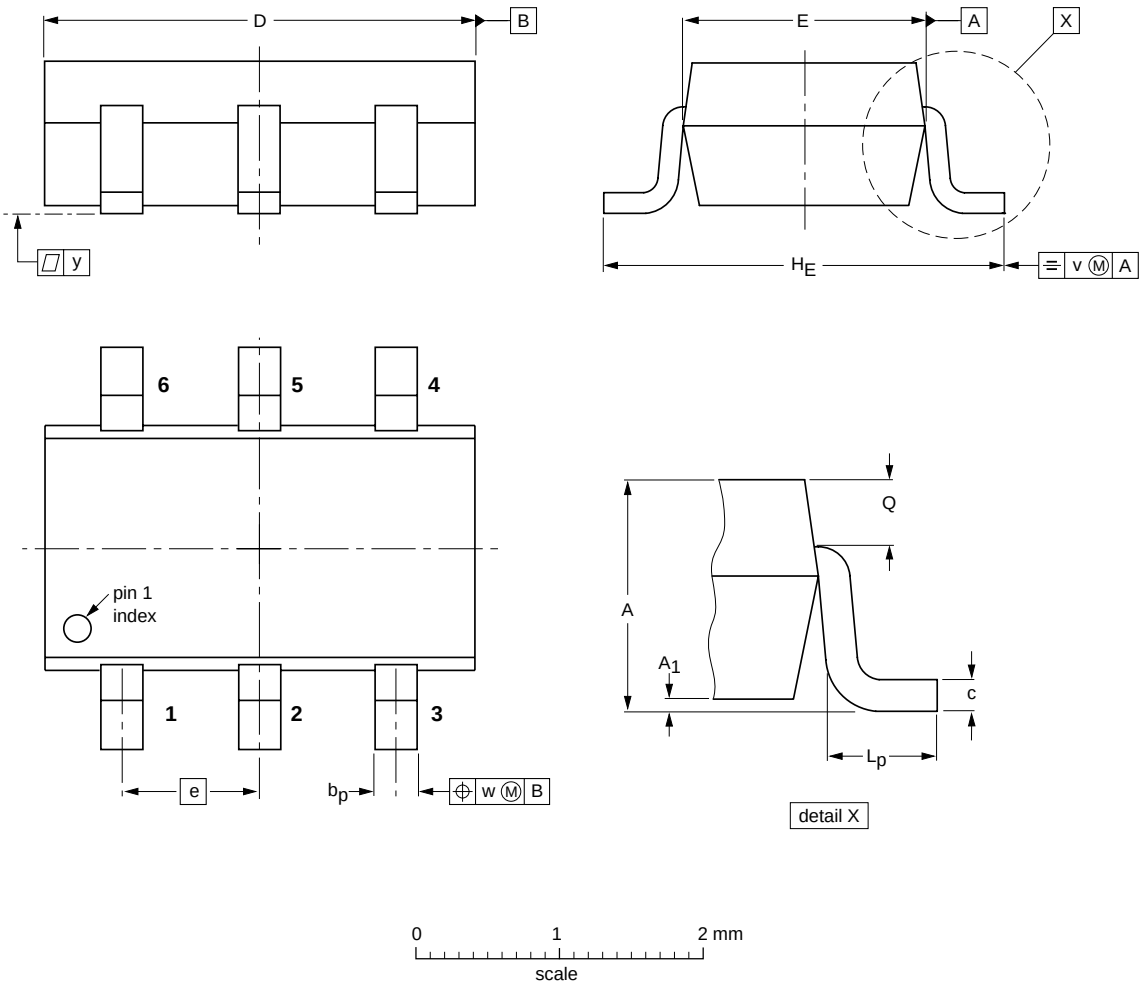


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Plastic surface mounted package; 6 leads **SOT457**

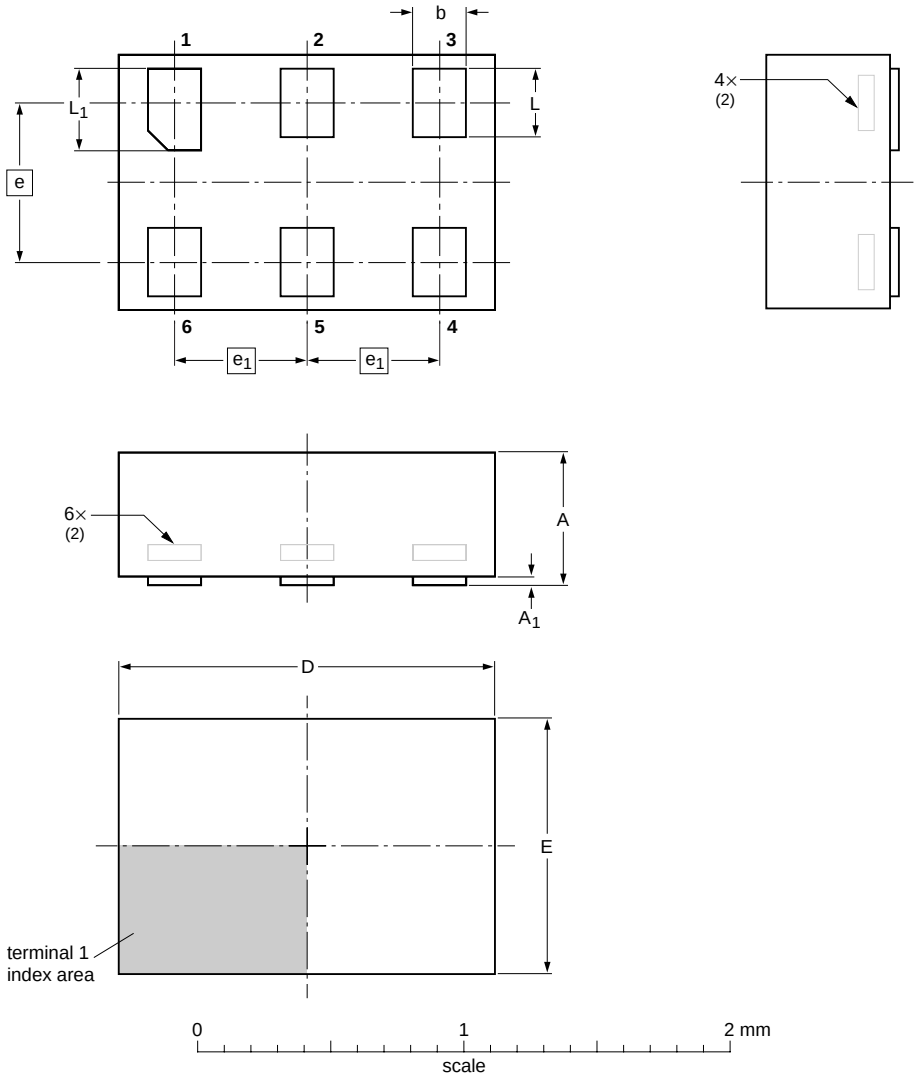


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			~~97-02-28~~ 01-05-04

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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