

64K x 16 Static RAM

Features

- 3.3V operation (3.0V–3.6V)
- High speed
 - $t_{AA} = 10, 12, 15$ ns
- CMOS for optimum speed/power
- Low Active Power (L version)
 - 576 mW (max.)
- Low CMOS Standby Power (L version)
 - 1.80 mW (max.)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in 44-pin TSOP II and 400-mil SOJ
- Available in a 48-Ball Mini BGA package

Functional Description^[1]

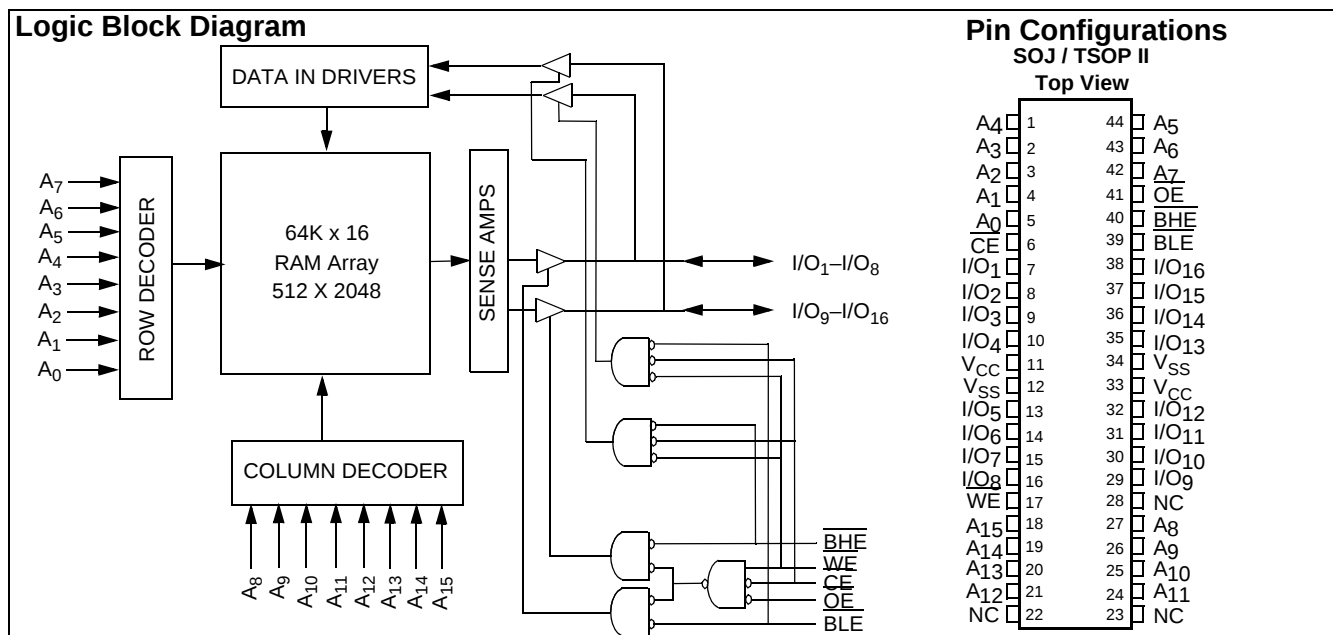
The CY7C1021BNV is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{15}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1021BNV is available in 400-mil-wide SOJ, standard 44-pin TSOP Type II, and 48-ball mini BGA packages.



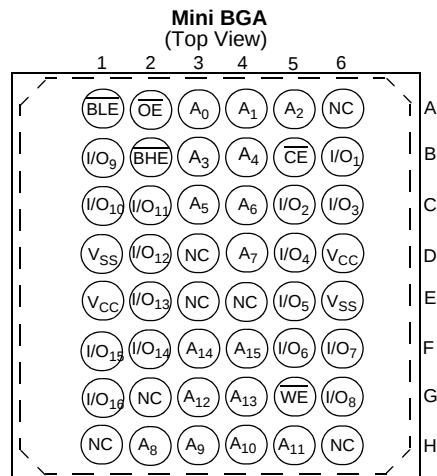
Note:

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com

Selection Guide

			-10	-12	-15
Maximum Access Time (ns)			10	12	15
Maximum Operating Current (mA)	Commercial		160	150	140
	Industrial		180	170	160
Maximum CMOS Standby Current (mA)	Commercial/Industrial		5	5	5
		L	0.5	0.5	0.5

Pin Configurations



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State^[1] -0.5V to $V_{CC}+0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC}+0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%

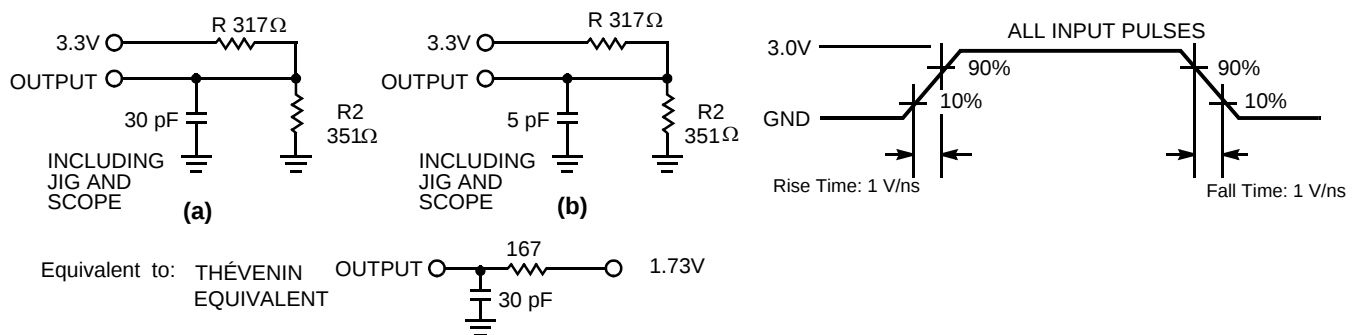
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC}+0.3V$	2.2	$V_{CC}+0.3V$	2.2	$V_{CC}+0.3V$	V
V_{IL}	Input LOW Voltage ^[1]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1	+1	-1	+1	-1	+1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT}=0\text{mA}$ $f = f_{MAX} = 1/t_{RC}$	Com'l	160		150		140	mA
			Ind'l	120		170		160	mA
I_{SB1}	Automatic CE Powerdown Current —TTL Inputs	Max. V_{CC} , $CE \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		40		40		40	mA
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	Max. V_{CC} , $CE \geq V_{CC}-0.3V$, $V_{IN} \geq V_{CC}-0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$		5		5		5	mA
			L	500		500		500	μA

Capacitance^[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms



Note:

1. Minimum voltage is -2.0V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[3] Over the Operating Range

Parameter	Description	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	10		12		15		ns
t _{AA}	Address to Data Valid		10		12		15	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		4		6		7	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[4, 5]		5		6		7	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[5]	3		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[4, 5]		5		6		7	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		12		12		15	ns
t _{DBE}	Byte Enable to Data Valid		5		6		7	ns
t _{LZBE}	Byte Enable to Low Z	0		0		0		ns
t _{HZBE}	Byte Disable to High Z		5		6		7	ns
WRITE CYCLE ^[6]								
t _{WC}	Write Cycle Time	10		12		15		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	8		9		10		ns
t _{AW}	Address Set-Up to Write End	7		8		10		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	WE Pulse Width	8		8		10		ns
t _{SD}	Data Set-Up to Write End	6		6		8		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[5]	3		3		3		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[4, 5]		5		6		7	ns
t _{BW}	Byte Enable to End of Write	8		8		9		ns

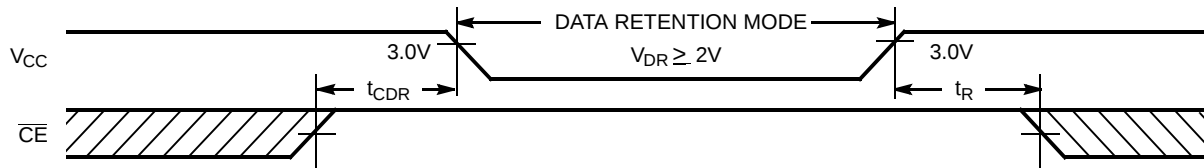
Data Retention Characteristics Over the Operating Range (L version only)

Parameter	Description		Conditions ^[7]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l	$V_{CC} = V_{DR} = 2.0V$, $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		100	μA
$t_{CDR}^{[8]}$	Chip Deselect to Data Retention Time			0		ns
$t_R^{[9]}$	Operation Recovery Time			t_{RC}		ns

Notes:

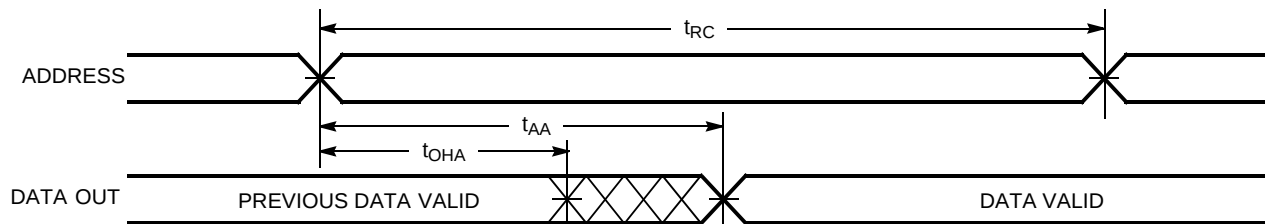
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of CE LOW, WE LOW and BHE / BLE LOW. CE , WE and BHE / BLE must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- No input may exceed $V_{CC} + 0.5V$.
- Tested initially and after any design or process changes that may affect these parameters.
- $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.

Data Retention Waveform

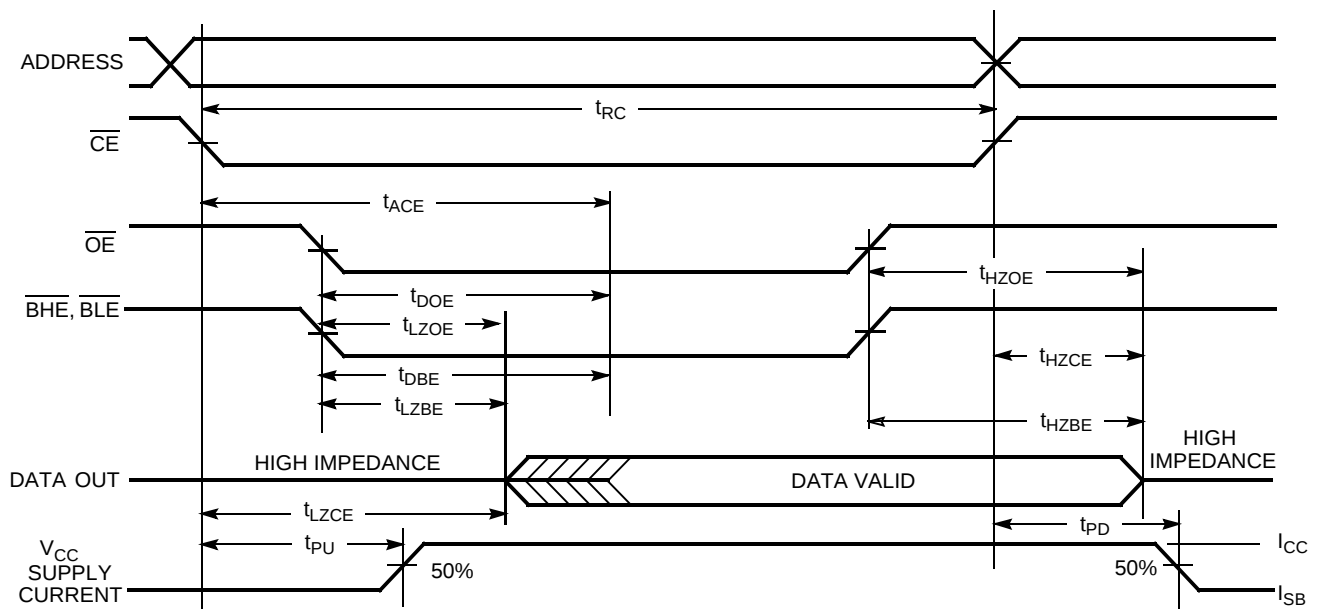


Switching Waveforms

Read Cycle No. 1^[10, 11]



Read Cycle No. 2 ($\overline{OE}$ Controlled)^[11, 12]

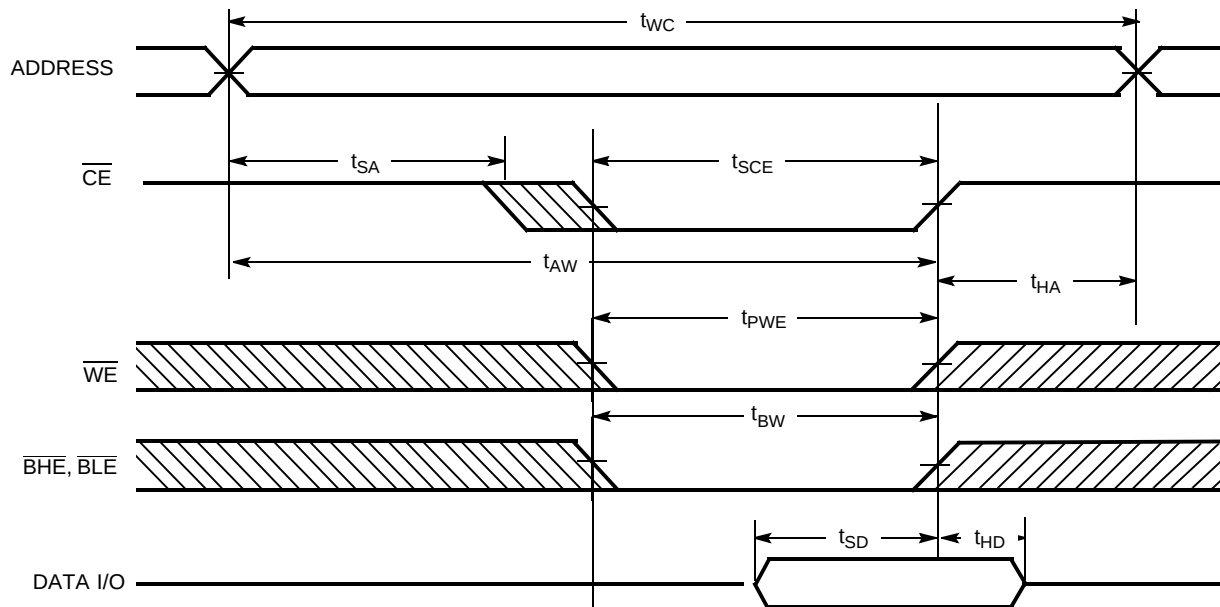


Notes:

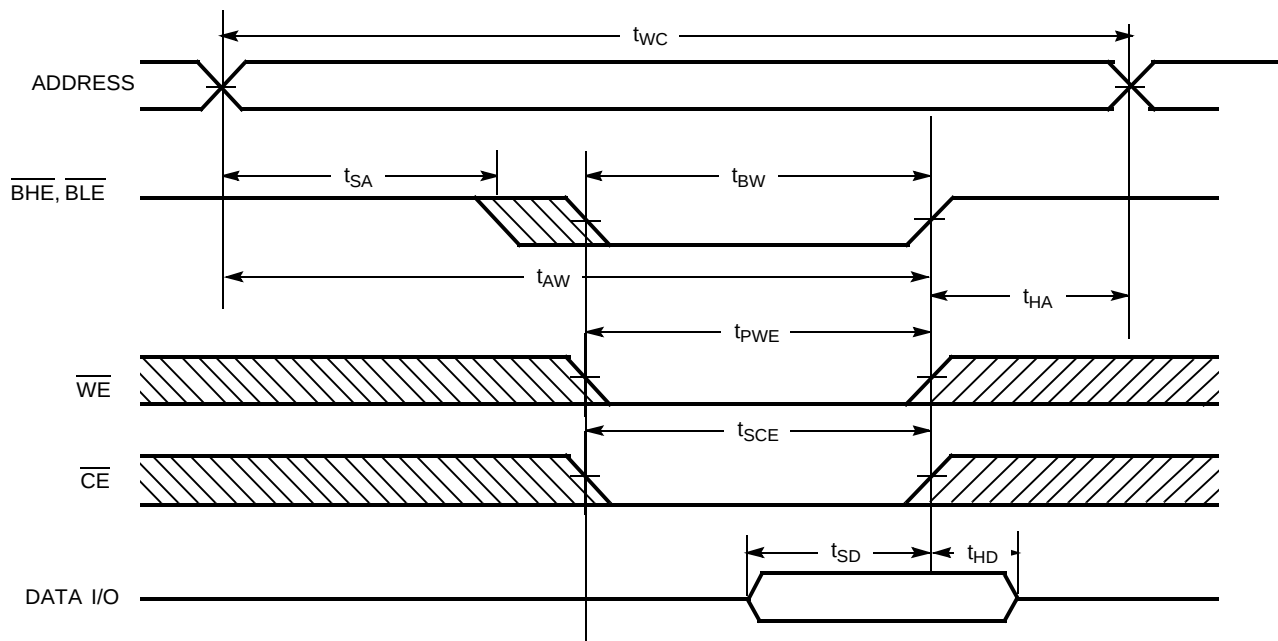
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL} .
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[13, 14]



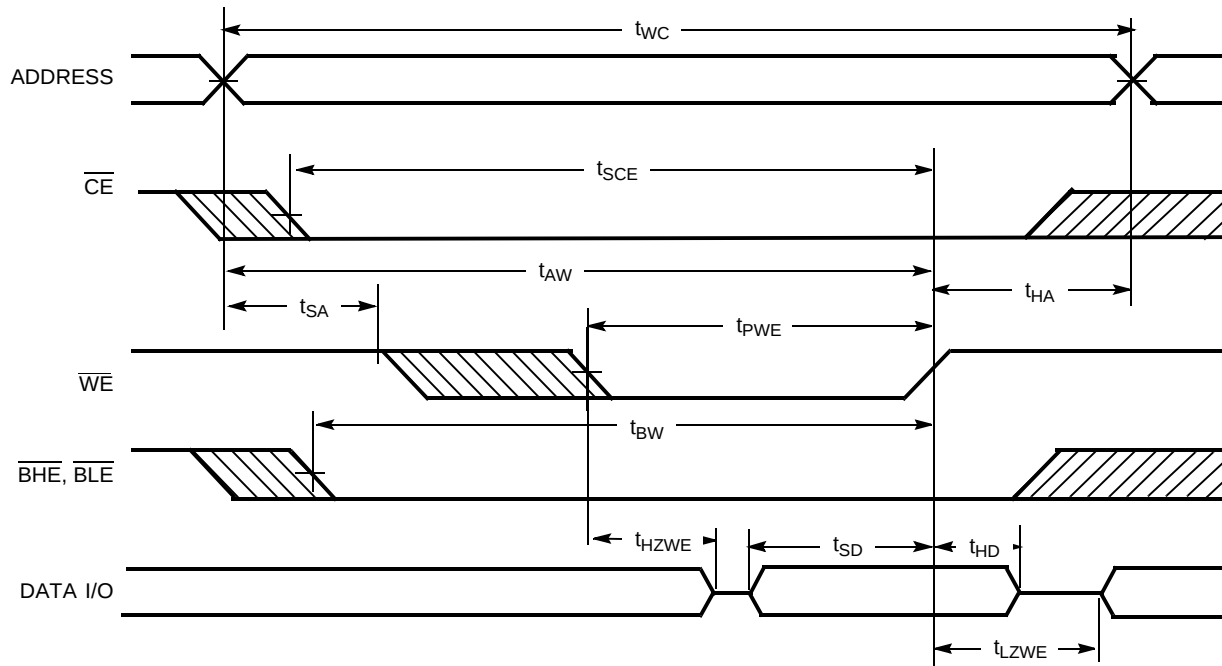
Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)



Notes:

13. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.

14. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)

Truth Table

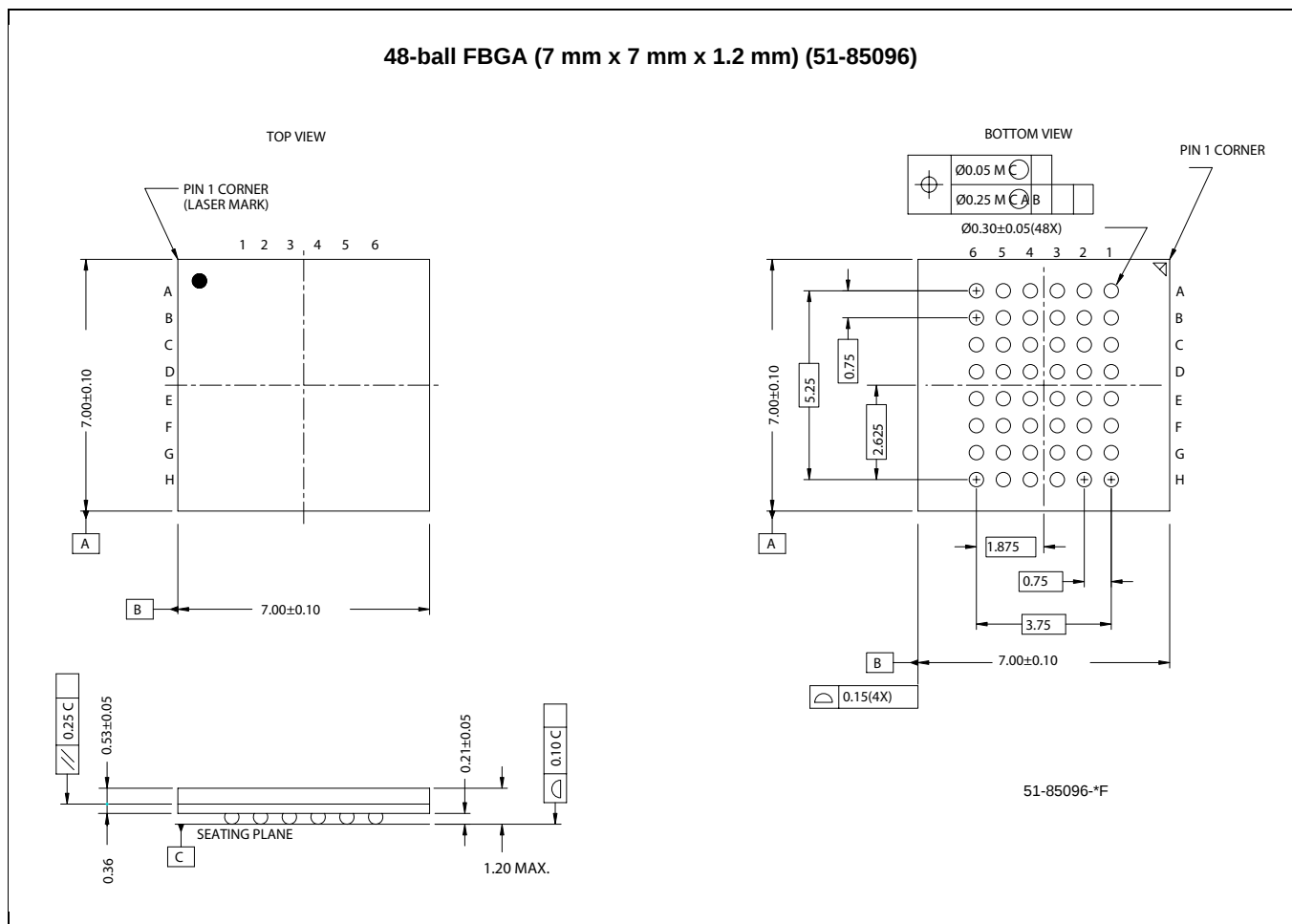
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O ₁ –I/O ₈	I/O ₉ –I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I_{CC})
			L	H	Data Out	High Z	Read - Lower bits only	Active (I_{CC})
			H	L	High Z	Data Out	Read - Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I_{CC})
			L	H	Data In	High Z	Write - Lower bits only	Active (I_{CC})
			H	L	High Z	Data In	Write - Upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021BNV33L-10VXC	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	Commercial
	CY7C1021BNV33L-10ZXC	51-85087	44-Lead TSOP Type II (Pb-free)	
12	CY7C1021BNV33L-12ZC	51-85087	44-Lead TSOP Type II	
	CY7C1021BNV33L-12ZXC	51-85087	44-Lead TSOP Type II (Pb-free)	
15	CY7C1021BNV33L-15ZC	51-85087	44-Lead TSOP Type II	Industrial
	CY7C1021BNV33L-15ZXC	51-85087	44-Lead TSOP Type II (Pb-free)	
	CY7C1021BNV33L-15VXC	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021BNV33L-15BAI	51-85096	48-ball Mini Ball Grid Array (7 mm x 7 mm)	
	CY7C1021BNV33L-15VXI	51-85082	44-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1021BNV33L-15ZXI	51-85087	44-Lead TSOP Type II (Pb-free)	
	CY7C1021BNV33L-15ZI	51-85087	44-Lead TSOP Type II	

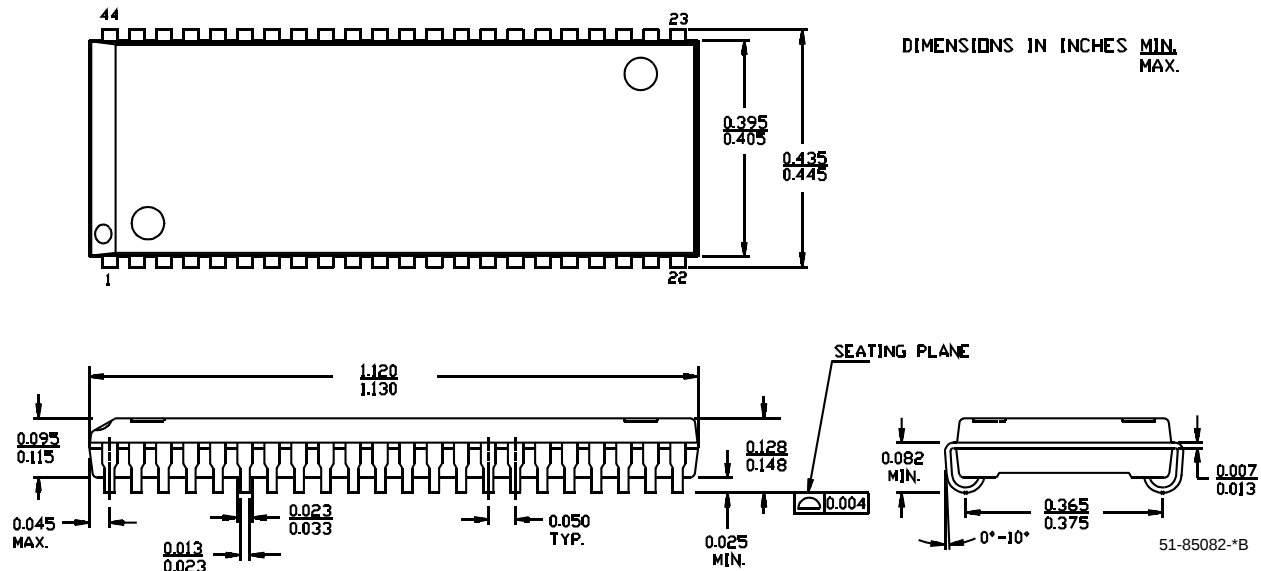
Please contact local sales representative regarding availability of these parts.

Package Diagrams



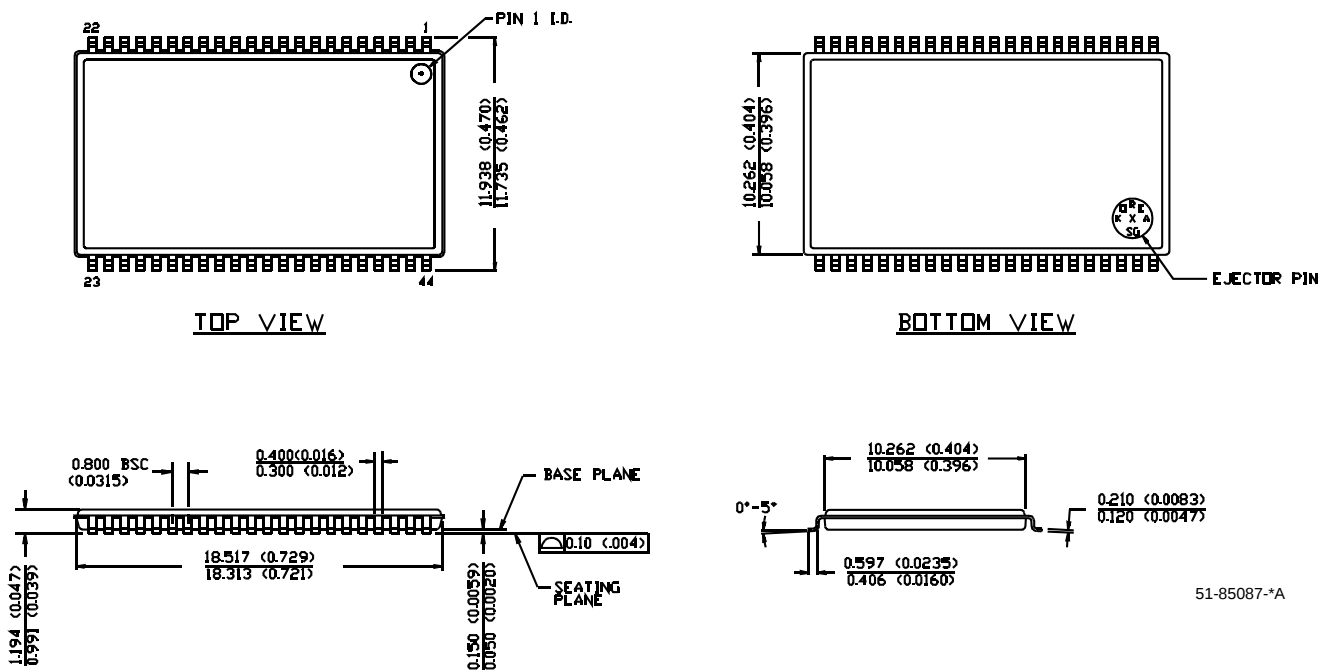
Package Diagrams (continued)

44-Lead (400-Mil) Molded SOJ (51-85082)



44-Pin TSOP Type II (51-85087)

**DIMENSION IN MM (INCH)
MAX
MIN.**



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Document History Page

Document Title: CY7C1021BNV33 64K x 16 Static RAM Document Number: 001-06433				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	423847	See ECN	NXR	New Data Sheet