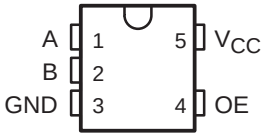
- **5-Ω Switch Connection Between Two Ports**
- **CMOS-Compatible Control Input Levels**

DBV OR DCK PACKAGE
(TOP VIEW)



description

The SN74CBT1G66 features a single high-speed line switch. The switch is disabled when the output-enable (OE) input is low.

ORDERING INFORMATION

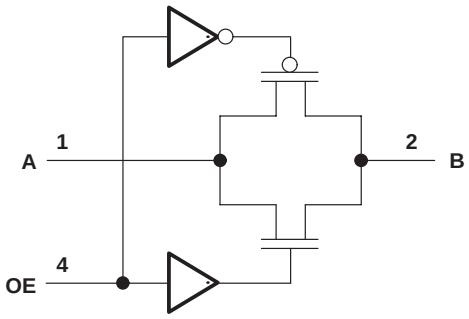
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74CBT1G66DBVR	S66_
	SOP (SC-70) – DCK	Tape and reel	SN74CBT1G66DCKR	S6_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT OE	FUNCTION
H	A port = B port
L	Disconnect

logic diagram (positive logic)



PRODUCT PREVIEW

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package . . . . . 206°C/W
DCK package . . . . . 252°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		$0.7 \times V_{CC}$		V
V_{IL}	Low-level input voltage			$0.3 \times V_{CC}$	V
V_{IN}	Control input voltage		0	5.5	V
t_r/t_f	Control input transition rise/fall time	V_{CC} = 2.3 V to 3.6 V		10	ns
		V_{CC} = 4.5 V to 5.5 V		5	
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP‡	MAX	UNIT
V_{IK}	I_I = –18 mA		4.5 V			–1.2	V
I_I	$0 \le V_I \le 5.5$ V		0 to 5.5 V			±1	µA
I_{off}	$0 \le$ A or B ≤ 4.5 V		V_{CC} = 0			10	µA
I_{OZ}	$0 \le$ A or B $\le V_{CC}$		2.3 V to 5.5 V			±10	µA
r_{on}	V_I = 0	I_I = 8 mA	2.3 V		5	12	Ω
	V_I = 2.3 V				13	30	
	V_I = 0	I_I = 24 mA	3 V		4	9	
	V_I = 3 V				10	20	
	V_I = 0,	I_I = 30 mA	4.5 V		3	7	
	V_I = 2.4 V,	I_I = 15 mA			5	12	
	V_I = 4.5 V,	I_I = 30 mA			7	15	
I_{CC}	$V_I = V_{CC}$ or GND	I_O = 0	5.5 V			10	µA
C_i			0				pF
C_{io}			5 V				pF

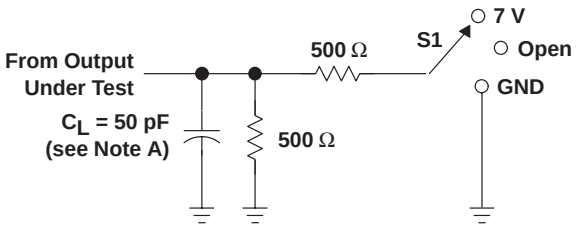
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PRODUCT PREVIEW

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

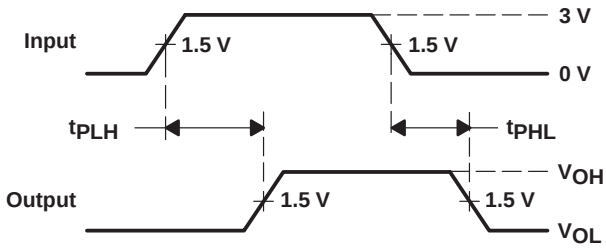
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	B or A							ns
t_{en}	OE	A or B							ns
t_{dis}	OE	A or B							ns

PARAMETER MEASUREMENT INFORMATION

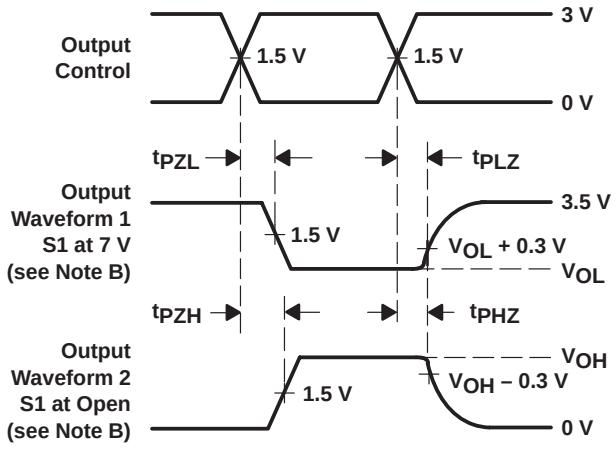


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74CBT1G66DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI
SN74CBT1G66DCKR	PREVIEW	SC70	DCK	5	3000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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