LPC11E6x

32-bit ARM Cortex-M0+ microcontroller; up to 256 kB flash and 36 kB SRAM; 4 kB EEPROM; 12-bit ADC

Rev. 1.5 — 12 August 2020 Product data sheet

1. General description

The LPC11E6x are an ARM Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 50 MHz. The LPC11E6x support up to 256 KB of flash memory, a 4 KB EEPROM, and 36 KB of SRAM.

The ARM Cortex-M0+ is an easy-to-use, energy-efficient core using a two-stage pipeline and fast single-cycle I/O access.

The peripheral complement of the LPC11E6x includes a DMA controller, a CRC engine, two I^2C-bus interfaces, up to five USARTs, two SSP interfaces, PWM/timer subsystem with six configurable multi-purpose timers, a Real-Time Clock, one 12-bit ADC, temperature sensor, function-configurable I/O ports, and up to 80 general-purpose I/O pins.

For additional documentation related to the LPC11E6x parts, see Section 18 “References”.

2. Features and benefits

- System:
  - ARM Cortex-M0+ processor (version r0p1), running at frequencies of up to 50 MHz with single-cycle multiplier and fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - AHB Multilayer matrix.
  - System tick timer.
  - Serial Wire Debug (SWD) and JTAG boundary scan modes supported.
  - Micro Trace Buffer (MTB) supported.
- Memory:
  - Up to 256 KB on-chip flash programming memory with page erase.
  - Up to 32 KB main SRAM.
  - Up to two additional SRAM blocks of 2 KB each.
  - Up to 4 KB EEPROM.
- ROM API support:
  - Boot loader.
  - USART drivers.
  - I2C drivers.
  - DMA drivers.
  - Power profiles.
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).

- 32-bit integer division routines.

- Digital peripherals:
  - Simple DMA engine with 16 channels and programmable input triggers.
  - High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 80 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors, programmable open-drain mode, input inverter, and programmable glitch filter and digital filter.
  - Pin interrupt and pattern match engine using eight selectable GPIO pins.
  - Two GPIO group interrupt generators.
  - CRC engine.
- Configurable PWM/timer subsystem (two 16-bit and two 32-bit standard counter/timers, two State-Configurable Timers (SCTimer/PWM)) that provides:
  - Up to four 32-bit and two 16-bit counter/timers or two 32-bit and six 16-bit counter/timers.
  - Up to 21 match outputs and 16 capture inputs.
  - Up to 19 PWM outputs with 6 independent time bases.
- Windowed WatchDog timer (WWDT).
- Real-time Clock (RTC) in the always-on power domain with separate battery supply pin and 32 kHz oscillator.
- Analog peripherals:
  - One 12-bit ADC with up to 12 input channels with multiple internal and external trigger inputs and with sample rates of up to 2 Msamples/s. The ADC supports two independent conversion sequences.
  - Temperature sensor.
- Serial interfaces:
  - Up to five USART interfaces, all with DMA, synchronous mode, and RS-485 mode support. Four USARTs use a shared fractional baud generator.
  - Two SSP controllers with DMA support.
  - Two I^2C-bus interfaces. One I^2C-bus interface with specialized open-drain pins supports I2C Fast-mode Plus.
- Clock generation:
  - 12 MHz internal RC oscillator trimmed to 1 % accuracy for $-25\ °C \leq T_{amb} \leq +85\ °C$ that can optionally be used as a system clock.
  - On-chip 32 kHz oscillator for RTC.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz. Oscillator pins are shared with the GPIO pins.
  - Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
  - PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal.
  - Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
  - Integrated PMU (Power Management Unit) to minimize power consumption.
  - Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
  - Wake-up from Deep-sleep and Power-down modes on external pin inputs and USART activity.

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- Power-On Reset (POR).
- Brownout detect.

- Unique device serial number for identification.
- Single power supply (2.4 V to 3.6 V).
- Separate VBAT supply for RTC.
- Operating temperature range -40 °C to 105 °C.
- Available as LQFP48, LQFP64, and LQFP100 packages.

3. Applications

- Three-phase e-meter
- GPS tracker
- Gaming accessories
- Car radio
- Medical monitor
- PC peripherals

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11E66JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11E67JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11E67JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11E67JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC11E68JBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC11E68JBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC11E68JBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/ KB	EEPROM/ KB	SRAM/ KB	USART0	USART1	USART2	USART3	USART4	I^2C	SSP	PWM/ timers	12-bit ADC channels	GPIO
LPC11E66JBD48	64	4	12	Y	Y	Y	Y	N	2	2	6	8	36
LPC11E67JBD48	128	4	20	Y	Y	Y	Y	N	2	2	6	8	36
LPC11E67JBD64	128	4	20	Y	Y	Y	Y	N	2	2	6	10	50
LPC11E67JBD100	128	4	20	Y	Y	Y	Y	Y	2	2	6	12	80
LPC11E68JBD48	256	4	36	Y	Y	Y	Y	N	2	2	6	8	36
LPC11E68JBD64	256	4	36	Y	Y	Y	Y	N	2	2	6	10	50
LPC11E68JBD100	256	4	36	Y	Y	Y	Y	Y	2	2	6	12	80

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5. Marking

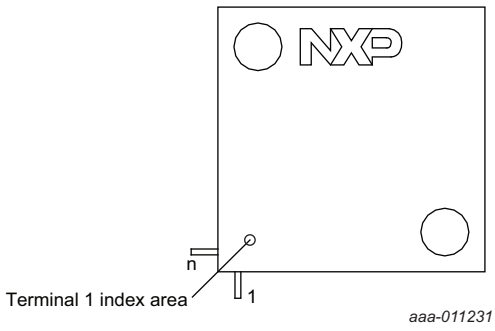


Fig 1. LQFP64/100 package marking

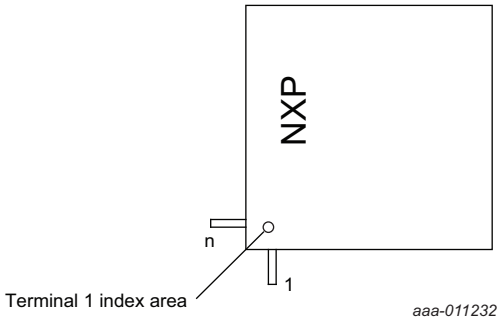


Fig 2. LQFP48 package marking

5.1 Product identification

The LPC11E6x devices typically have the following top-side marking for LQFP100 packages:

LPC11E6xJBD100

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP64 packages:

LPC11E6xJ

xxxxxx xx

xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP48 packages:

LPC11E6xJ

xx xx

xxxyy

wwxR[x]

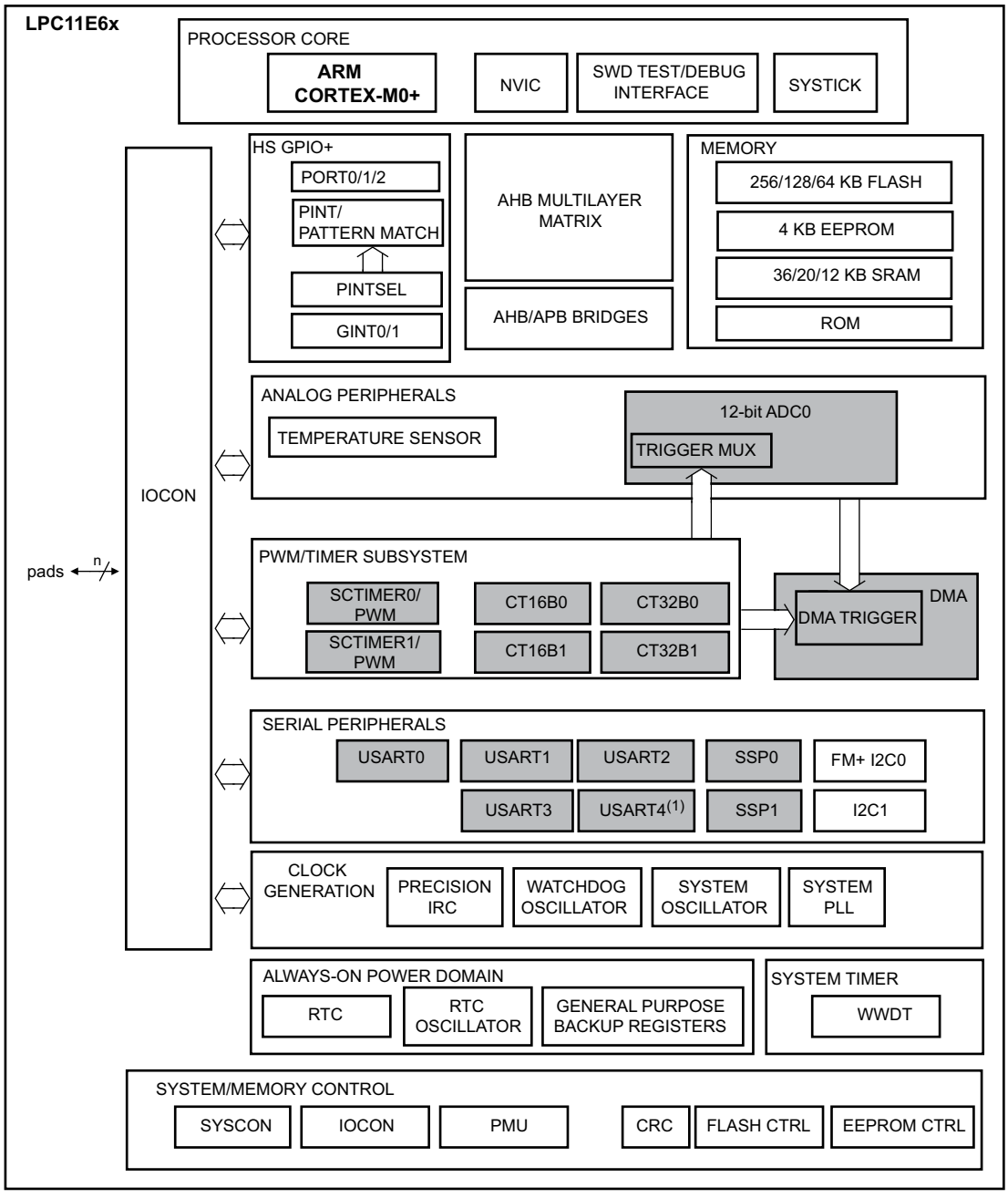
Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

Field ‘R’ identifies the device revision.

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6. Block diagram



Gray-shaded blocks show peripherals that can provide hardware triggers for DMA transfers or have DMA request lines.

(1) Available on LQFP100 packages only.

Fig 3. LPC11E6x block diagram

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7. Pinning information

7.1 Pinning

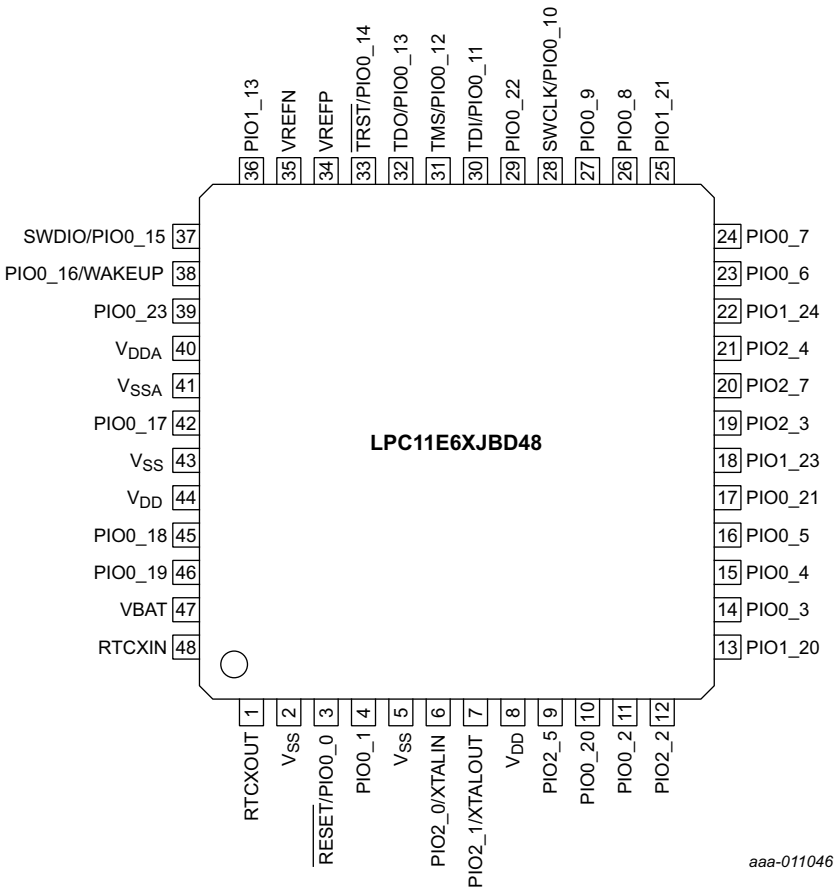


Fig 4. LQFP48 pinning

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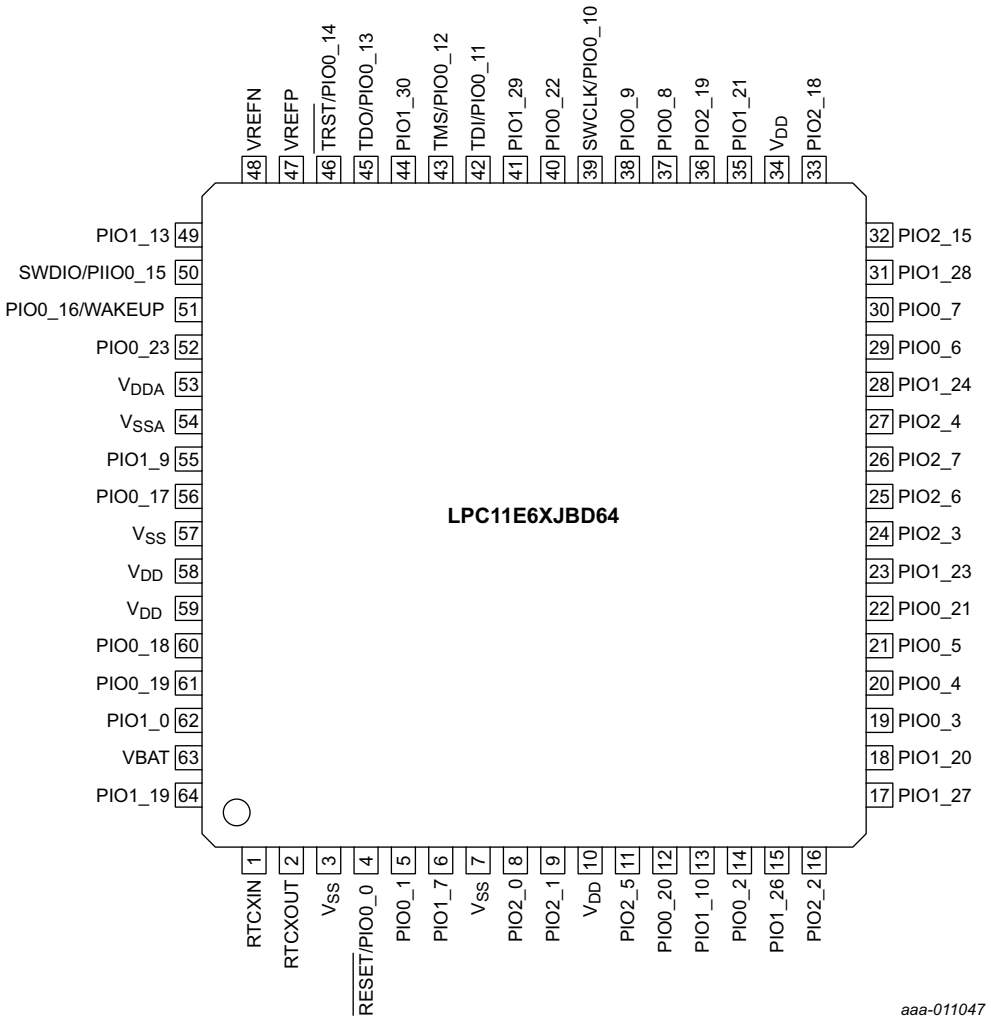


Fig 5. LQFP64 pinning

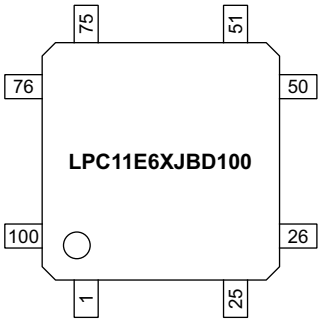


Fig 6. LQFP100 pinning

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7.2 Pin description

Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
$\overline{\text{RESET}}$/PIO0_0	3	4	8	[8]	I; PU	I	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode. In deep power-down mode, this pin must be pulled HIGH externally. The $\overline{\text{RESET}}$ pin can be left unconnected or be used as a GPIO pin if an external $\overline{\text{RESET}}$ function is not needed and Deep power-down is not used.
						IO	**PIO0_0 —** General-purpose digital input/output pin.
PIO0_1	4	5	9	[6]	I; PU	IO	**PIO0_1 —** General-purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
						O	**CLKOUT —** Clockout pin.
						O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO0_2	11	14	19	[6]	I; PU	IO	**PIO0_2 —** General-purpose port 0 input/output 2.
						IO	**SSP0_SSEL —** Slave select for SSP0.
						I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
						-	**R_0 —** Reserved.
PIO0_3	14	19	30	[6]	I; PU	IO	**PIO0_3 —** General-purpose digital input/output pin.
						-	**R —** Reserved.
							R_1 — Reserved.
PIO0_4	15	20	31	[7]	IA	IO	**PIO0_4 —** General-purpose port 0 input/output 4 (open-drain).
						IO	**I2C0_SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	**R_2 —** Reserved.
PIO0_5	16	21	32	[7]	IA	IO	**PIO0_5 —** General-purpose port 0 input/output 5 (open-drain).
						IO	**I2C0_SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
						-	**R_3 —** Reserved.
PIO0_6	23	29	44	[6]	I; PU	IO	**PIO0_6 —** General-purpose port 0 input/output 6.
						-	**R —** Reserved.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						-	**R_4 —** Reserved.

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO0_7	24	30	45	[5]	I; PU	IO	**PIO0_7 —** General-purpose port 0 input/output 7 (high-current output driver).
						I	**$\overline{\text{U0_CTS}}$ —** Clear To Send input for USART.
						-	**R_5 —** Reserved.
						IO	**I2C1_SCL —** I^2C-bus clock input/output. This pin is not open-drain.
PIO0_8	26	37	58	[6]	I; PU	IO	**PIO0_8 —** General-purpose port 0 input/output 8.
						IO	**SSP0_MISO —** Master In Slave Out for SSP0.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	**R_6 —** Reserved.
PIO0_9	27	38	59	[6]	I; PU	IO	**PIO0_9 —** General-purpose port 0 input/output 9.
						IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
						O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	**R_7 —** Reserved.
SWCLK/PIO0_10	28	39	60	[6]	I; PU	IO	**SWCLK —** Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
						IO	**PIO0_10 —** General-purpose digital input/output pin.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						O	**CT16B0_MAT2 —** 16-bit timer0 MAT2
TDI/PIO0_11	30	42	64	[3]	I; PU	IO	**TDI —** Test Data In for JTAG interface. In boundary scan mode only.
						IO	**PIO0_11 —** General-purpose digital input/output pin.
						AI	**ADC_9 —** A/D converter, input channel 9.
						O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
						O	**$\overline{\text{U1_RTS}}$ —** Request To Send output for USART1.
						IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
TMS/PIO0_12	31	43	66	[3]	I; PU	IO	**TMS —** Test Mode Select for JTAG interface. In boundary scan mode only.
						IO	**PIO0_12 —** General-purpose digital input/output pin.
						AI	**ADC_8 —** A/D converter, input channel 8.
						I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
						I	**$\overline{\text{U1_CTS}}$ —** Clear To Send input for USART1.
TDO/PIO0_13	32	45	68	[3]	I; PU	IO	**TDO —** Test Data Out for JTAG interface. In boundary scan mode only.
						IO	**PIO0_13 —** General-purpose digital input/output pin.
						AI	**ADC_7 —** A/D converter, input channel 7.
						O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
						I	**U1_RXD —** Receiver input for USART1.

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
TRST/PIO0_14	33	46	69	[3]	I; PU	IO	**TRST —** Test Reset for JTAG interface. In boundary scan mode only.
						IO	**PIO0_14 —** General-purpose digital input/output pin.
						AI	**ADC_6 —** A/D converter, input channel 6.
						O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						O	**U1_TXD —** Transmitter output for USART1.
SWDIO/PIO0_15	37	50	81	[3]	I; PU	IO	**SWDIO —** Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
						IO	**PIO0_15 —** General-purpose digital input/output pin.
						AI	**ADC_3 —** A/D converter, input channel 3.
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO0_16/WAKEUP	38	51	82	[4]	I; PU	IO	**PIO0_16 —** General-purpose digital input/output pin. This pin also serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
						I	**ADC_2 —** A/D converter, input channel 2.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_8 —** Reserved.
PIO0_17	42	56	90	[6]	I; PU	IO	**PIO0_17 —** General-purpose digital input/output pin.
						O	**U0_RTS —** Request To Send output for USART0.
						I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						IO	**U0_SCLK —** Serial clock input/output for USART0 in synchronous mode.
PIO0_18	45	60	94	[6]	I; PU	IO	**PIO0_18 —** General-purpose digital input/output pin.
						I	**U0_RXD —** Receiver input for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO0_19	46	61	95	[6]	I; PU	IO	**PIO0_19 —** General-purpose digital input/output pin.
						O	**U0_TXD —** Transmitter output for USART0. Used in UART ISP mode.
						O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO0_20	10	12	17	[6]	I; PU	IO	**PIO0_20 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
						I	**U2_RXD —** Receiver input for USART2.
PIO0_21	17	22	33	[6]	I; PU	IO	**PIO0_21 —** General-purpose digital input/output pin.
						O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO0_22	29	40	62	[3]	I; PU	IO	**PIO0_22 —** General-purpose digital input/output pin.
						AI	**ADC_11 —** A/D converter, input channel 11.
						I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						IO	**SSP1_MISO —** Master In Slave Out for SSP1.
PIO0_23	39	52	83	[3]	I; PU	IO	**PIO0_23 —** General-purpose digital input/output pin.
						AI	**ADC_1 —** A/D converter, input channel 1.
						-	**R_9 —** Reserved.
						I	**$\overline{\text{U0_RI}}$ —** Ring Indicator input for USART0.
						IO	**SSP1_SSEL —** Slave select for SSP1.
PIO1_0	-	62	97	[6]	I; PU	IO	**PIO1_0 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
						-	**R_10 —** Reserved.
						O	**U2_TXD —** Transmitter output for USART2.
PIO1_1	-	-	28	[6]	I; PU	IO	**PIO1_1 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
						-	**R_11 —** Reserved.
						O	**$\overline{\text{U0_DTR}}$ —** Data Terminal Ready output for USART0.
PIO1_2	-	-	55	[6]	I; PU	IO	**PIO1_2 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	**R_12 —** Reserved.
						I	**U1_RXD —** Receiver input for USART1.
PIO1_3	-	-	72	[3]	I; PU	IO	**PIO1_3 —** General-purpose digital input/output pin.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_13 —** Reserved.
						IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).
						AI	**ADC_5 —** A/D converter, input channel 5.
PIO1_4	-	-	23	[6]	I; PU	IO	**PIO1_4 —** General-purpose digital input/output pin.
						I	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
						-	**R_14 —** Reserved.
						I	**$\overline{\text{U0_DSR}}$ —** Data Set Ready input for USART0.
PIO1_5	-	-	47	[6]	I; PU	IO	**PIO1_5 —** General-purpose digital input/output pin.
						I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						-	**R_15 —** Reserved.
						I	**$\overline{\text{U0_DCD}}$ —** Data Carrier Detect input for USART0.
PIO1_6	-	-	98	[6]	I; PU	IO	**PIO1_6 —** General-purpose digital input/output pin.
						-	**R_16 —** Reserved.
						I	**U2_RXD —** Receiver input for USART2.
						I	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_7	-	6	10	[6]	I; PU	IO	**PIO1_7 —** General-purpose digital input/output pin.
						-	**R_17 —** Reserved.
						I	**$\overline{\text{U2_CTS}}$ —** Clear To Send input for USART2.
						I	**CT16B1_CAP0 —** Capture input 0 for 32-bit timer 1.
PIO1_8	-	-	61	[6]	I; PU	IO	**PIO1_8 —** General-purpose digital input/output pin.
						-	**R_18 —** Reserved.
						O	**U1_TXD —** Transmitter output for USART1.
						I	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO1_9	-	55	86	[3]	I; PU	IO	**PIO1_9 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0_CTS}}$ —** Clear To Send input for USART0.
						O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						AI	**ADC_0 —** A/D converter, input channel 0.
PIO1_10	-	13	18	[6]	I; PU	IO	**PIO1_10 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U2_RTS}}$ —** Request To Send output for USART2.
						IO	**U2_SCLK —** Serial clock input/output for USART2 in synchronous mode.
						O	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_11	-	-	65	[6]	I; PU	IO	**PIO1_11 —** General-purpose digital input/output pin.
						IO	**I2C1_SCL —** I^2C1-bus clock input/output (not open-drain).
						O	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
						I	**$\overline{\text{U0_RI}}$ —** Ring Indicator input for USART0.
PIO1_12	-	-	89	[6]	I; PU	IO	**PIO1_12 —** General-purpose digital input/output pin.
						IO	**SSP0_MOSI —** Master Out Slave In for SSP0.
						O	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
						-	**R_21 —** Reserved.
PIO1_13	36	49	78	[6]	I; PU	IO	**PIO1_13 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U1_CTS}}$ —** Clear To Send input for USART1.
						O	**SCT0_OUT3 —** SCTimer0/PWM output 3.
						-	**R_22 —** Reserved.
PIO1_14	-	-	79	[6]	I; PU	IO	**PIO1_14 —** General-purpose digital input/output pin.
						IO	**I2C1_SDA —** I^2C1-bus data input/output (not open-drain).
						O	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
						-	**R_23 —** Reserved.
PIO1_15	-	-	87	[6]	I; PU	IO	**PIO1_15 —** General-purpose digital input/output pin.
						IO	**SSP0_SSEL —** Slave select for SSP0.
						O	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
						-	**R_24 —** Reserved.

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_16	-	-	96	[6]	I; PU	IO	**PIO1_16 —** General-purpose digital input/output pin.
						IO	**SSP0_MISO —** Master In Slave Out for SSP0.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
						-	**R_25 —** Reserved.
PIO1_17	-	-	34	[6]	I; PU	IO	**PIO1_17 —** General-purpose digital input/output pin.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R_26 —** Reserved.
PIO1_18	-	-	43	[6]	I; PU	IO	**PIO1_18 —** General-purpose digital input/output pin.
						I	**CT16B1_CAP1 —** Capture input 1 for 16-bit timer 1.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R_27 —** Reserved.
PIO1_19	-	64	4	[6]	I; PU	IO	**PIO1_19 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U2_CTS}}$ —** Clear To Send input for USART2.
						O	**SCT0_OUT0 —** SCTimer0/PWM output 0.
						-	**R_28 —** Reserved.
PIO1_20	13	18	29	[6]	I; PU	IO	**PIO1_20 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0_DSR}}$ —** Data Set Ready input for USART0.
						IO	**SSP1_SCK —** Serial clock for SSP1.
						O	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.
PIO1_21	25	35	56	[6]	I; PU	IO	**PIO1_21 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U0_DCD}}$ —** Data Carrier Detect input for USART0.
						IO	**SSP1_MISO —** Master In Slave Out for SSP1.
						I	**CT16B0_CAP2 —** Capture input 2 for 16-bit timer 0.
PIO1_22	-	-	80	[3]	I; PU	IO	**PIO1_22 —** General-purpose digital input/output pin.
						IO	**SSP1_MOSI —** Master Out Slave In for SSP1.
						I	**CT32B1_CAP1 —** Capture input 1 for 32-bit timer 1.
						AI	**ADC_4 —** A/D converter, input channel 4.
						-	**R_29 —** Reserved.
PIO1_23	18	23	35	[6]	I; PU	IO	**PIO1_23 —** General-purpose digital input/output pin.
						O	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
						IO	**SSP1_SSEL —** Slave select for SSP1.
						O	**U2_TXD —** Transmitter output for USART2.
PIO1_24	22	28	42	[6]	I; PU	IO	**PIO1_24 —** General-purpose digital input/output pin.
						O	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
						IO	**I2C1_SDA —** I^2C-bus data input/output (not open-drain).

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO1_25	-	-	100	[6]	I; PU	IO	**PIO1_25 —** General-purpose digital input/output pin.
						O	**U2_RTS —** Request To Send output for USART2.
						IO	**U2_SCLK —** Serial clock input/output for USART2 in synchronous mode.
						I	**SCT0_IN0 —** SCTimer0/PWM input 0.
						-	**R_30 —** Reserved.
PIO1_26	-	15	20	[6]	I; PU	IO	**PIO1_26 —** General-purpose digital input/output pin.
						O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
						I	**U0_RXD —** Receiver input for USART0.
						-	**R_19 —** Reserved.
PIO1_27	-	17	22	[6]	I; PU	IO	**PIO1_27 —** General-purpose digital input/output pin.
						O	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
						O	**U0_TXD —** Transmitter output for USART0.
						-	**R_20 —** Reserved.
						IO	**SSP1_SCK —** Serial clock for SSP1.
PIO1_28	-	31	46	[6]	I; PU	IO	**PIO1_28 —** General-purpose digital input/output pin.
						I	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
						IO	**U0_SCLK —** Serial clock input/output for USART in synchronous mode.
						O	**$\overline{\text{U0_RTS}}$ —** Request To Send output for USART0.
PIO1_29	-	41	63	[3]	I; PU	IO	**PIO1_29 —** General-purpose digital input/output pin.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						I	**CT32B0_CAP2 —** Capture input 2 for 32-bit timer 0.
						O	**$\overline{\text{U0_DTR}}$ —** Data Terminal Ready output for USART0.
						AI	**ADC_10 —** A/D converter, input channel 10.
PIO1_30	-	44	67	[6]	I; PU	IO	**PIO1_30 —** General-purpose digital input/output pin.
						IO	**I2C1_SCL —** I^2C1-bus clock input/output (not open-drain).
						I	**SCT0_IN3 —** SCTimer0/PWM input 3.
						-	**R_31 —** Reserved.
PIO1_31	-	-	48	[5]	I; PU	IO	**PIO1_31 —** General-purpose digital input/output pin (high-current output driver).
PIO2_0	6	8	12	[9]	I; PU	IO	**PIO2_0 —** General-purpose digital input/output pin.
						AI	**XTALIN —** Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
PIO2_1	7	9	13	[9]	I; PU	IO	**PIO2_1 —** General-purpose digital input/output pin.
						AO	**XTALOUT —** Output from the oscillator amplifier.

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO2_2	12	16	21	[6]	I; PU	IO	**PIO2_2 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U3_RTS}}$ —** Request To Send output for USART3.
						IO	**U3_SCLK —** Serial clock input/output for USART3 in synchronous mode.
						O	**SCT0_OUT1 —** SCTimer0/PWM output 1.
PIO2_3	19	24	36	[6]	I; PU	IO	**PIO2_3 —** General-purpose digital input/output pin.
						I	**U3_RXD —** Receiver input for USART3.
						O	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO2_4	21	27	41	[6]	I; PU	IO	**PIO2_4 —** General-purpose digital input/output pin.
						O	**U3_TXD —** Transmitter output for USART3.
						O	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
PIO2_5	9	11	15	[6]	I; PU	IO	**PIO2_5 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U3_CTS}}$ —** Clear To Send input for USART3.
						I	**SCT0_IN1 —** SCTimer0/PWM input 1.
PIO2_6	-	25	37	[6]	I; PU	IO	**PIO2_6 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U1_RTS}}$ —** Request To Send output for USART1.
						IO	**U1_SCLK —** Serial clock input/output for USART1 in synchronous mode.
						I	**SCT0_IN2 —** SCTimer0/PWM input 2.
PIO2_7	20	26	40	[6]	I; PU	IO	**PIO2_7 —** General-purpose digital input/output pin.
						IO	**SSP0_SCK —** Serial clock for SSP0.
						O	**SCT0_OUT2 —** SCTimer0/PWM output 2.
PIO2_8	-	-	2	[6]	I; PU	IO	**PIO2_8 —** General-purpose digital input/output pin.
						I	**SCT1_IN0 —** SCTimer1/PWM input 0.
PIO2_9	-	-	3	[6]	I; PU	IO	**PIO2_9 —** General-purpose digital input/output pin.
						I	**SCT1_IN1 —** SCTimer1/PWM_IN1
PIO2_10	-	-	16	[6]	I; PU	IO	**PIO2_10 —** General-purpose digital input/output pin.
						O	**$\overline{\text{U4_RTS}}$ —** Request To Send output for USART4.
						IO	**U4_SCLK —** Serial clock input/output for USART4 in synchronous mode.
PIO2_11	-	-	24	[6]	I; PU	IO	**PIO2_11 —** General-purpose digital input/output pin.
						I	**U4_RXD —** Receiver input for USART4.
PIO2_12	-	-	25	[6]	I; PU	IO	**PIO2_12 —** General-purpose digital input/output pin.
						O	**U4_TXD —** Transmitter output for USART4.
PIO2_13	-	-	26	[6]	I; PU	IO	**PIO2_13 —** General-purpose digital input/output pin.
						I	**$\overline{\text{U4_CTS}}$ —** Clear To Send input for USART4.
PIO2_14	-	-	27	[6]	I; PU	IO	**PIO2_14 —** General-purpose digital input/output pin.
						I	**SCT1_IN2 —** SCTimer1/PWM input 2.

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Table 3. Pin description

Pin functions are selected through the IOCON registers. See Table 2 for availability of USART4 pin functions.

Symbol	LQFP48	LQFP64	LQFP100		Reset state[1]	Type	Description of pin functions
PIO2_15	-	32	49	[6]	I; PU	IO	**PIO2_15 —** General-purpose digital input/output pin.
						I	**SCT1_IN3 —** SCTimer1/PWM input 3.
PIO2_16	-	-	50	[6]	I; PU	IO	**PIO2_16 —** General-purpose digital input/output pin.
						O	**SCT1_OUT0 —** SCTimer1/PWM output 0.
PIO2_17	-	-	51	[6]	I; PU	IO	**PIO2_17 —** General-purpose digital input/output pin.
						O	**SCT1_OUT1 —** SCTimer1/PWM output 1.
PIO2_18	-	33	52	[6]	I; PU	IO	**PIO2_18 —** General-purpose port 2 input/output 18.
						O	**SCT1_OUT2 —** SCTimer1/PWM output 2.
PIO2_19	-	36	57	[6]	I; PU	IO	**PIO2_19 —** General-purpose port 2 input/output 19.
						O	**SCT1_OUT3 —** SCTimer1/PWM output 3.
PIO2_20	-	-	75	[6]	I; PU	IO	**PIO2_20 —** General-purpose port 2 input/output 20.
PIO2_21	-	-	76	[6]	I; PU	IO	**PIO2_21 —** General-purpose port 2 input/output 21.
PIO2_22	-	-	77	[6]	I; PU	IO	**PIO2_22 —** General-purpose port 2 input/output 22.
PIO2_23	-	-	1	[6]	I; PU	IO	**PIO2_23 —** General-purpose port 2 input/output 23.
$\overline{\text{RSTOUT}}$	-	-	88	[6]	IA	IO	Internal reset status output.
RTCXIN	48	1	5	[2]	-	-	RTC oscillator input. This input should be grounded if the RTC is not used.
RTCXOUT	1	2	6	[2]	-	-	RTC oscillator output.
VREFP	34	47	73		-	-	ADC positive reference voltage. If the ADC is not used, tie VREFP to V_{DD}.
VREFN	35	48	74		-	-	ADC negative voltage reference. If the ADC is not used, tie VREFN to V_{SS}.
V_{DDA}	40	53	84		-	-	Analog voltage supply. V_{DDA}should typically be the same voltages as V_{DD} but should be isolated to minimize noise and error. V_{DDA} should be tied to V_{DD} if the ADC is not used.
V_{DD}	44, 8	58, 10, 34, 59	92, 14, 71, 54, 93		-	-	Supply voltage to the internal regulator and the external rail.
VBAT	47	63	99		-	-	Battery supply. Supplies power to the RTC. If no battery is used, tie VBAT to VDD.
V_{SSA}	41	54	85		-	-	Analog ground. V_{SSA}should typically be the same voltage as V_{SS} but should be isolated to minimize noise and error. V_{SSA} should be tied to V_{SS} if the ADC is not used.
V_{SS}	43, 2, 5	57, 3, 7	91, 7, 11, 53, 70		-	-	Ground.
n.c.	-	-	39				Not connected.
n.c.	-	-	38				Not connected.

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[1] Pin state at reset for default function: I = Input; O = Output; AI = Analog Input; PU = internal pull-up enabled; IA = inactive, no pull-up/down enabled;
F = floating; If the pins are not used, tie floating pins to ground or power to minimize power consumption.

[2] Special analog pad.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

[4] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as analog input, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital input glitch filter. WAKEUP pin. The wake-up pin function can be disabled and the pin can be used for other purposes if the RTC is enabled for waking up the part from Deep power-down mode.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[7] I^2C-bus pin compliant with the I^2C-bus specification for I^2C standard mode, I^2C Fast-mode, and I^2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[8] 5 V tolerant pad. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[9] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog crystal oscillator connections. When configured for the crystal oscillator input/output, digital section of the pad is disabled and the pin is not 5 V tolerant; includes digital, programmable filter.

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8. Functional description

8.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 50 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

8.2 AHB multilayer matrix

The AHB multilayer matrix supports two masters, the M0+ core and the DMA. All masters can access all slaves (peripherals and memories).

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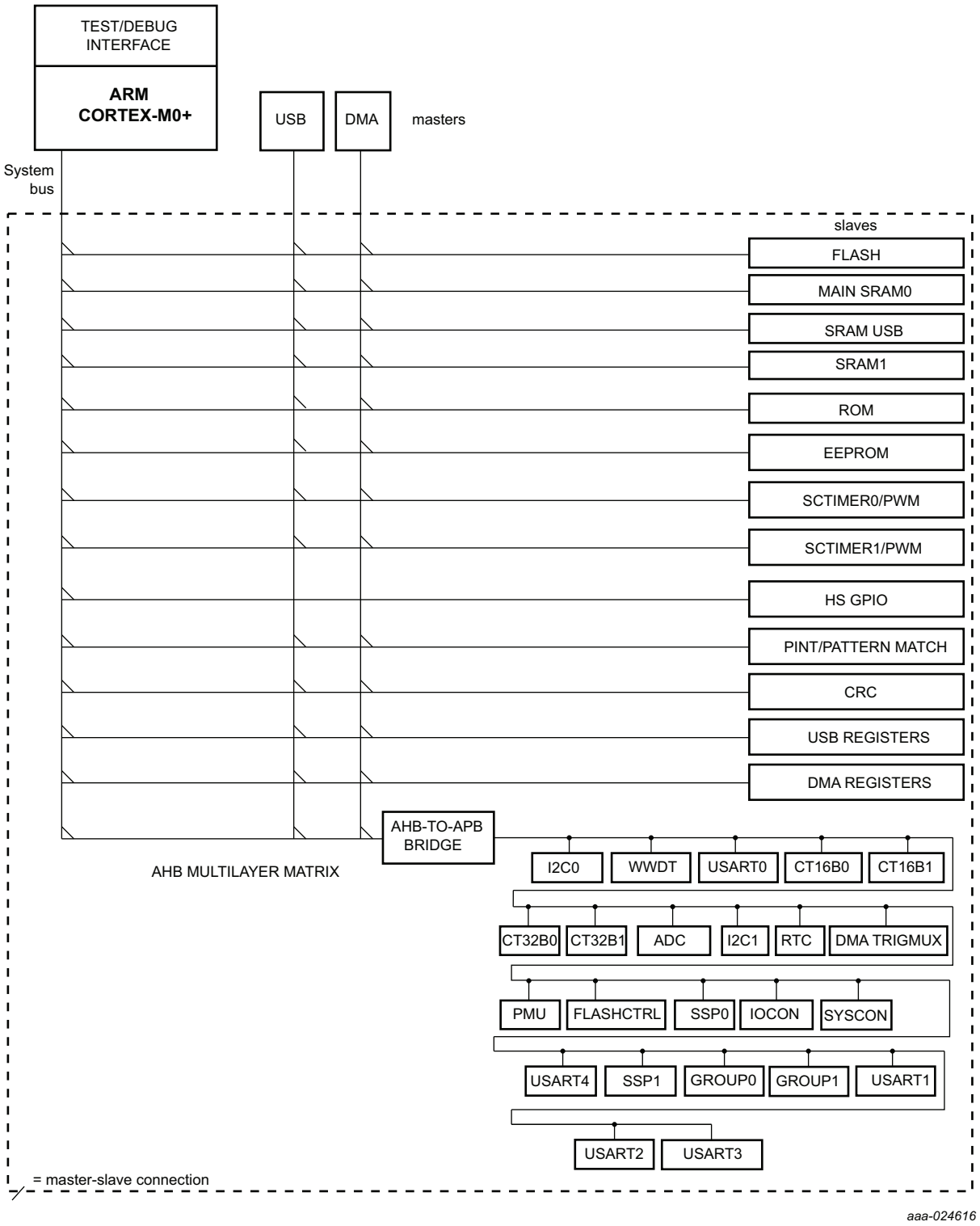


Fig 7. AHB multilayer matrix

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8.3 On-chip flash programming memory

The LPC11E6x contain up to 256 KB on-chip flash program memory. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip bootloader software.

The flash memory is divided into 24 x 4 KB and 5 x 32 KB sectors. Individual pages of 256 byte each can be erased using the IAP erase page command.

8.4 EEPROM

The LPC11E6x contain 4 KB of on-chip byte-erasable and byte-programmable EEPROM data memory. The EEPROM can be programmed using In-Application Programming (IAP) via the on-chip bootloader software.

8.5 SRAM

The LPC11E6x contain a total of up to 36 KB on-chip static RAM memory. The main SRAM block contains either 8 KB, 16 KB. or 32 KB of main SRAM0. Two additional SRAM blocks of 2 KB (SRAM1 and SRAM2) are located in separate areas of the memory map. See Figure 8.

8.6 On-chip ROM

The on-chip ROM contains the bootloader and the following Application Programming Interfaces (APIs):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash including IAP erase page command.
- IAP support for EEPROM
- Power profiles for configuring power consumption and PLL settings
- 32-bit integer division routines
- APIs to use the following peripherals:
  - I2C
  - USART0 and USART1/2/3/4
  - DMA

8.7 Memory mapping

The LPC11E6x incorporates several distinct memory regions, shown in the following figures. Figure 8 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB (Advanced High-performance Bus) peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB (Advanced Peripheral Bus) peripheral area is 512 KB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 KB of space. This addressing scheme allows simplifying the address decoding for each peripheral.

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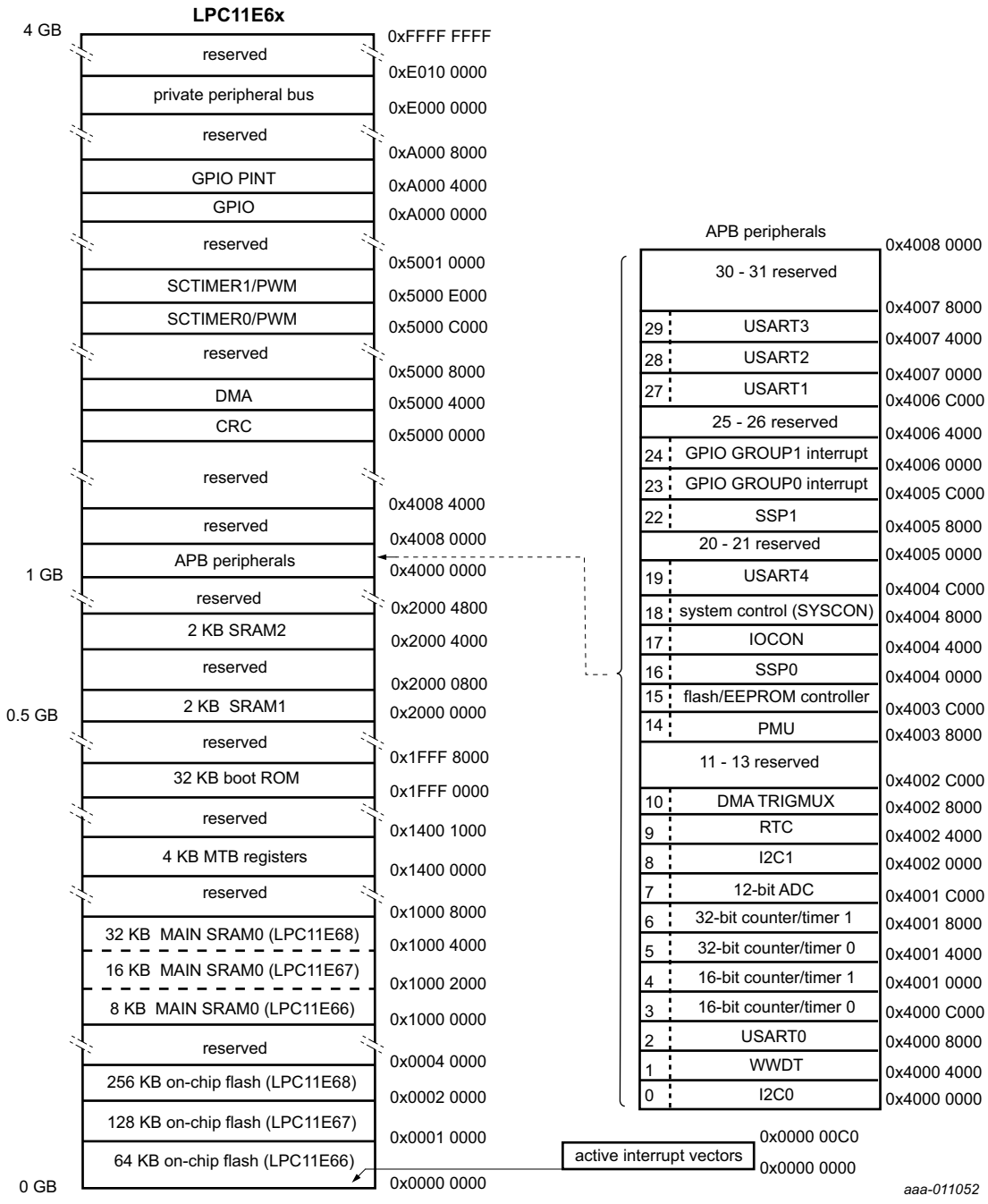


Fig 8. LPC11E6x Memory map

8.8 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

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8.8.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC11E6x, the NVIC supports vectored interrupts for each of the peripherals and the eight pin interrupts. The following peripheral interrupts are ORed to contribute to one interrupt in the NVIC:
  - USART1, USART4
  - USART2, USART3
  - SCTimer0/PWM, SCTimer1/PWM
  - BOD, WWDT
  - ADC end-of-sequence A interrupt, threshold crossing interrupt
  - ADC end-of-sequence B interrupt, overrun interrupt
  - Flash, EEPROM
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation.

8.8.2 Interrupt sources

Each peripheral device has at least one interrupt line connected to the NVIC but can have several interrupt flags. Individual interrupt flags can also represent more than one interrupt source.

8.9 IOCON block

The IOCON block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Connect peripherals to the appropriate pins before activating the peripheral and before enabling any related interrupt.

Enabling an analog function disables the digital pad. However, the internal pull-up and pull-down resistors as well as the pin hysteresis must be disabled to obtain an accurate reading of the analog input.

8.9.1 Features

- Programmable pin function.
- Programmable pull-up, pull-down, or repeater mode.
- All pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled.
- Programmable pseudo open-drain mode.
- Programmable (on/off) 10 ns glitch filter on pins PIO0_22, PIO0_23, PIO0_11 to PIO0_16, PIO1_3, PIO1_9, PIO1_22, and PIO1_29. The glitch filter is turned on by default.
- Programmable hysteresis.
- Programmable input inverter.

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- Digital filter with programmable filter constant on all pins. The minimum filter constant is 1/50 MHz = 20 ns.

8.9.2 Standard I/O pad configuration

Figure 9 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input digital filter selectable on all pins. In addition, a 10 ns digital glitch filter is selectable on pins with analog function.
- Analog input

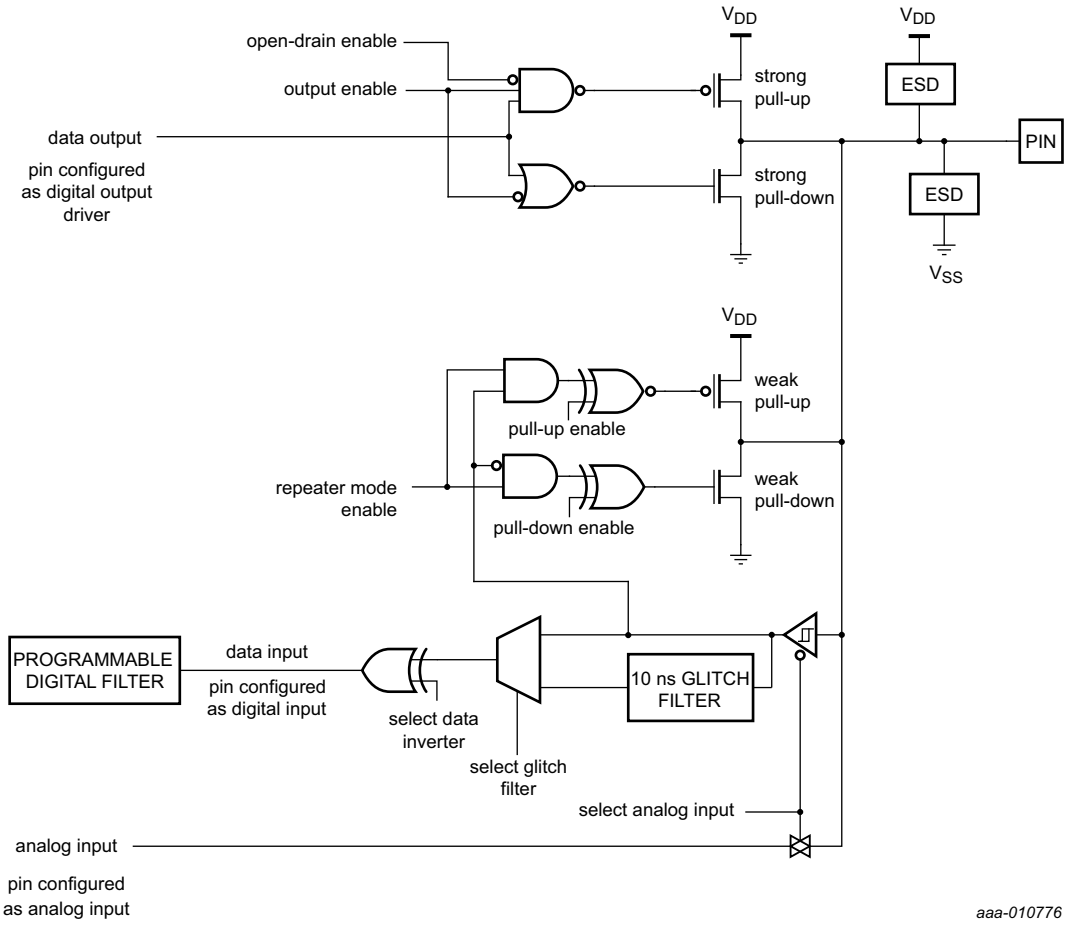


Fig 9. Standard I/O pin configuration

8.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

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LPC11E6x use accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ IO bus for fastest possible single-cycle I/O timing, allowing GPIO toggling with rates of up to 25 MHz.
- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

8.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.

8.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin except pins PIO2_8 and PIO2_23 can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are on the IO+ bus for fast single-cycle access.

8.11.1 Features

- Pin interrupts
  - Up to eight pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH- or LOW-active.
  - Pin interrupts can wake up the part from sleep mode, deep-sleep mode, and power-down mode.
- Pin interrupt pattern match engine
  - Up to 8 pins can be selected from all digital pins except pins PIO2_8 and PIO2_23 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can be programmed to generate an RXEV notification to the ARM CPU as well.
  - The pattern match engine does not facilitate wake-up.

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8.12 GPIO group interrupts

The GPIO pins can be used in several ways to set pins as inputs or outputs and use the inputs as combinations of level and edge sensitive interrupts. For each port/pin connected to one of the two the GPIO Grouped Interrupt blocks (GINT0 and GINT1), the GPIO grouped interrupt registers determine which pins are enabled to generate interrupts and the active polarities of each of those inputs.

The GPIO grouped interrupt registers also select whether the interrupt output is level or edge triggered and whether it is based on the OR or the AND of all of the enabled inputs.

When the designated pattern is detected on the selected input pins, the GPIO grouped interrupt block generates an interrupt. If the part is in a power-savings mode, it first asynchronously wakes up the part prior to asserting the interrupt request. The interrupt request line can be cleared by writing a one to the interrupt status bit in the control register.

8.12.1 Features

- Two group interrupts are supported to reflect two distinct interrupt patterns.
- The inputs from any number of digital pins can be enabled to contribute to a combined group interrupt.
- The polarity of each input enabled for the group interrupt can be configured HIGH or LOW.
- Enabled interrupts can be logically combined through an OR or AND operation.
- The grouped interrupts can wake up the part from sleep, deep-sleep or power-down modes.

8.13 DMA controller

The DMA controller can access all memories and the USART and SSP peripherals using DMA requests. DMA transfers can also be triggered by internal events like the ADC interrupts, timer match outputs, the pin interrupts (PINT0 and PINT1) and the SCTimer DMA requests.

8.13.1 Features

- 16 channels with 14 channels connected to peripheral request inputs.
- DMA operations can be triggered by on-chip events or two of the pin interrupts. Each DMA channel can select one trigger input from 12 sources.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache with two entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

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8.14 USART0

Remark: The LPC11E6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11E1x/3x parts. USART1 to USART4 use a different register interface.

The USART0 includes full modem control, support for synchronous mode, and a smart card interface. The RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The USART0 uses a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

8.14.1 Features

- Maximum USART0 data bit rate of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.
- 16 byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.
- Support for synchronous mode.
- Includes smart card interface.
- DMA support.

8.15 USART1/2/3/4

Remark: The LPC11E6x contains two distinctive types of UART interfaces: USART0 is software-compatible with the USART interface on the LPC11E1x/LPC11E3x parts. USART1 to USART4 use a different register interface to achieve the same UART functionality except for modem and smart card control.

Remark: USART4 IS available only on part LPC11E68JBD100.

Interrupts generated by the USART1/2/3/4 peripherals can wake up the part from Deep-sleep and power-down modes if the USART is in synchronous mode, the 32 kHz mode is enabled, or the CTS interrupt is enabled. This wake-up mechanism is not available with the USART0 peripheral.

8.15.1 Features

- Maximum bit rates of 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode.
- 7, 8, or 9 data bits and 1 or 2 stop bits

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- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software-address compare feature. (RS-485 possible with software address detection and transceiver direction control.)
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep and power-down modes.
- Special operating mode allows operation at up to 9600 baud using the 32 kHz RTC oscillator as the UART clock. This mode can be used while the device is in Deep-sleep or Power-down mode and can wake up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

8.16 SSP serial I/O controller (SSP0/1)

The SSP controllers operate on an SSP, 4-wire SSI, or Microwire bus. The controller can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one direction carries meaningful data.

8.16.1 Features

- Maximum SSP speed of 25 Mbit/s (master) or 4.17 Mbit/s (slave) (in SSP mode)
- Compatible with Motorola SPI (Serial Peripheral Interface), 4-wire Texas Instruments SSI (Serial Synchronous Interface), and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive

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- 4-bit to 16-bit frame
- DMA support

8.17 I²C-bus serial I/O controller

The LPC11E6x contain two I²C-bus controllers.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

8.17.1 Features

- One I²C-interface (I2C0) is an I²C-bus compliant interface with open-drain pins. The I²C-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- One I²C-interface (I2C1) uses standard digital pins. The I²C-bus interface supports bit rates up to 400 kbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

8.18 Timer/PWM subsystem

Four standard timers and two state configurable timers can be combined to create multiple PWM outputs using the match outputs and the match registers for each timer. Each timer can create multiple PWM outputs with its own time base.

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Table 4. PWM resources

PWM outputs			Peripheral	Pin functions available for PWM			Match registers used
LQFP100	LQFP64	LQFP48		LQFP100	LQFP64	LQFP48	
3	3	3	CT16B0	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	CT16B0_MAT0, CT16B0_MAT1, CT16B0_MAT2	4
2	2	2	CT16B1	CT16B1_MAT0, CT16B1_MAT1	CT16B1_MAT0, CT16B1_MAT1	CT16B1_MAT0, CT16B1_MAT1	3
3	3	3	CT32B0	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	three of CT32B0_MAT0, CT32B0_MAT1, CT32B0_MAT2, CT32B0_MAT3	4
3	3	3	CT32B1	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	three of CT32B1_MAT0, CT32B1_MAT1, CT32B1_MAT2, CT32B1_MAT3	4
4	4	3	SCTIMER0/ PWM	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT0, SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	SCT0_OUT1, SCT0_OUT2, SCT0_OUT3	up to 5
4	2	-	SCTIMER1/ PWM	SCT1_OUT0, SCT1_OUT1, SCT1_OUT2, SCT1_OUT3	SCT1_OUT2, SCT1_OUT3	-	up to 5

The standard timers and the SCTimers combine to up to eight independent timers. Each SCTimer can be configured either as one 32-bit timer or two independently counting 16-bit timers which use the same input clock. The following combinations are possible:

Table 5. Timer configurations

32-bit timers	Resources	16-bit timers	Resources
4	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer, SCTimer1/PWM as 32-bit timer	2	CT16B0, CT16B1
2	CT32B0, CT32B1	6	CT16B0, CT16B1, SCTimer0/PWM as two 16-bit timers, SCTimer1/PWM as two 16-bit timers
3	CT32B0, CT32B1, SCTimer0/PWM as 32-bit timer (or SCTimer1/PWM as 32-bit timer)	4	CT16B0, CT16B1, SCTimer1/PWM as two 16-bit timers (or SCTimer0/PWM as two 16-bit timers)

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8.18.1 State Configurable Timers (SCTimer0/PWM and SCTimer1/PWM)

The state configurable timer can create timed output signals such as PWM outputs triggered by programmable events. Combinations of events can be used to define timer states. The SCTimer/PWM can control the timer operations, capture inputs, change states, and toggle outputs triggered only by events entirely without CPU intervention.

If multiple states are not implemented, the SCTimer/PWM simply operates as one 32-bit or two 16-bit timers with match, capture, and PWM functions.

8.18.1.1 Features

- Each SCTimer/PWM supports:
  - 5 match/capture registers.
  - 6 events.
  - 8 states.
  - 4 inputs and 4 outputs.
- Counter/timer features:
  - Each SCTimer is configurable as two 16-bit counters or one 32-bit counter.
  - Counters can be clocked by the system clock or selected input.
  - Configurable as up counters or up-down counters.
  - Configurable number of match and capture registers. Up to five match and capture registers total.
  - Upon match create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.
- PWM features:
  - Counters can be used with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to four single-edge or dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as a rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.

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- Each event can be assigned to one or more states.
- State variable allows sequencing across multiple counter cycles.

- SCTimer match outputs (ORed with the general-purpose timer match outputs) serve as ADC hardware trigger inputs.

8.18.2 General purpose external event counter/timers (CT32B0/1 and CT16B0/1)

The LPC11E6x includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

8.18.2.1 Features

- A 32-bit/16-bit timer/counter with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- PWM output function.
- Match outputs and capture inputs serve as hardware triggers for ADC conversions.

8.19 System tick timer (SysTick)

The ARM Cortex-M0+ includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval (typically 10 ms).

8.20 Windowed WatchDog Timer (WWDT)

The purpose of the WWDT is to prevent an unresponsive system state. If software fails to update the watchdog within a programmable time window, the watchdog resets the microcontroller

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8.20.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time before watchdog time-out.
- Software enables the WWDT, but a hardware reset or a watchdog reset/interrupt is required to disable the WWDT.
- Incorrect feed sequence causes reset or interrupt, if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The WatchDog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDOsc). The clock source selection provides a wide range of potential timing choices of watchdog operation under different power conditions.

8.21 Real-Time Clock (RTC)

The RTC resides in a separate always-on voltage domain with battery back-up. The RTC uses an independent oscillator, also located in the always-on voltage domain.

8.21.1 Features

- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low-power modes, including Deep power-down.

8.22 Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12 bit and fast conversion rates of up to 2 MSamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the counter/timer match outputs and capture inputs and the ARM TXEV.

The ADC includes a hardware threshold compare function with zero-crossing detection.

8.22.1 Features

- 12-bit successive approximation analog to digital converter.
- 12-bit conversion rate of up to 2 MSamples/s.
- Temperature sensor voltage output selectable as internal voltage source for channel 0.
- Two configurable conversion sequences with independent triggers.

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- Optional automatic high/low threshold comparison and zero-crossing detection.
- Power-down mode and low-power operating mode.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed V_{DDA} voltage level).
- Burst conversion mode for single or multiple inputs.

8.23 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C) for typical samples. The temperature sensor is approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up and after switching the input channels of the ADC, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

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8.24 Clocking and power control

8.24.1 Clock generation

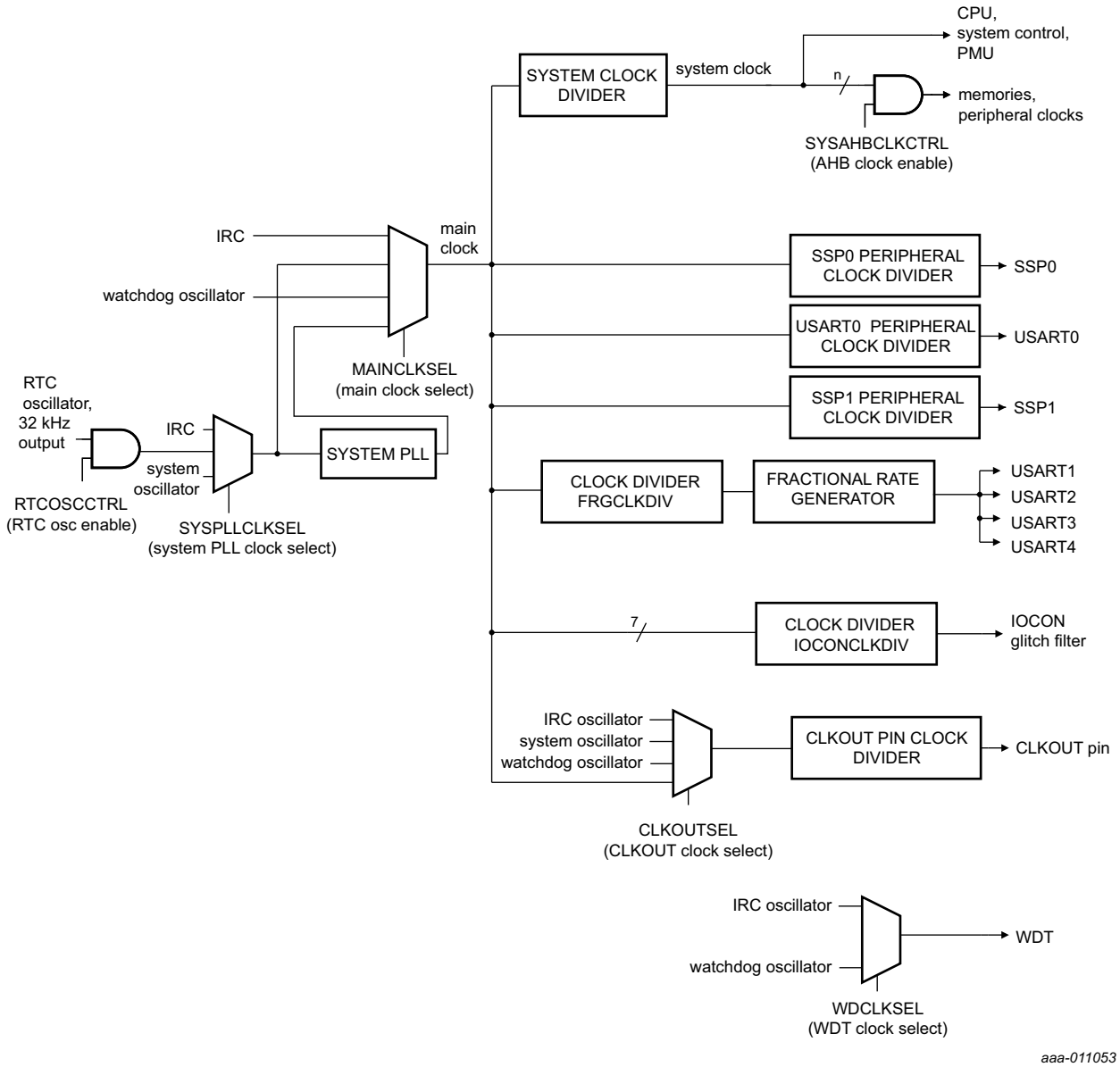


Fig 10. Clock generation

8.24.2 Power domains

The LPC11E6x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

The VBAT pin supplies power only to the RTC domain. The RTC requires a minimum of power to operate, which can be supplied by an external battery. The device core power (V_{DD}) is used to operate the RTC whenever V_{DD} is present. Therefore, there is no power drain from the RTC battery when V_{DD} is available and $V_{DD} \geq$ VBAT + 0.3 V.

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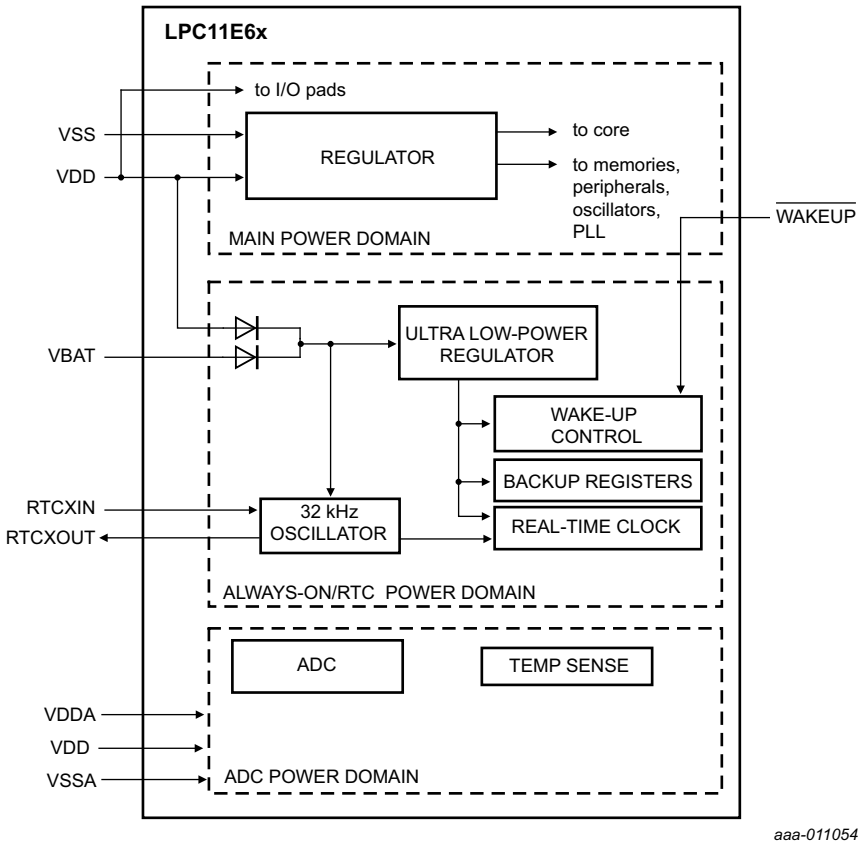


Fig 11. Power distribution

8.24.3 Integrated oscillators

The LPC11E6x include the following independent oscillators: the system oscillator, the Internal RC oscillator (IRC), the watchdog oscillator, and the 32 kHz RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC11E6x operates from the internal RC oscillator until software switches to a different clock source. The IRC allows the system to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 10 for an overview of the LPC11E6x clock generation.

8.24.3.1 Internal RC oscillator

The IRC can be used as the clock source for the WDT or as the clock that drives the system PLL and then the CPU. The nominal IRC frequency is 12 MHz.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC11E6x use the IRC as the clock source. Software can later switch to one of the other available clock sources.

8.24.3.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL.

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The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

The system oscillator has a wake-up time of approximately 500 µs.

8.24.3.3 WatchDog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 14).

8.24.3.4 RTC oscillator

The low-power RTC oscillator provides a 1 Hz clock and a 1 kHz clock to the RTC and a 32 kHz clock output that can be used to obtain the main clock (see Figure 10).

8.24.4 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. To support this frequency range, an additional divider keeps the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. Software can enable the PLL later. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 µs.

8.24.5 Clock output

The LPC11E6x feature a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

8.24.6 Wake-up process

The LPC11E6x begin operation by using the 12 MHz IRC oscillator as the clock source at power-up and when awakened from Deep power-down mode. This mechanism allows chip operation to resume quickly. If the application uses the main oscillator or the PLL, software must enable these components and wait for them to stabilize. Only then can the system use the PLL and main oscillator as a clock source.

8.24.7 Power control

The LPC11E6x support various power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate can also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This power control mechanism allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals. This register allows fine-tuning of power

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consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

8.24.7.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC11E6x for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

8.24.7.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and can generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, by memory systems and related controllers, and by internal buses.

8.24.7.3 Deep-sleep mode

In Deep-sleep mode, the LPC11E6x is in Sleep mode and all peripheral clocks and all clock sources are off except for the IRC. The IRC output is disabled unless the IRC is selected as input to the watchdog timer. In addition, all analog blocks are shut down and the flash is in standby mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC11E6x can wake up from Deep-sleep mode via reset, selected GPIO pins, a watchdog timer interrupt, an RTC interrupt, or any interrupts that the USART1 to USART4 interfaces can create in Deep-sleep mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Deep-sleep mode saves power and allows for short wake-up times.

8.24.7.4 Power-down mode

In Power-down mode, the LPC11E6x is in Sleep mode and all peripheral clocks and all clock sources are off except for watchdog oscillator if selected. In addition, all analog blocks and the flash are shut down. In Power-down mode, the application can keep the BOD circuit running for BOD protection.

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The LPC11E6x can wake up from Power-down mode via reset, selected GPIO pins, a watchdog timer interrupt, an RTC interrupt, or any interrupts that the USART1 to USART4 interfaces can create in Power-down mode. The USART wake-up requires the 32 kHz mode, the synchronous mode, or the CTS interrupt to be set up.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

8.24.7.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the always-on RTC power domain. The LPC11E6x can wake up from Deep power-down mode via the WAKEUP pin or a wake-up signal generated by the RTC interrupt.

The LPC11E6x can be blocked from entering Deep power-down mode by setting a lock bit in the PMU block. Blocking the Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

If the WAKEUP pin is used in the application, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH while the part is in deep power-down mode. To wake up from deep power-down mode, pull the WAKEUP pin LOW. In addition, pull the $\overline{\text{RESET}}$ pin HIGH to prevent it from floating while in Deep power-down mode.

8.25 System control

8.25.1 Reset

Reset has four sources on the LPC11E6x: the $\overline{\text{RESET}}$ pin, the WatchDog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values. The internal reset status is reflected on the $\overline{\text{RSTOUT}}$ pin.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

The $\overline{\text{RESET}}$ pin is operational in active, sleep, deep-sleep, and power-down modes if the $\overline{\text{RESET}}$ function is selected in the IOCON register for pin PIO0_0 (this is the default). A LOW-going pulse as short as 50 ns executes the reset and also wakes up the part if in sleep, deep-sleep or power-down mode. The $\overline{\text{RESET}}$ pin is not functional in Deep power-down mode.

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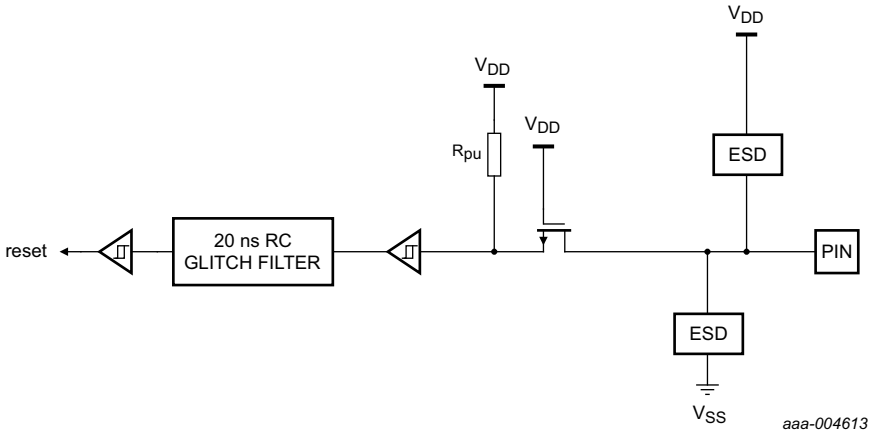


Fig 12. $\overline{\text{RESET}}$ pin configuration

8.25.2 Brownout detection

The LPC11E6x includes two levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels can be selected to cause a forced reset of the chip.

8.25.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC11U6x/E6x user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

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CAUTION



If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC11U6x/Ex user manual*.

8.26 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}}$ = LOW) and the ARM SWD debug ($\overline{\text{RESET}}$ = HIGH). The ARM SWD debug port is disabled while the LPC11E6x is in reset.

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs.
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

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9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[2]	−0.5	4.6	V
V_{DDA}	analog supply voltage			−0.5	4.6	V
V_{ref}	reference voltage	on pin VREFP		−0.5	4.6	V
V_{BAT}	battery supply voltage			−0.5	4.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the $V_{DD(IO)}$ supply voltage is present	[3][4]	−0.5	+5.5	V
		on open-drain I2C-bus pins PIO0_4 and PIO0_5	[5]	−0.5	+5.5	V
V_{IA}	analog input voltage		[6] [7]	−0.5	4.6	V
$V_{i(xtal)}$	crystal input voltage	pins configured for XTALIN and XTALOUT	[2]	−0.5	+2.5	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage		[2]	−0.5	4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5\ V_{DD(IO)}) < V_I < (1.5\ V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[8]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model; all pins	[9]	-	3	kV

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 8) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] Applies to all 5 V tolerant I/O pins except true open-drain pins PIO0_4 and PIO0_5.

[4] Including the voltage on outputs in 3-state mode.

[5] $V_{DD(IO)}$ present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when $V_{DD(IO)}$ is powered down.

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[6] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[8] Dependent on package type.

[9] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

10. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 7. Thermal resistance value (C/W): ±15 %

Symbol	Parameter	Conditions	Typ	Unit
LQFP48				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	67	°C/W
		1 m/s	58	°C/W
		2.5 m/s	53	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	100	°C/W
		1 m/s	79	°C/W
		2.5 m/s	71	°C/W
θjc	thermal resistance junction-to-case		15	°C/W
θjb	thermal resistance junction-to-board		19	°C/W
LQFP64				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	58	°C/W
		1 m/s	51	°C/W
		2.5 m/s	47	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	81	°C/W
		1 m/s	66	°C/W
		2.5 m/s	60	°C/W

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Table 7. Thermal resistance value (C/W): ±15 %

Symbol	Parameter	Conditions	Typ	Unit
θjc	thermal resistance junction-to-case		18	°C/W
θjb	thermal resistance junction-to-board		23	°C/W
LQFP100				
θja	thermal resistance junction-to-ambient			
		JEDEC (4.5 in × 4 in)		
		0 m/s	49	°C/W
		1 m/s	44	°C/W
		2.5 m/s	41	°C/W
		8-layer (4.5 in × 3 in)		
		0 m/s	66	°C/W
		1 m/s	55	°C/W
		2.5 m/s	51	°C/W
θjc	thermal resistance junction-to-case		18	°C/W
θjb	thermal resistance junction-to-board		24	°C/W

11. Static characteristics

Table 8. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			2.4	3.3	3.6	V
V_{DDA}	analog supply voltage			2.4	3.3	3.6	V
V_{ref}	reference voltage	on pin VREFP		2.4	-	V_{DDA}	V
V_{BAT}	battery supply voltage			2.4	3.3	3.6	V
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	2.3	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4][6][7]	-	1.5	-	mA
		system clock = 50 MHz; default mode; V_{DD} = 3.3 V	[2][3][6][7][9]	-	7.8	-	mA
		system clock = 50 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][6][7][9]	-	6.4	-	mA

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Table 8. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{DD}	supply current	Sleep mode;					
		system clock = 12 MHz; default mode; V_{DD} = 3.3 V	[2][3][4] [6][7]	-	1.2	-	mA
		system clock = 12 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][4] [6][7]	-	0.8	-	mA
		system clock = 50 MHz; default mode; V_{DD} = 3.3 V	[2][3][9] [6][7]	-	3.3	-	mA
		system clock = 50 MHz; low-current mode; V_{DD} = 3.3 V	[2][3][9] [6][7]	-	2.8	-	mA
I_{DD}	supply current	Deep-sleep mode; V_{DD} = 3.3 V; T_{amb} = 25 °C	[2][3][10]	-	275	350	µA
		T_{amb} = 105 °C		-	-	640	µA
I_{DD}	supply current	Power-down mode; V_{DD} = 3.3 V T_{amb} = 25 °C	[2][3][10]	-	5	22	µA
		T_{amb} = 105 °C		-	-	130	µA
I_{DD}	supply current	Deep power-down mode; V_{DD} = 3.3 V; VBAT = 0 or VBAT = 3.0 V RTC oscillator running T_{amb} = 25 °C	[2][11]	-	1.2	5	µA
		T_{amb} = 105 °C		-	-	14	
		RTC oscillator input grounded	[2][11]	-	550	-	nA
I_{BAT}	battery supply current	Deep power-down mode; V_{DD} = V_{DDA} = 3.3 V; VBAT = 3.0 V; RTC oscillator running		-	0	-	-
		RTC off		-	0	-	-
I_{BAT}	battery supply current	V_{DD} = V_{DDA} = 0 V; VBAT = 3.0 V RTC oscillator running		-	1.2	-	µA
Standard port pins configured as digital pins, $\overline{\text{RESET}}$; see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	V_{DD} ≥ 2.4 V; 5 V tolerant pins	[13] [14]	0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V

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Table 8. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V;		4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V; 2.4 V ≤ V_{DD} ≤ 3.6 V		−10	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
High-drive output pins configured as digital pin (PIO0_7 and PIO1_31); see Figure 13							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	V_{DD} ≥ 2.4 V	[13] [14]	0	-	5	V
		V_{DD} = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 12 mA; 2.4 V ≤ V_{DD} < 2.5 V		V_{DD} − 0.4	-	-	V
		I_{OH} = 20 mA; 2.5 V ≤ V_{DD} < 3.6 V		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 2.4 V ≤ V_{DD} < 2.5 V		12	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.5 V ≤ V_{DD} < 3.6 V		20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[15]	-	-	45	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[15]	-	-	50	mA

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Table 8. Static characteristics *...continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pd}	pull-down current	V_I = 5 V	[16]	10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[16]	−10	−50	−85	µA
		$V_{DD} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 13							
V_{IH}	HIGH-level input voltage			0.7 V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3 V_{DD}	V
V_{hys}	hysteresis voltage			0.05 V_{DD}	-	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins		3.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins		20	-	-	mA
I_{LI}	input leakage current	$V_I = V_{DD}$	[17]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V
$V_{i(rtcx)}$	32 kHz oscillator input voltage	on pin RTCXIN	[19]	−0.5	-	3.6	V
$V_{o(rtcx)}$	32 kHz oscillator output voltage	on pin RTCXOUT	[19]	−0.5	-	3.6	V
Pin capacitance							
C_{io}	input/output capacitance	pins with analog and digital functions	[20]	-	-	7.1	pF
		I^2C-bus pins (PIO0_4 and PIO0_5)	[20]	-	-	2.5	pF
		pins with digital functions only	[20]	-	-	2.8	pF

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC enabled; system oscillator disabled; system PLL enabled.

[9] IRC disabled; system oscillator enabled; system PLL enabled.

[10] All oscillators and analog blocks turned off.

[11] WAKEUP pin pulled HIGH externally.

[12] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[13] Including voltage on outputs in tri-state mode.

[14] Tri-state outputs go into tri-state mode in Deep power-down mode.

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[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] Pull-up and pull-down currents are measured across the weak internal pull-up/pull-down resistors. See Figure 13.

[17] To V_{SS}.

[18] The parameter values specified are simulated and absolute values.

[19] The input voltage of the RTC oscillator is limited as follows: $V_{i(rtcx)}$, $V_{o(rtcx)}$ < max(VBAT, V_{DD}).

[20] Including bonding pad capacitance.

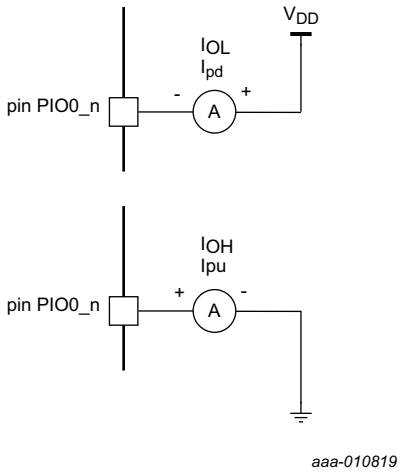


Fig 13. Pin input/output current measurement

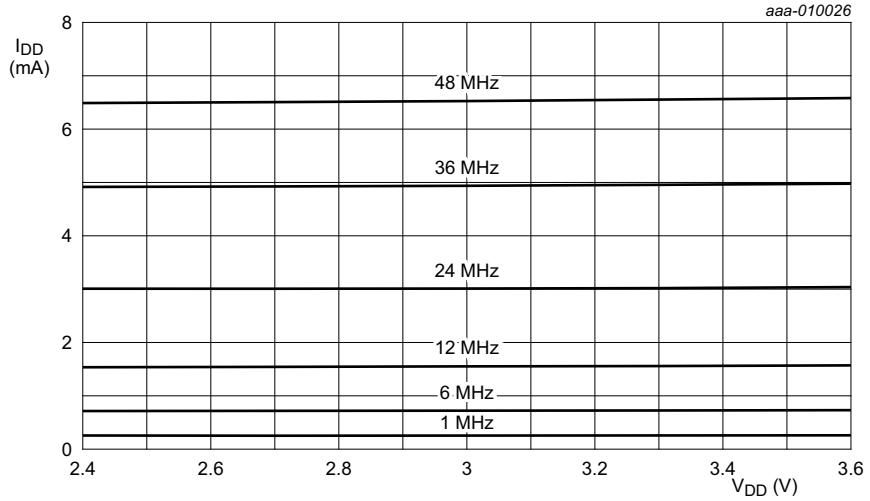
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11.1 Power consumption

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.



Conditions: T_{amb} = 25 °C; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F), all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

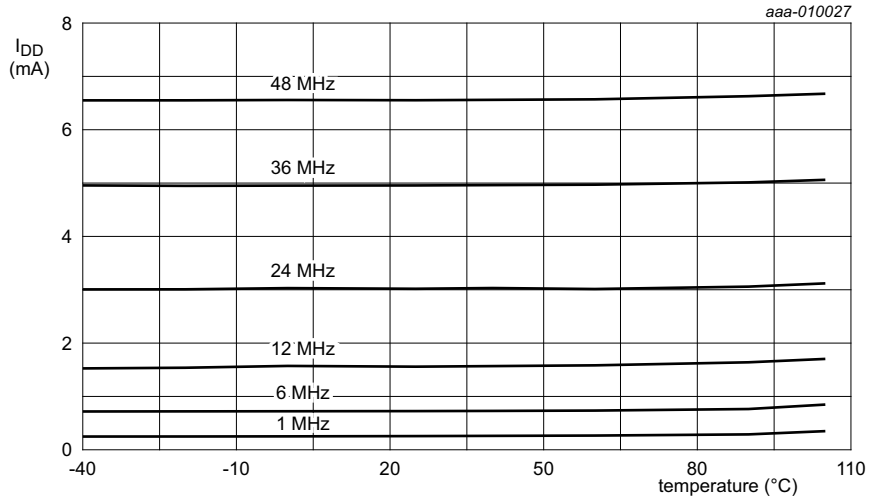
12 MHz: IRC enabled; PLL disabled.

24 MHz to 50 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 14. Active mode: Typical supply current I_{DD} versus supply voltage V_{DD}

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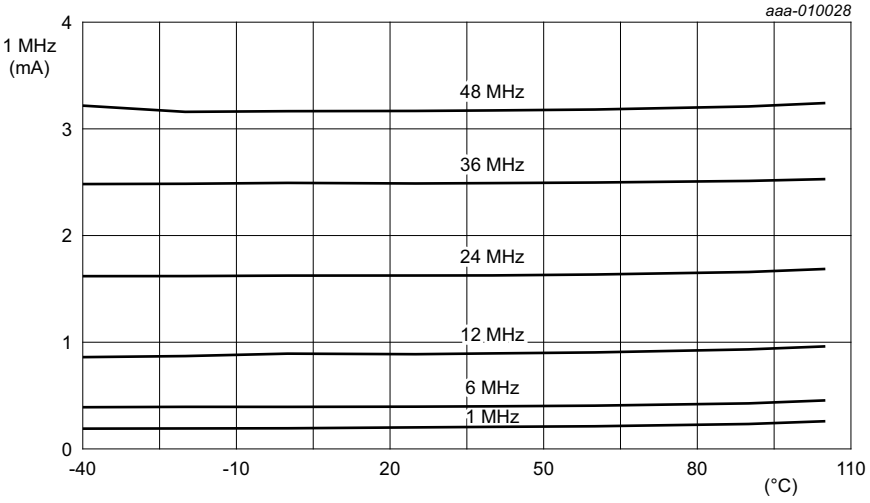
Conditions: V_{DD} = 3.3 V; active mode entered executing code `while(1){}` from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F; all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

12 MHz: IRC enabled; PLL disabled.

24 MHz to 50 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 15. Active mode: Typical supply current I_{DD} versus temperature



Conditions: V_{DD} = 3.3 V; sleep mode entered from flash; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F) all peripheral clocks disabled; internal pull-up resistors disabled; BOD disabled; low-current mode.

1 MHz - 6 MHz: IRC enabled; PLL disabled.

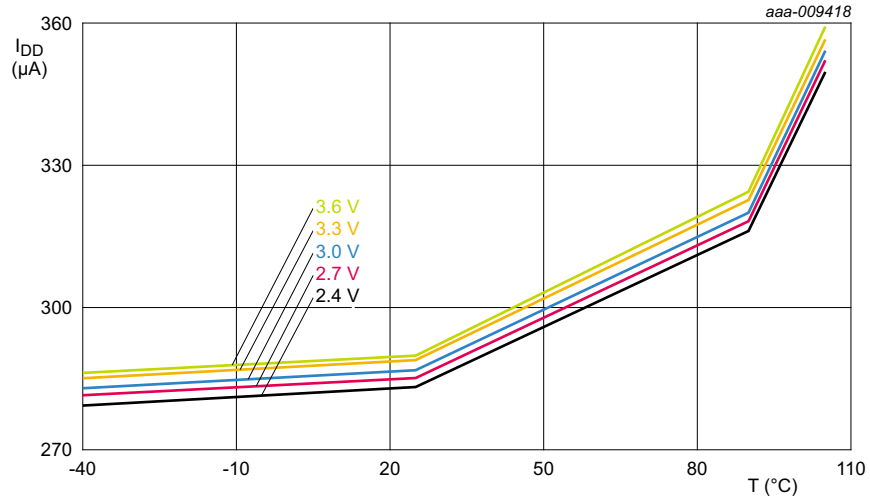
12 MHz: IRC enabled; PLL disabled.

24 MHz to 48 MHz: IRC disabled; PLL enabled; sysosc enabled.

Fig 16. Sleep mode: Typical supply current I_{DD} versus temperature for different system clock frequencies

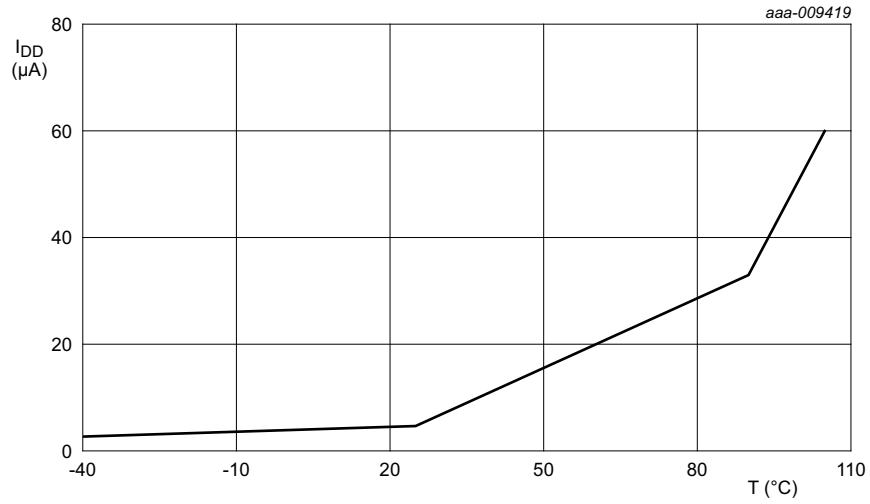
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Conditions: BOD disabled; all oscillators and analog blocks disabled

Fig 17. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

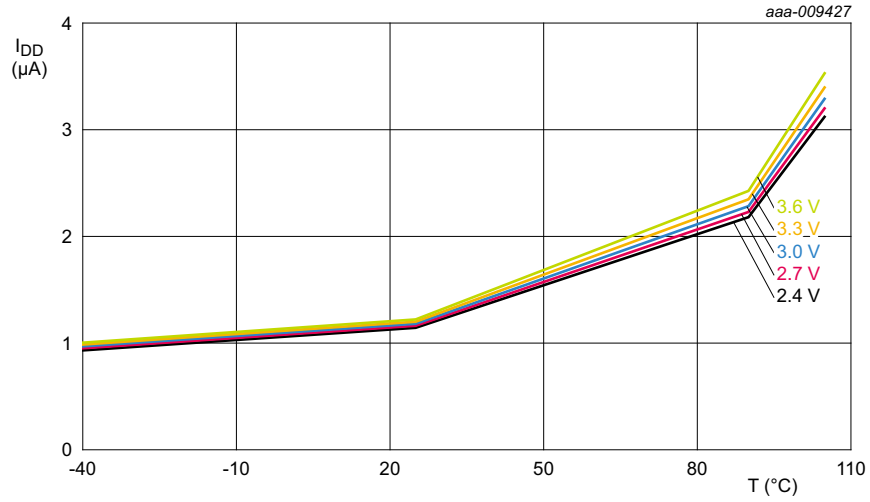


Conditions: BOD disabled; all oscillators and analog blocks disabled; V_{DD} = 2.4 V to 3.6 V.

Fig 18. Power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

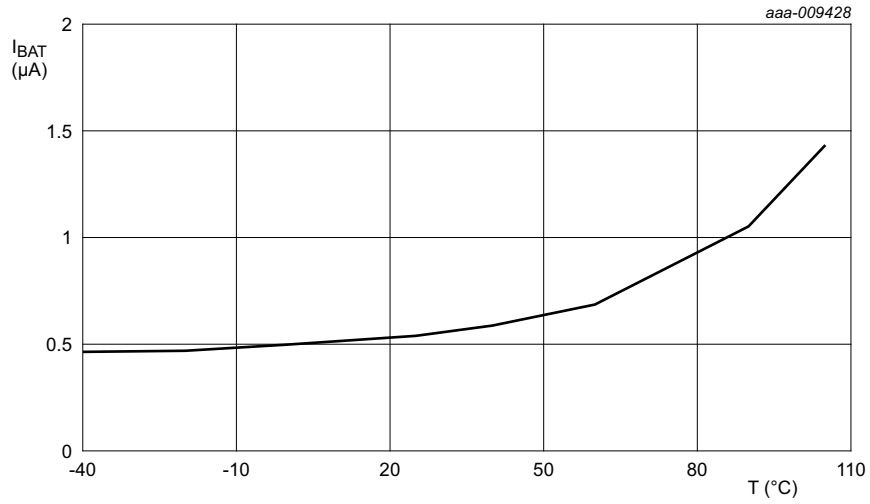
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Conditions: RTC running; VBAT = 0 V

Fig 19. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



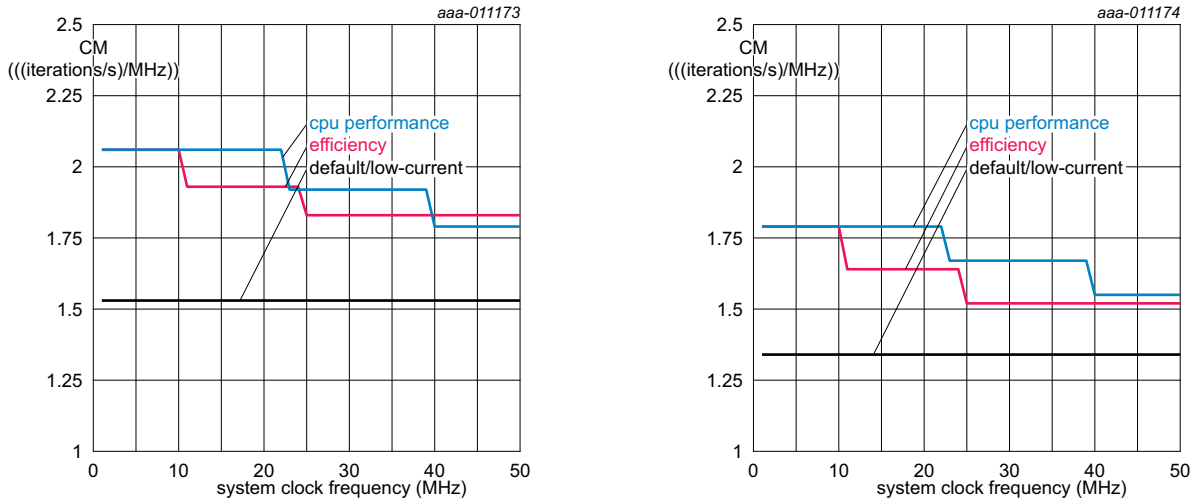
Conditions: RTC not running; V_{BAT} = 3.0 V; V_{DD} floating.

Fig 20. Deep power-down mode: Typical battery supply current I_{BAT} versus temperature

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11.2 CoreMark data

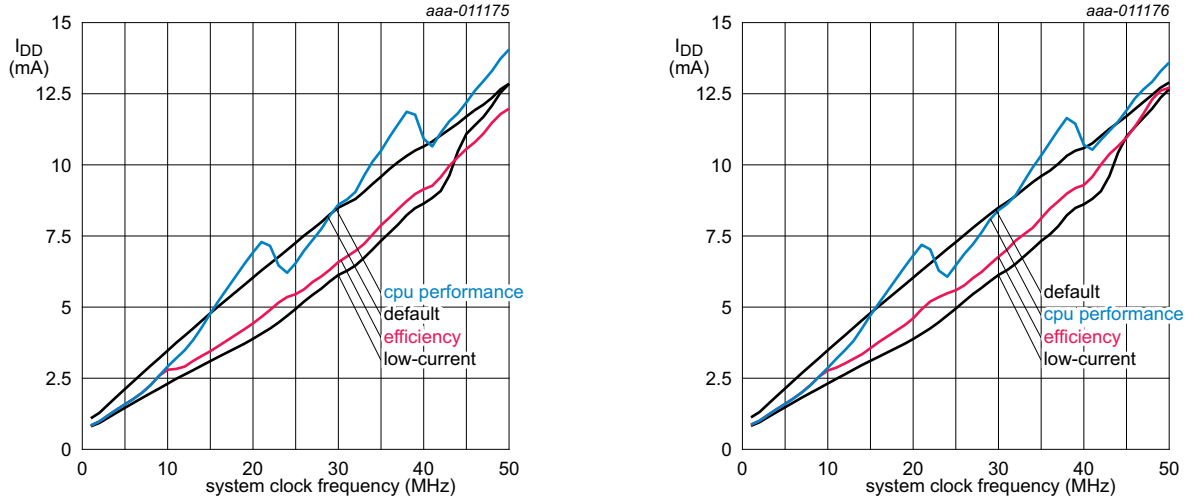


Measured with Keil uVision v.4.72.

Measured with Keil uVision v.4.60.

Conditions: Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCTimer disabled in the SYSAHBCLKCTRL register; internal pull-up resistors enabled; BOD disabled.

Fig 21. CoreMark score for different power mode settings of the power profiles



Measured with Keil uVision v.4.72.

Measured with Keil uVision v.4.60.

Conditions: Conditions: V_{DD} = 3.3 V; active mode; all peripherals except one UART and the SCTimer disabled in the SYSAHBCLKCTRL register; internal pull-up resistors enabled; BOD disabled.

Fig 22. Active mode: CoreMark power consumption I_{DD} for different power mode settings of the power profiles

The CoreMark scores serve as a guideline to select the best power mode for a given application. To find the most suitable power mode, run the application in mode and compare power consumption and performance.

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The power profiles optimize the chip performance for power consumption or core efficiency by controlling the flash access and core power. As shown in Figure 21 and Figure 22, different power modes result in different CoreMark scores reflecting the trade-off of efficiency and power consumption. In CPU and efficiency modes, the power profiles aim to keep the core efficiency at a maximum for the given system frequency. Depending on optimal flash access parameters that change with frequency, the CoreMark score and also the power consumption change. Since the compiled code for CoreMark testing runs out of flash memory, the CoreMark score depends on the compiler version.

11.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code accessing the peripheral is executed except for the ADC. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

Table 9. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.24	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.28	-	-	IRC running; PLL off; independent of main clock frequency.
WatchDog oscillator at 600 kHz/2	0	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.05	-	-	Independent of main clock frequency.
System PLL	0.25	-	-	-
CLKOUT	-	0.25	0.89	System PLL is source of CLKOUT.
ROM	-	0.09	0.37	-
FLASHREG	-	0.17	0.66	-
FLASHARRAY	-	0.13	0.52	-
SRAM1	-	0.15	0.59	-
SRAM2	-	0.14	0.56	-
GPIO + pin interrupt/pattern match	-	0.18	0.69	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCON	-	0.08	0.30	-
SCTimer0/PWM + SCTimer1/PWM	-	0.29	1.1	-
CT16B0	-	0.05	0.17	-
CT16B1	-	0.04	0.16	-
CT32B0	-	0.04	0.13	-
CT32B1	-	0.03	0.13	-
RTC	-	0.02	0.10	-

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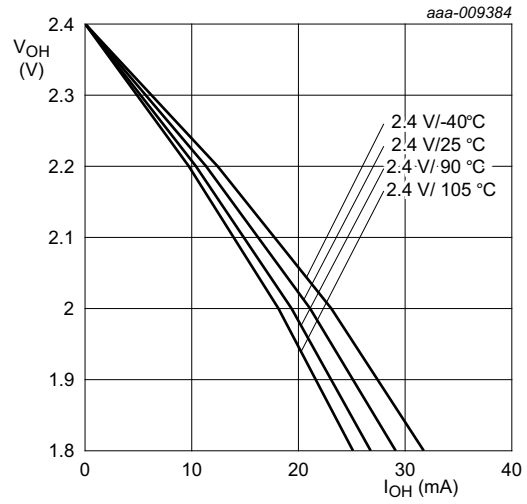
Table 9. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
WWDT	-	0.05	0.17	Main clock selected as clock source for the WDT.
I2C0	-	0.05	0.22	-
I2C1	-	0.05	0.18	-
SSP0	-	0.15	0.59	-
SSP1	-	0.15	0.58	-
USART0	-	0.31	1.19	-
USART1	-	0.12	0.50	-
USART2	-	0.13	0.49	-
USART3 + USART4	-	0.21	0.81	-
ADC0	-	2.15	2.68	Register interface disabled in SYSAHBCLKCTRL and analog block disabled in PDRUNCFG registers. Power consumption measured while the ADC is sampling a single channel with an ADC clock of 12 MHz or 48 MHz.
Temperature sensor	0.18	-	-	-
DMA	-	0.28	1.1	-
CRC	-	0.04	0.14	-

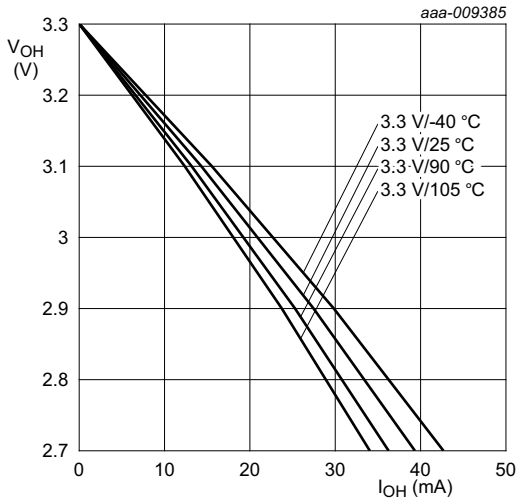
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11.4 Electrical pin characteristics

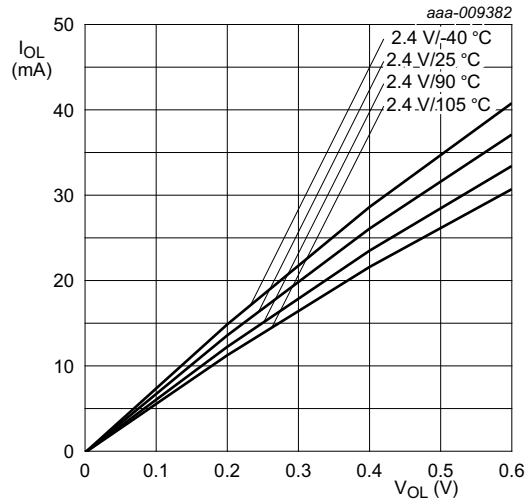


Conditions: V_{DD} = 2.4 V; ON pin PIO0_7 and PIO1_31.

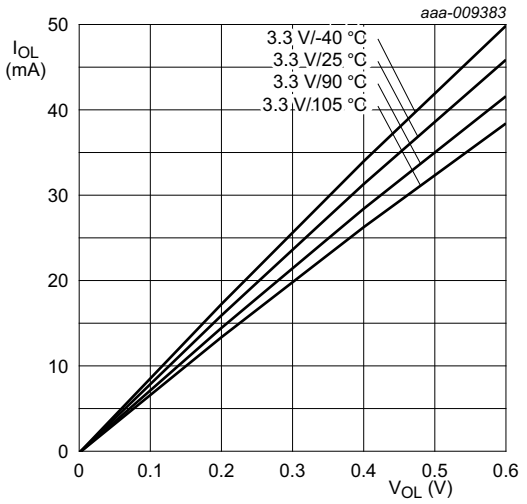


Conditions: V_{DD} = 3.3 V; ON pin PIO0_7 and PIO1_31.

Fig 23. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}



Conditions: V_{DD} = 2.4 V; on pins PIO0_4 and PIO0_5.

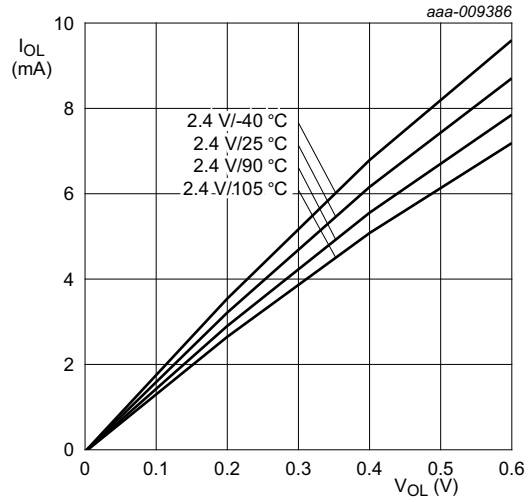


Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

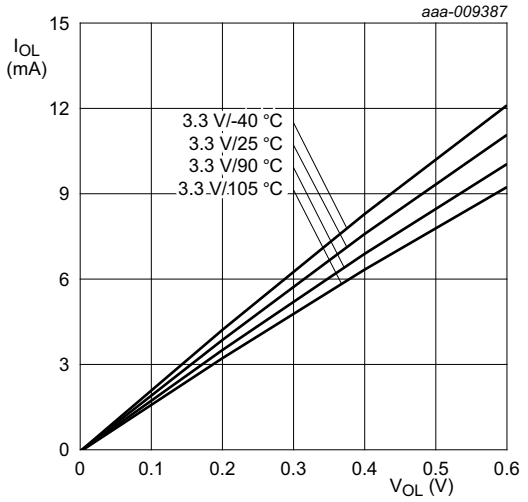
Fig 24. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

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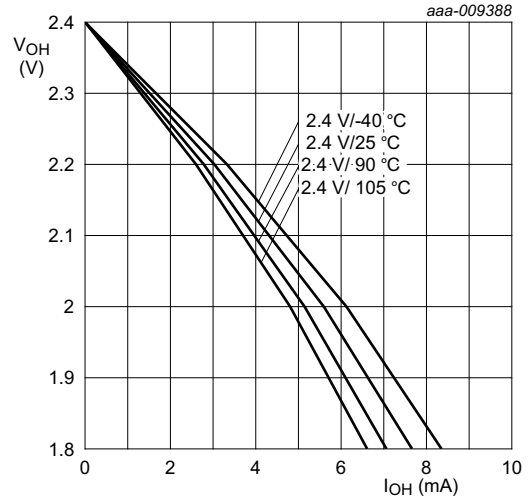


Conditions: V_{DD} = 2.4 V; standard port pins and high-drive pins PIO0_7 and PIO1_31.

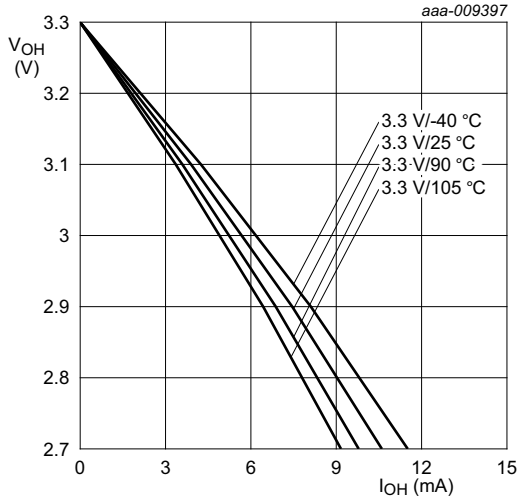


Conditions: V_{DD} = 3.3 V; standard port pins and high-drive pins PIO0_7 and PIO1_31.

Fig 25. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 2.4 V; standard port pins.

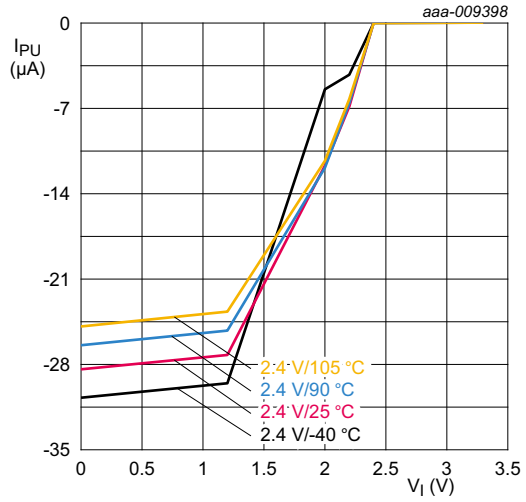


Conditions: V_{DD} = 3.3 V; standard port pins.

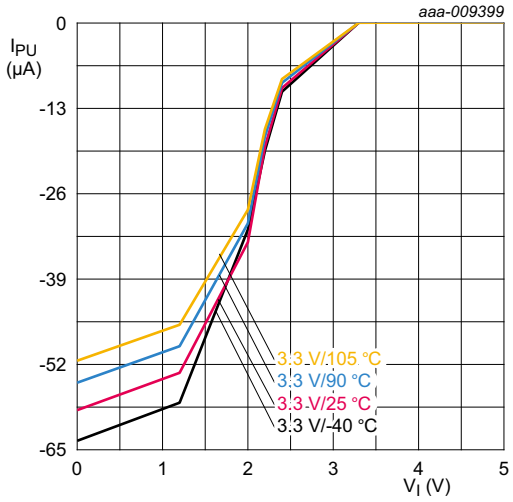
Fig 26. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

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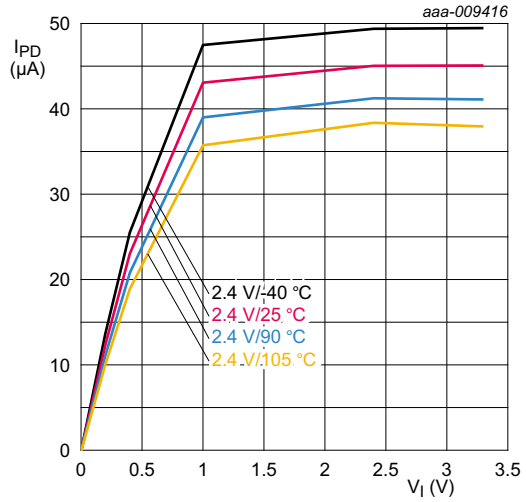


Conditions: V_{DD} = 2.4 V; standard port pins.

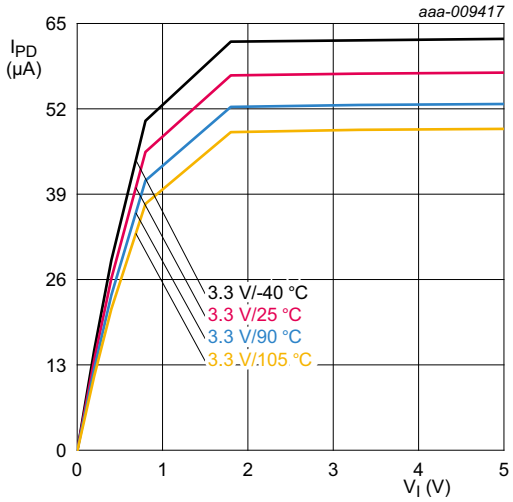


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 27. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 2.4 V; standard port pins.



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 28. Typical pull-down current I_{PD} versus input voltage V_I

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12. Dynamic characteristics

12.1 Flash/EEPROM memory

Table 10. Flash characteristics

T_{amb} = –40 °C to +105 °C. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	20	-	years
		unpowered		20	40	-	years
t_{er}	erase time	page or multiple consecutive pages, sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes to the flash. T_{amb} <= +85 °C. Flash programming with IAP calls (see *LPC11E6x user manual*).

Table 11. EEPROM characteristics

T_{amb} = –40 °C to +85 °C; V_{DD} = 2.7 V to 3.6 V. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance			100000	1000000	-	cycles
t_{ret}	retention time	powered		100	200	-	years
		unpowered		150	300	-	years
t_{prog}	programming time	64 bytes		-	2.9	-	ms

12.2 External clock for the oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.95 V (see Table 8). For connecting the oscillator to the XTAL pins, also see Section 14.3.

Table 12. Dynamic characteristic: external clock (XTALIN input)

T_{amb} = –40 °C to +105 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency			1	-	25	MHz
$T_{cy(clk)}$	clock cycle time			40	-	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time			-	-	5	ns
t_{CHCL}	clock fall time			-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

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[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

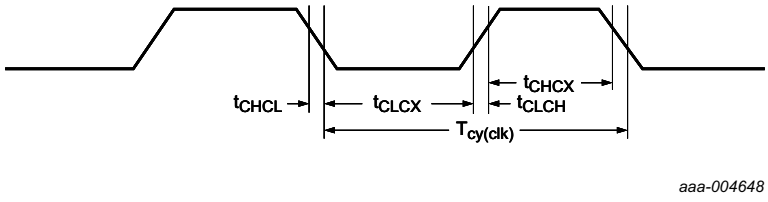


Fig 29. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

12.3 Internal oscillators

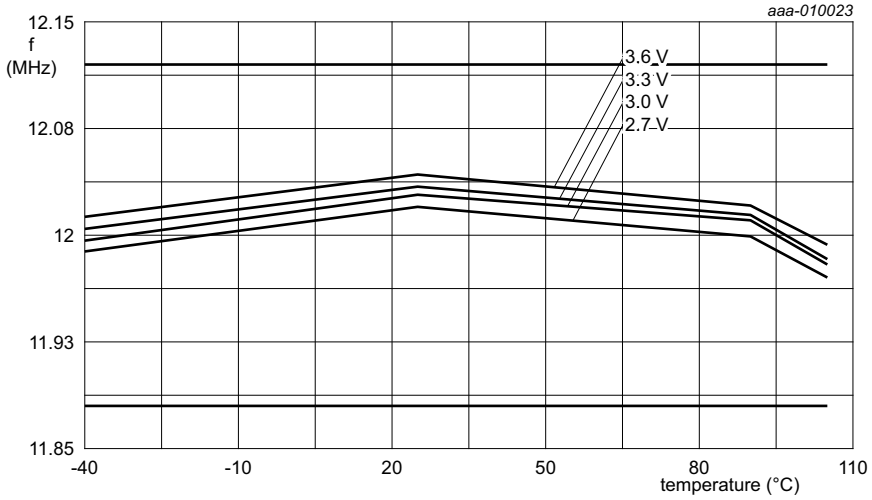
Table 13. Dynamic characteristics: IRC

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	−25 °C ≤ T_{amb} ≤ +85 °C	12 - 1 %	12	12 + 1 %	MHz
		−40 °C ≤ T_{amb} < −25 °C	12 - 2 %	12	12 + 1 %	MHz
		85 °C < T_{amb} ≤ 105 °C	12 - 1.5 %	12	12 + 1.5 %	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −25 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 30. Typical Internal RC oscillator frequency versus temperature

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Table 14. Dynamic characteristics: WatchDog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] See the *LPC11E6x user manual.*

12.4 I/O pins

Table 15. Dynamic characteristics: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	pin configured as output		3.0	-	5.0	ns
t_f	fall time	pin configured as output		2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

12.5 I²C-bus

Table 16. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	0.26	-	µs

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Table 16. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus; on pins PIO0_4 and PIO0_5	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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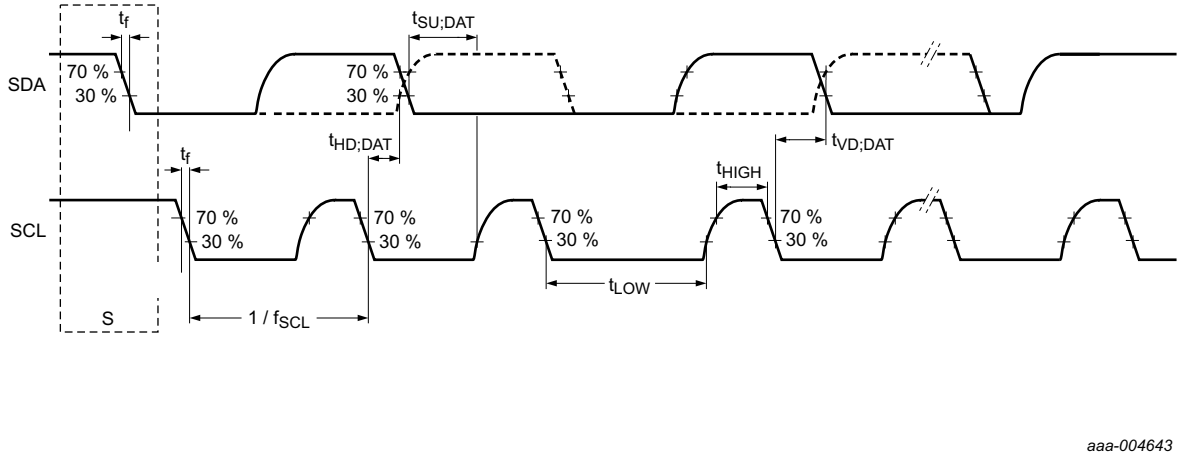


Fig 31. I²C-bus pins clock timing

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12.6 SSP interface

Table 17. Dynamic characteristics of SPI pins in SPI mode

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master (in SPI mode)							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	50	-	-	ns
		when only transmitting	[1]	40			ns
t_{DS}	data set-up time	in SPI mode	[2]	15	-	-	ns
t_{DH}	data hold time	in SPI mode	[2]	0	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	-	10	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	0	-	-	ns
SPI slave (in SPI mode)							
$T_{cy(PCLK)}$	PCLK cycle time			20	-	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	0	-	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	$3 \times T_{cy(PCLK)} + 4$	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	-	$3 \times T_{cy(PCLK)} + 11$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	-	-	$2 \times T_{cy(PCLK)} + 5$	ns

[1] $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SPI peripheral clock divider (SSPCLKDIV), the SPI SCR parameter (specified in the SSP0CR0 register), and the SPI CPSDVSR parameter (specified in the SPI clock prescale register).

[2] $T_{amb} = -40$ °C to 105 °C; 2.4 V ≤ V_{DD} ≤ 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

[4] T_{amb} = 25 °C; for normal voltage supply range: V_{DD} = 3.3 V.

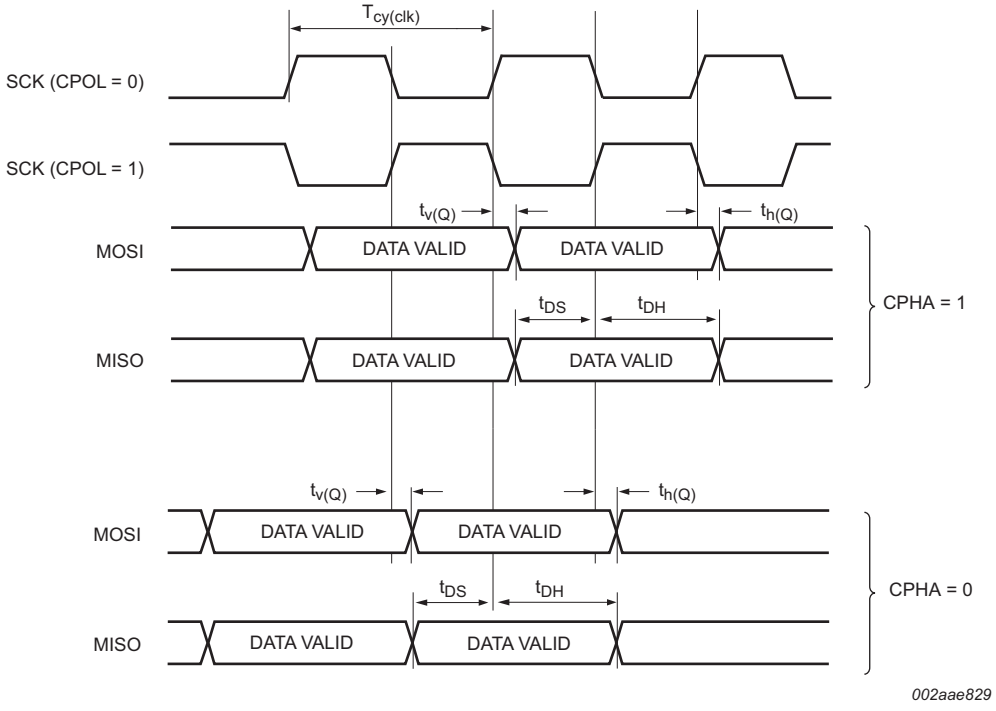


Fig 32. SSP master timing in SPI mode

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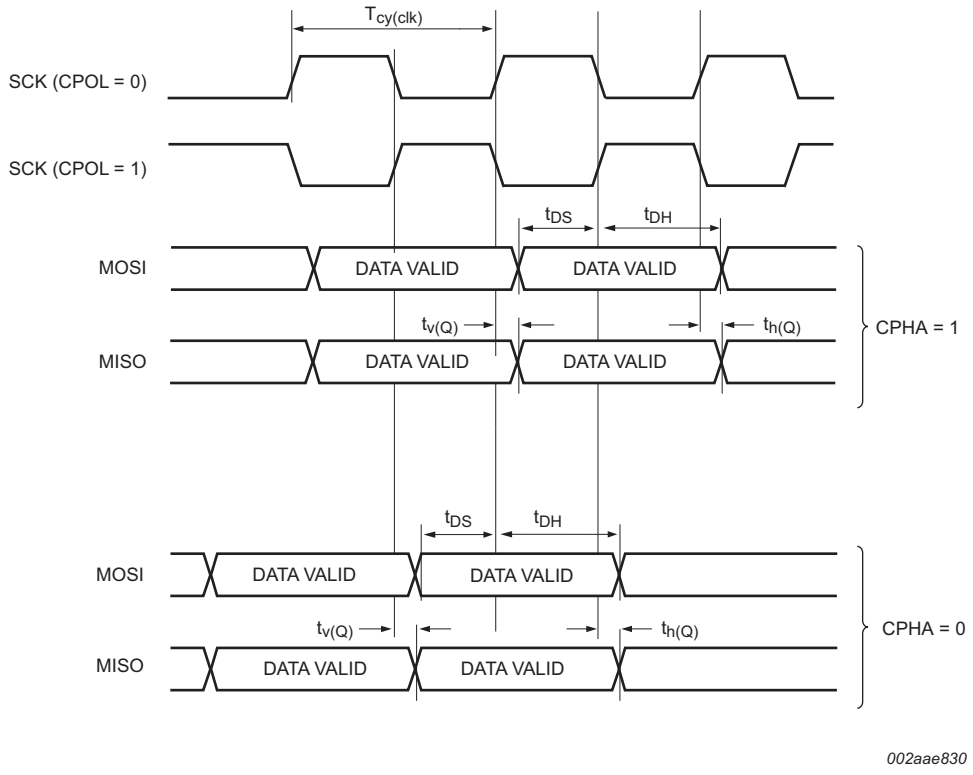


Fig 33. SSP slave timing in SPI mode

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12.7 USART interface

The maximum USART bit rate for all USARTs is 3.125 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous slave and master mode.

Table 18. USART dynamic characteristics USART0

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	[1]	100	-	ns
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time		44	-	ns
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		-	10	ns
$t_{h(Q)}$	data output hold time		0	-	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		20	-	ns
$t_{v(Q)}$	data output valid time		-	40	ns
$t_{h(Q)}$	data output hold time		25	-	ns

[1] $T_{cy(clk)}$ = (main clock cycle time)/(UARTCLKDIV x 2 x (256 x DLM + DLL)). See the *LPC11E6x User manual UM10732*.

Table 19. USART dynamic characteristics USART1/2/3/4

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V; C_L = 10 pF. Simulated parameters sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	[1]	100	-	ns
USART master (in synchronous mode)					
$t_{su(D)}$	data input set-up time		44	-	ns
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		-	10	ns
$t_{h(Q)}$	data output hold time		0	-	ns
USART slave (in synchronous mode)					
$t_{su(D)}$	data input set-up time		5	-	ns
$t_{h(D)}$	data input hold time		0	-	ns
$t_{v(Q)}$	data output valid time		-	40	ns
$t_{h(Q)}$	data output hold time		20	-	ns

[1] $T_{cy(clk)}$ = U_PCLK/BRGVAL. See the *LPC11E6x User manual UM10732*.

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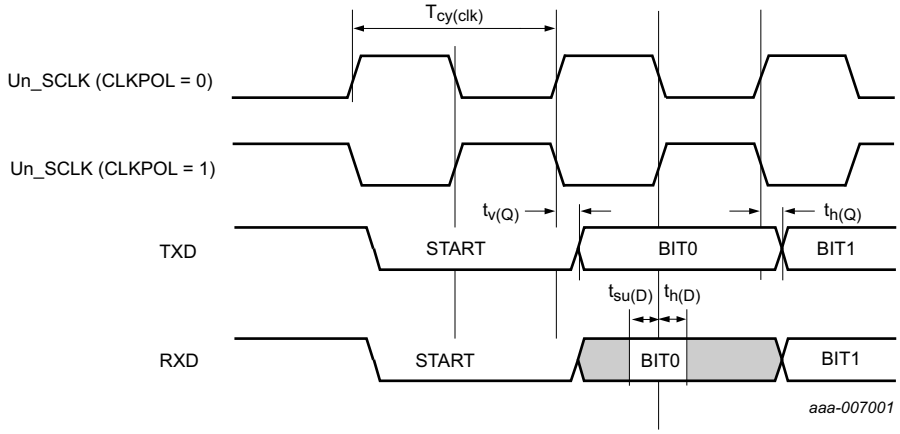


Fig 34. USART timing

12.8 SCTimer/PWM output timing

To estimate the skew between different outputs, compare the worst case to worst case (or best case to best case) values of individual pins.

Table 20. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V <= V_{DD} <= 3.6 V. Simulated skew (over process, voltage, and temperature) between any two SCT outputs; sampled at the 50 % level of the falling or rising edge; values guaranteed by design.

Symbol	Parameter		Min	Max	Unit
SCTimer0/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns
SCTimer1/PWM					
$t_{sk(o)}$	output skew time		< 1	2	ns

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13. Characteristics of analog peripherals

Table 21. BOD static characteristics[1]

T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2					
		assertion		-	2.54	-	V
		de-assertion		-	2.68	-	V
		interrupt level 3					
		assertion		-	2.82	-	V
		de-assertion		-	2.93	-	V
		reset level 2					
		assertion		-	2.34	-	V
		de-assertion		-	2.49	-	V
		reset level 3					
		assertion		-	2.62	-	V
		de-assertion		-	2.77	-	V

[1] Interrupt and reset levels are selected by writing the level value to the BOD control register BODCTRL, see *the LPC11E6x user manual*. Interrupt levels 0 and 1 are reserved.

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Table 22. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; V_{DD} = 2.4 V to 3.6 V; VREFP = V_{DDA}; V_{SSA} = 0; VREFN = V_{SSA}. ADC calibrated at T = 25 °C.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IA}	analog input voltage		[2]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[3]	-	-	0.1	pF
$f_{clk(ADC)}$	ADC clock frequency	$V_{DDA} \geq 2.7$ V				50	MHz
		$V_{DDA} \geq 2.4$ V				25	MHz
f_s	sampling frequency	$V_{DDA} \geq 2.7$ V		-	-	2	Msamples/s
		$V_{DDA} \geq 2.4$ V		-	-	1	Msamples/s
E_D	differential linearity error		[4]	-	-	±2.5	LSB
$E_{L(adj)}$	integral non-linearity		[5]	-	-	±2.5	LSB
E_O	offset error		[6]	-	-	±4.5	LSB
$V_{err(FS)}$	full-scale error voltage		[7]	-	-	±0.5	%
Z_i	input impedance	f_s = 2 Msamples/s	[8][9]	0.1	-	-	MΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The input resistance of ADC channel 0 is higher than for all other channels.

[3] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 2 Msamples/s.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 35.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 35.

[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 35.

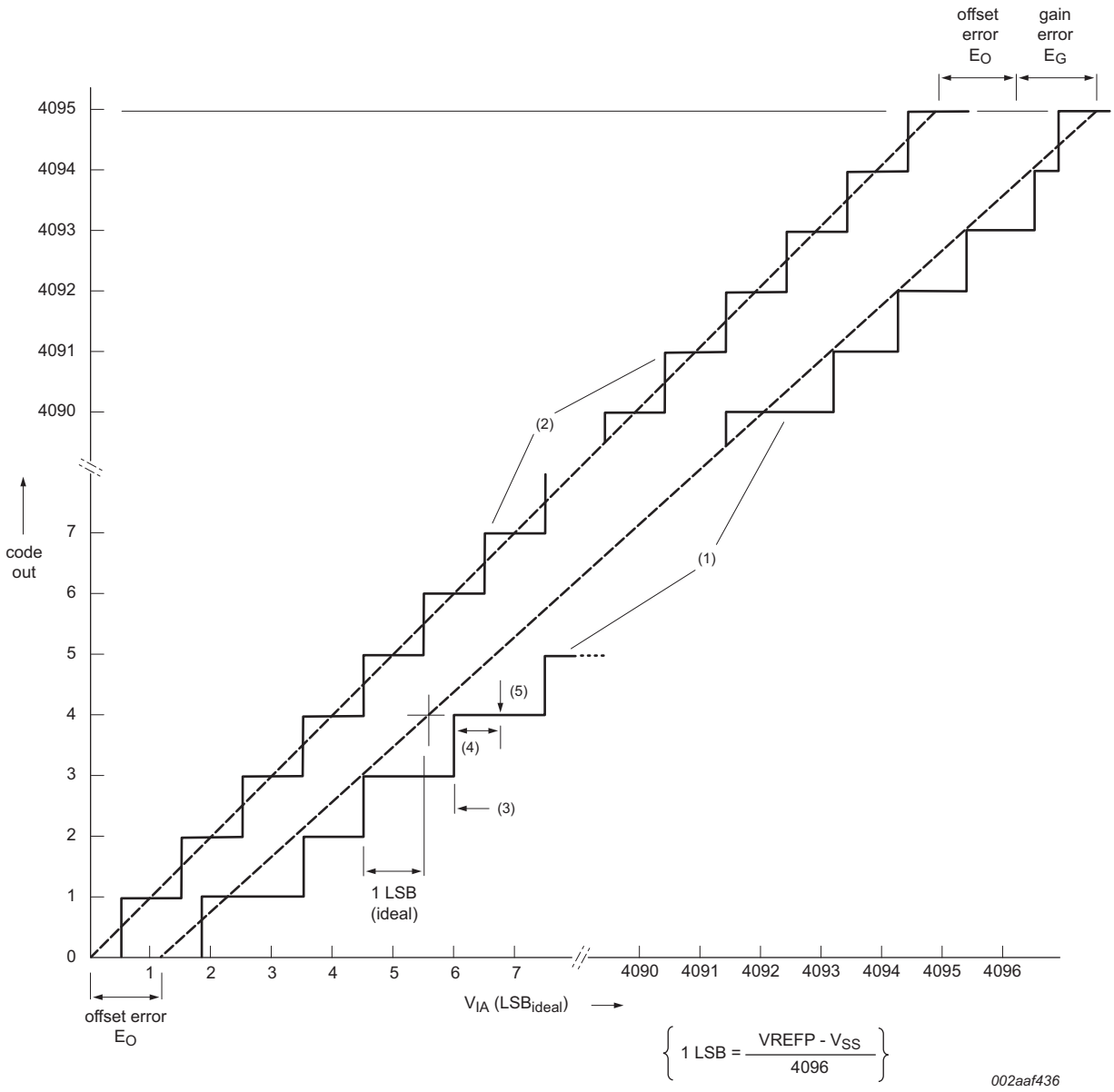
[7] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 35.

[8] T_{amb} = 25 °C; maximum sampling frequency f_s = 2 Msamples/s and analog input capacitance C_{ia} = 0.1 pF.

[9] Input resistance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia}: $Z_i \propto 1 / (f_s \times C_i)$. See Figure 36 “ADC input impedance”.

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(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 35. 12-bit ADC characteristics

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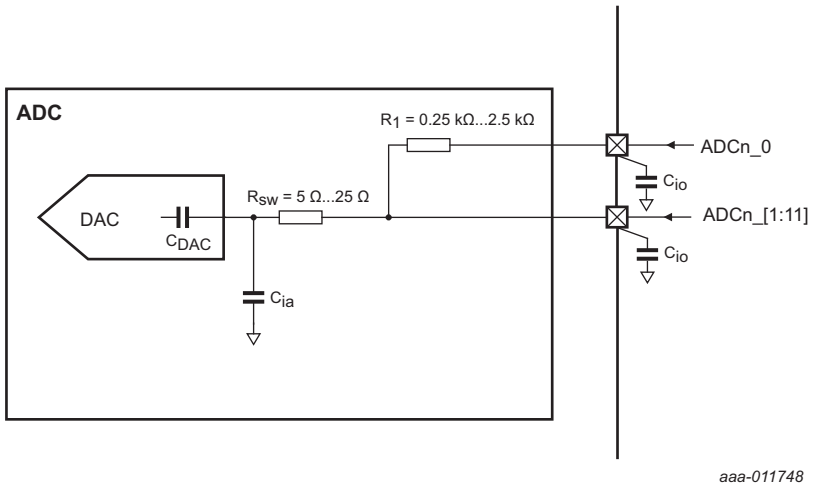


Fig 36. ADC input impedance

Table 23. Temperature sensor static and dynamic characteristics
V_{DDA} = 2.4 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = –40 °C to +105 °C	[1]	-	±5	-	°C
E_L	linearity error	T_{amb} = –40 °C to +105 °C		-	±4	-	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	14	-	µs

[1] Absolute temperature accuracy.

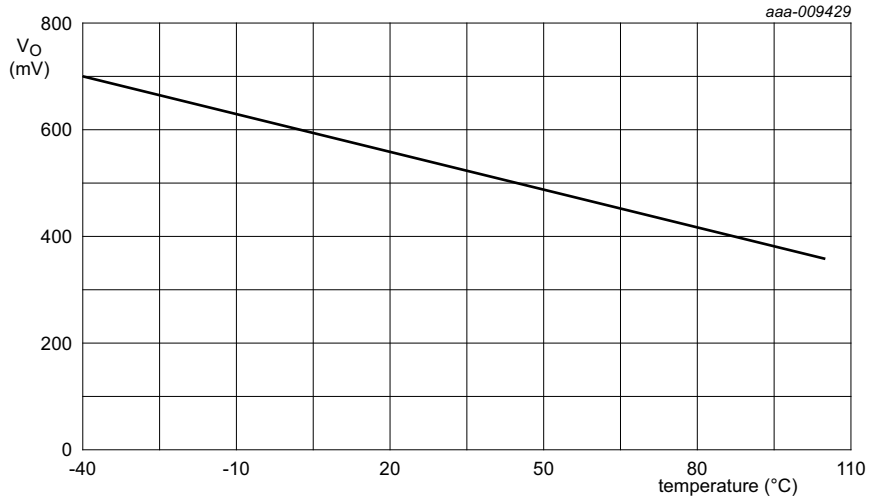
[2] Typical values are derived from nominal simulation (V_{DDA} = 3.3 V; T_{amb} = 27 °C; nominal process models).

Table 24. Temperature sensor Linear-Least-Square (LLS) fit parameters
V_{DDA} = 2.4 V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = –40 °C to +105 °C		-	–2.36	-	mV/°C
LLS intercept	T_{amb} = –40 °C to +105 °C		-	606	-	mV

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V_{DDA} = 3.3 V; measured on a typical silicon sample.

Fig 37. Typical LLS fit of the temperature sensor output voltage

14. Application information

14.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 22:

- The ADC input trace must be short and as close as possible to the LPC11E6x chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- If the ADC and the digital core share the power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

14.2 Typical wake-up times

Table 25. Typical wake-up times

V_{DD} = 3.3 V; T_{amb} = 25 °C.

Power modes	Wake-up time
Sleep mode (12 MHz)[1][2]	2.6 μs
Deep-sleep mode[1][3]	4.4 μs
Power-down mode[1][3]	86.8 μs
Deep Power-down mode[4]	276 μs

[1] The wake-up time measured is the time between when a GPIO input pin is triggered to wake up the device from the low-power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[2] IRC enabled, all peripherals off.

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[3] WatchDog oscillator disabled, Brown-Out Detect (BOD) disabled.

[4] Wake-up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when a wake-up pin is triggered to wake up the device from the low-power modes and when a GPIO output pin is set in the reset handler.

14.3 XTAL input and crystal oscillator component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

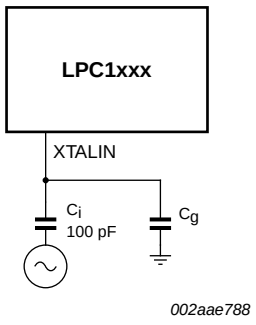


Fig 38. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled through a capacitor of 100 pF (Figure 38), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 39 and in Table 26 and Table 27. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} must be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 39 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 26).

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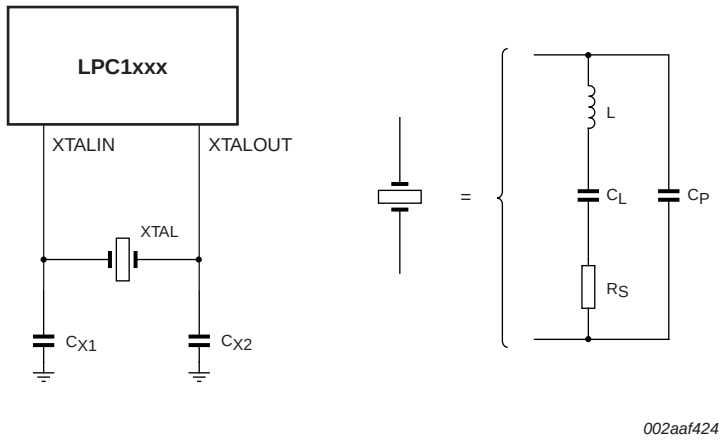


Fig 39. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{osc}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 27. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{osc}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.4 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible to

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keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.

14.5 RTC oscillator component selection

The 32 kHz crystal must be connected to the part via the RTCXIN and RTCXOUT pins as shown in Figure 40. If the RTC is not used, the RTCXIN pin can be grounded.

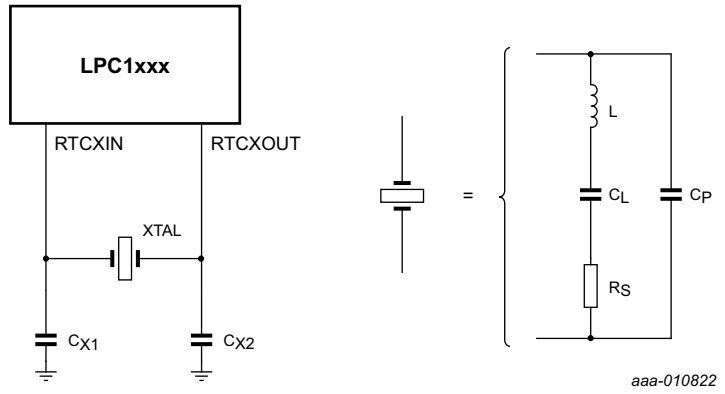


Fig 40. RTC oscillator components

Select C_{x1} and C_{x2} based on the external 32 kHz crystal used in the application circuitry. The pad capacitance C_P of the RTCXIN and RTCXOUT pad is 3 pF. If load capacitance of the external crystal is C_L, the optimal C_{x1} and C_{x2} can be selected as:

$C_{x1} = C_{x2} = 2 \times C_L - C_P$

To achieve the best performance and accurate frequency, it is recommended to use Cx1 = Cx2 = 24 pF and CL = 12 pF.

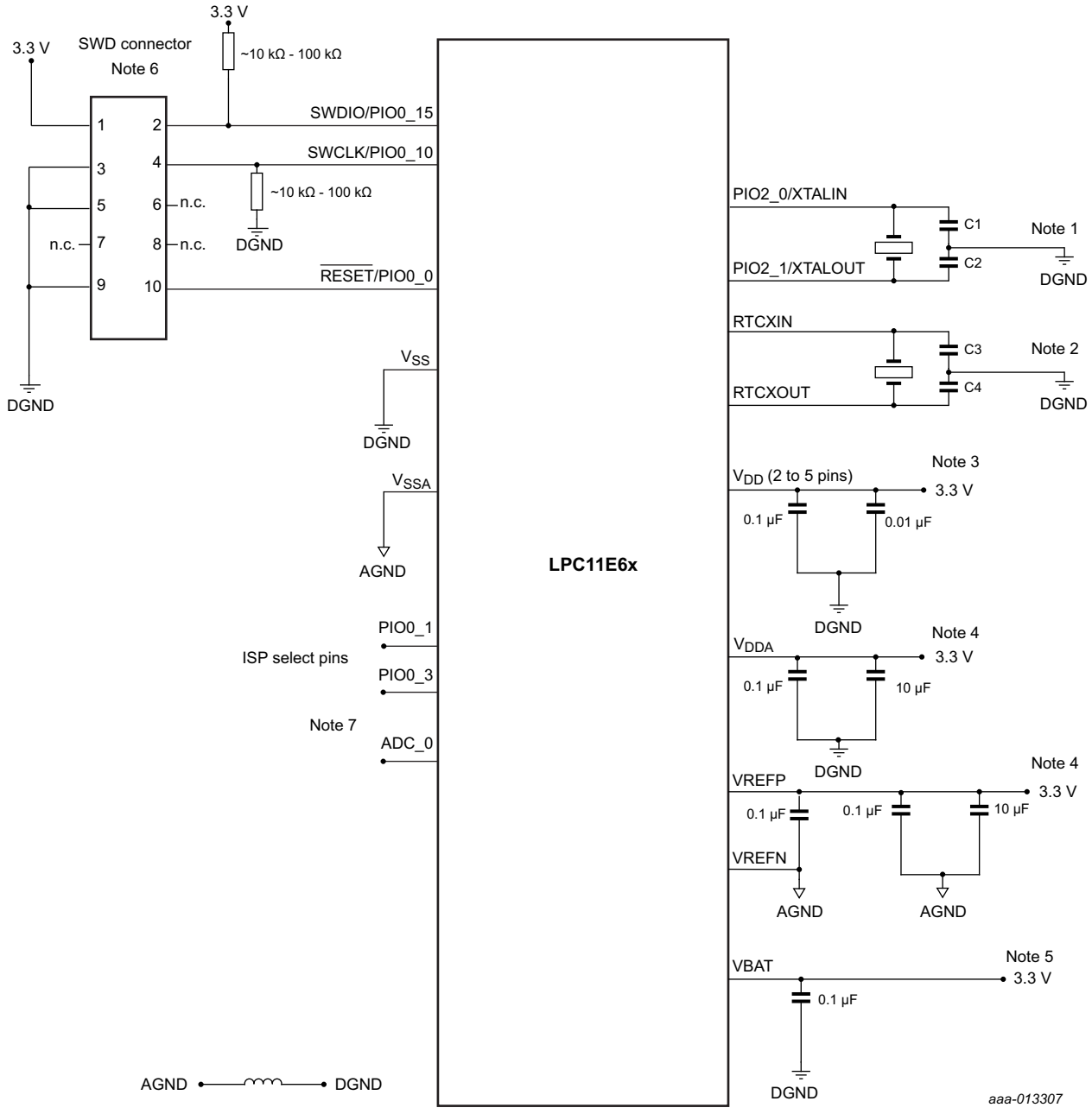
Please note the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on the hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the CLOCKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

14.6 Connecting power, clocks, and debug functions

Figure 41 shows the basic board connections to power the LPC11E6x, to connect an external crystal and the 32 kHz oscillator, and provide debug capabilities.

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(1) See Section 14.3 “XTAL input and crystal oscillator component selection” for the values of C1 and C2.

(2) See Section 14.5 “RTC oscillator component selection” for the values of C3 and C4.

(3) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(4) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(5) Position the decoupling capacitor of 0.1 µF as close as possible to the VBAT pin. Tie VBAT to V_{DD} if not used.

(6) Uses the ARM 10-pin interface for SWD.

(7) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

Fig 41. Power, clock, and debug connections

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14.7 Termination of unused pins

Table 28 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 28. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$/PIO0_0	I; PU	In an application that does not use the $\overline{\text{RESET}}$ pin or its GPIO function, the termination of this pin depends on whether Deep power-down mode is used: • Deep power-down used: Connect an external pull-up resistor and keep pin in default state (input, pull-up enabled) during all other power modes. • Deep power-down not used and no external pull-up connected: can be left unconnected if internal pull-up is disabled and pin is driven LOW and configured as output by software.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
$\overline{\text{RSTOUT}}$	IA; O	Can be left unconnected. Not configurable by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VBAT	-	Tie to VDD if no external battery connected.
VSSA	-	Tie to VSS.

[1] I = Input, O = Output, IA = Inactive (no pull-up/pull-down enabled), F = floating, PU = Pull-Up.

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14.8 Pin states in different power modes

Table 29. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep/Power-down	Deep power-down
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating.
PIO0_4/PIO0_5 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating.
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled.			Reset function disabled; floating; if the part is in deep power-down mode, the $\overline{\text{RESET}}$ pin needs an external pull-up to reduce power consumption.
PIO0_16/ WAKEUP	As configured in the IOCON[1]. WAKEUP function inactive.			Wake-up function enabled; can be disabled by software.

[1] Default and programmed pin states are retained in sleep, deep-sleep, and power-down modes.

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14.9 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for part LPC11U68JBD100 (similar to LPC11E68JBD100).

Table 30. ElectroMagnetic Compatibility (EMC) for part LPC11U68 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =				Unit
		12 MHz	24 MHz	36 MHz	48 MHz	
Input clock: IRC (12 MHz)						
maximum peak level	1 MHz to 30 MHz	-5	-5	-5	-5	dBµV
	30 MHz to 150 MHz	-1	0	+4	+4	dBµV
	150 MHz to 1 GHz	-1	0	+4	+4	dBµV
IEC level[1]	-	O	O	O	O	-
Input clock: crystal oscillator (12 MHz)						
maximum peak level	1 MHz to 30 MHz	-2	–6	-4	-5	dBµV
	30 MHz to 150 MHz	-1	0	+3	+3	dBµV
	150 MHz to 1 GHz	-2	0	+2	+5	dBµV
IEC level[1]	-	O	O	O	O	-

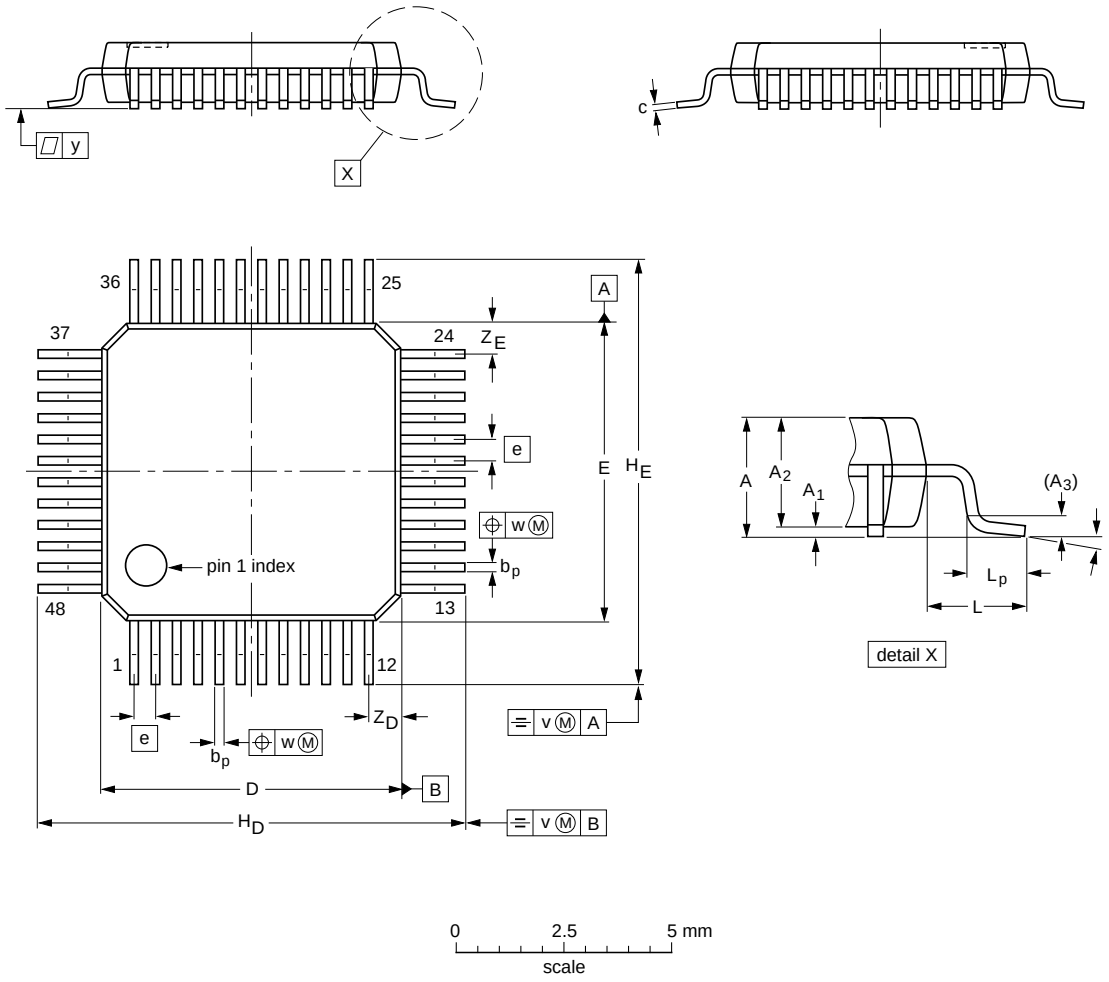
[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

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15. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

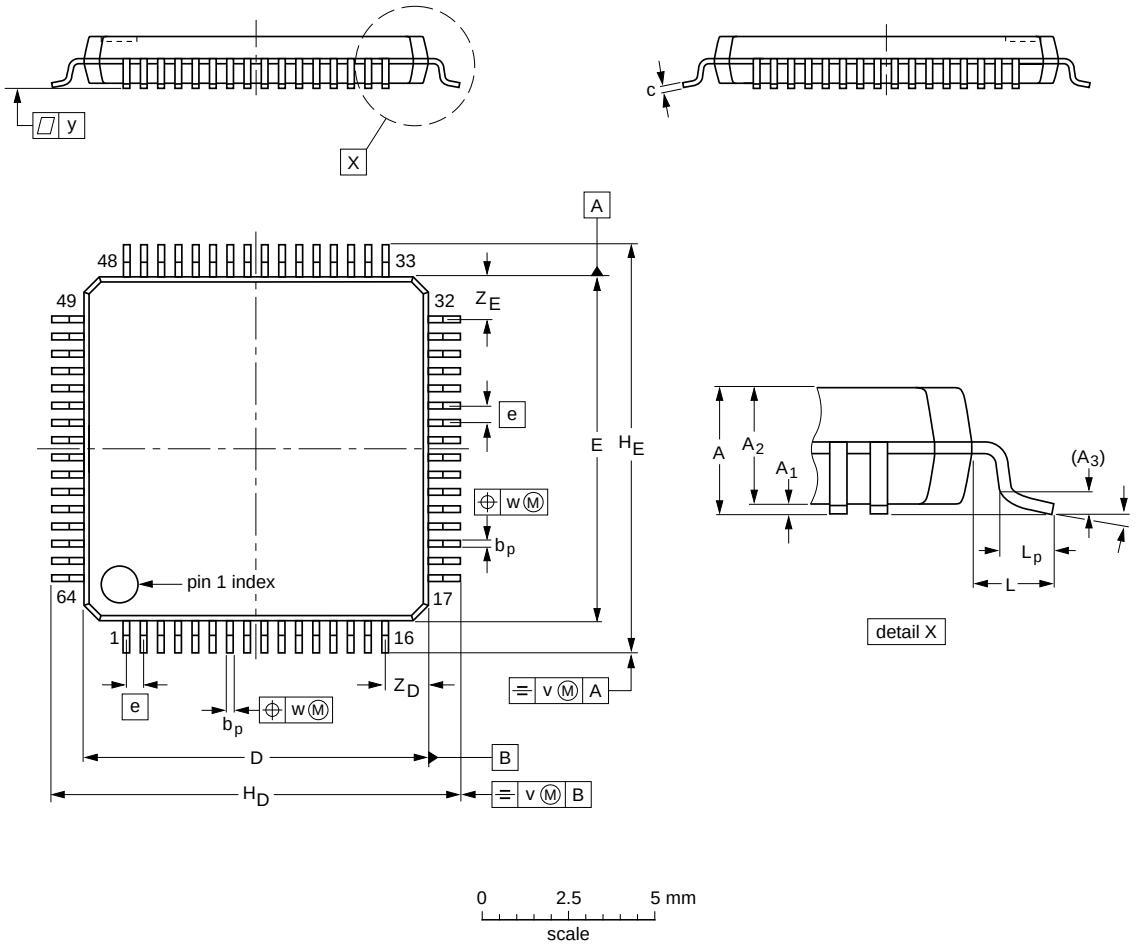
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 42. Package outline LQFP48 (SOT313-2)

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LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

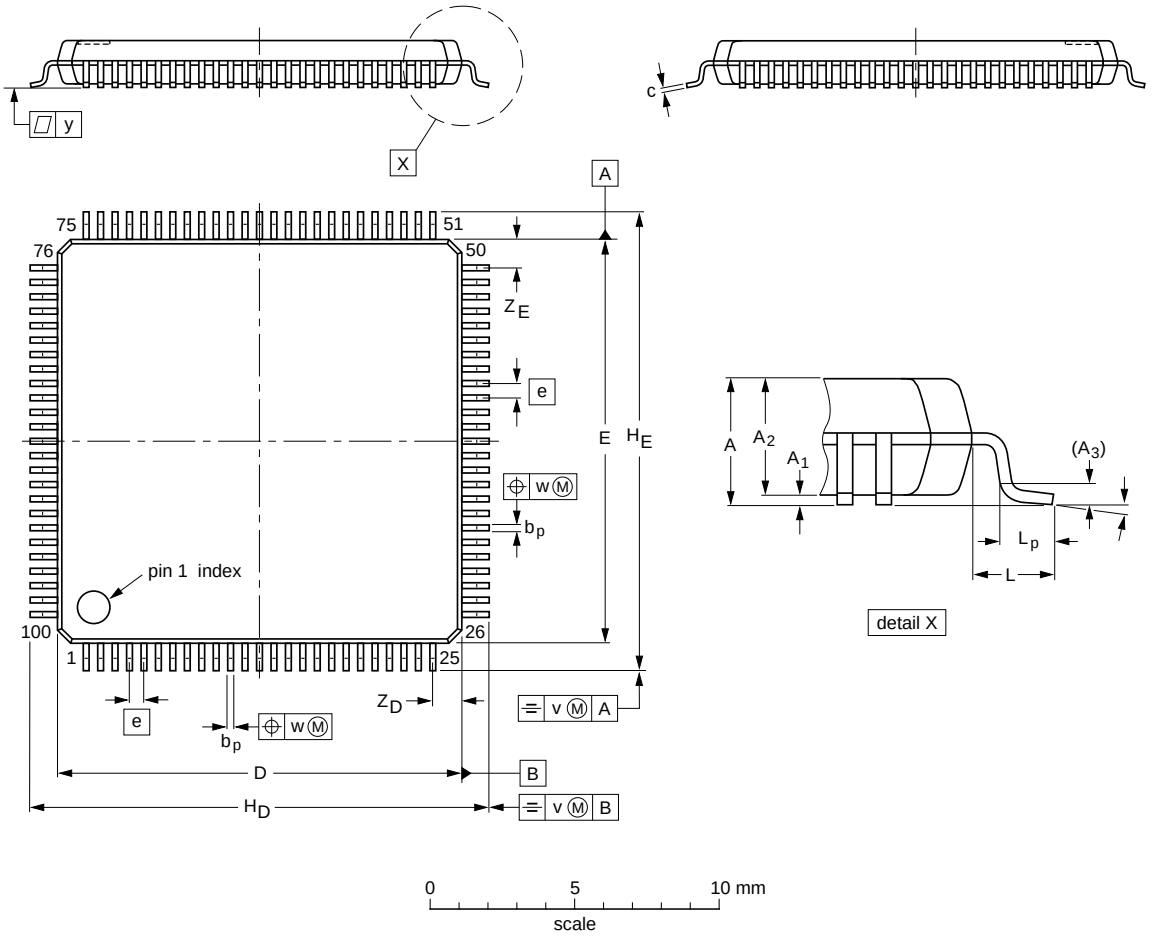
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
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Fig 43. Package outline LQFP64 (SOT314-2)

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LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

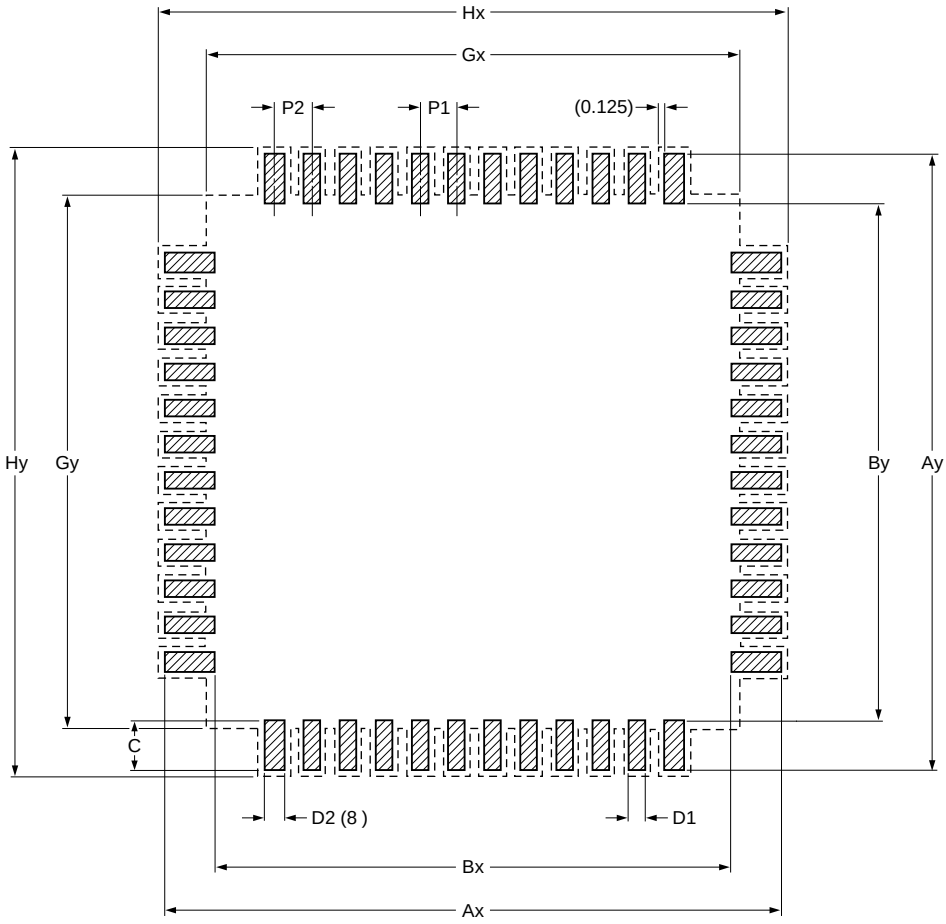
Fig 44. Package outline LQFP100 (SOT407-1)

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16. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

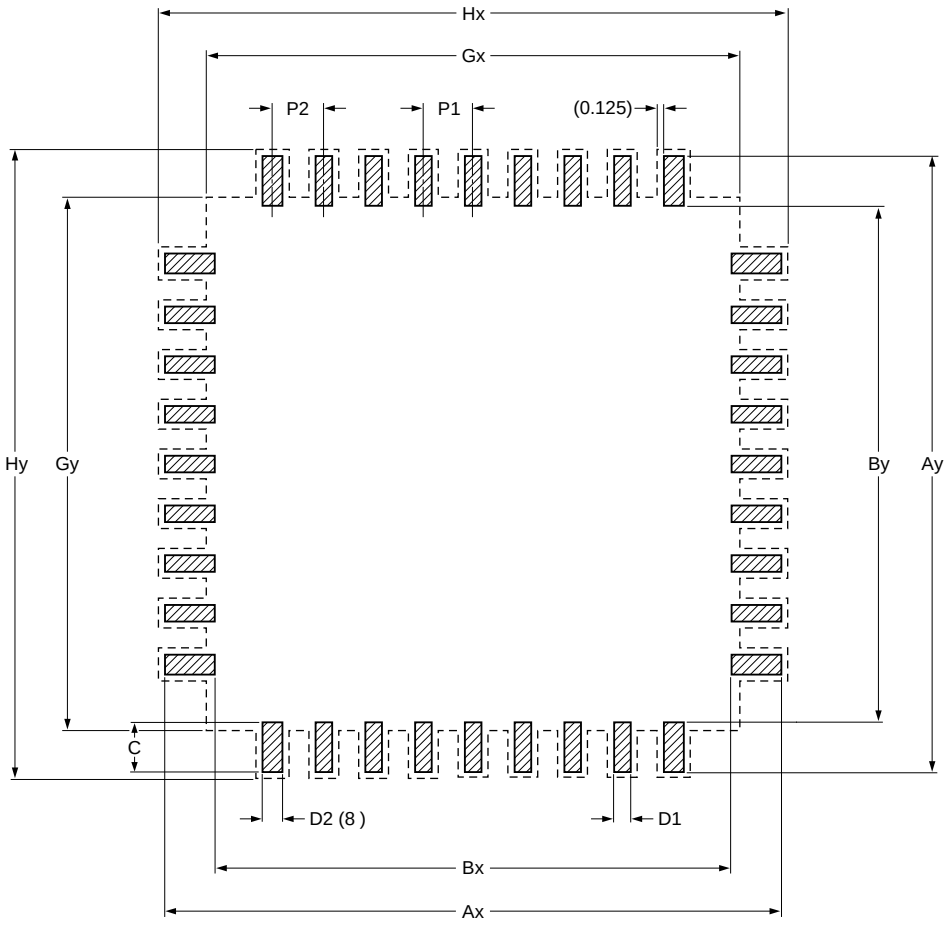
sot313-2_fr

Fig 45. Reflow soldering for the LQFP48 package

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Footprint information for reflow soldering of LQFP64 package **SOT314-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	13.300	13.300	10.300	10.300	1.500	0.280	0.400	10.500	10.500	13.550	13.550

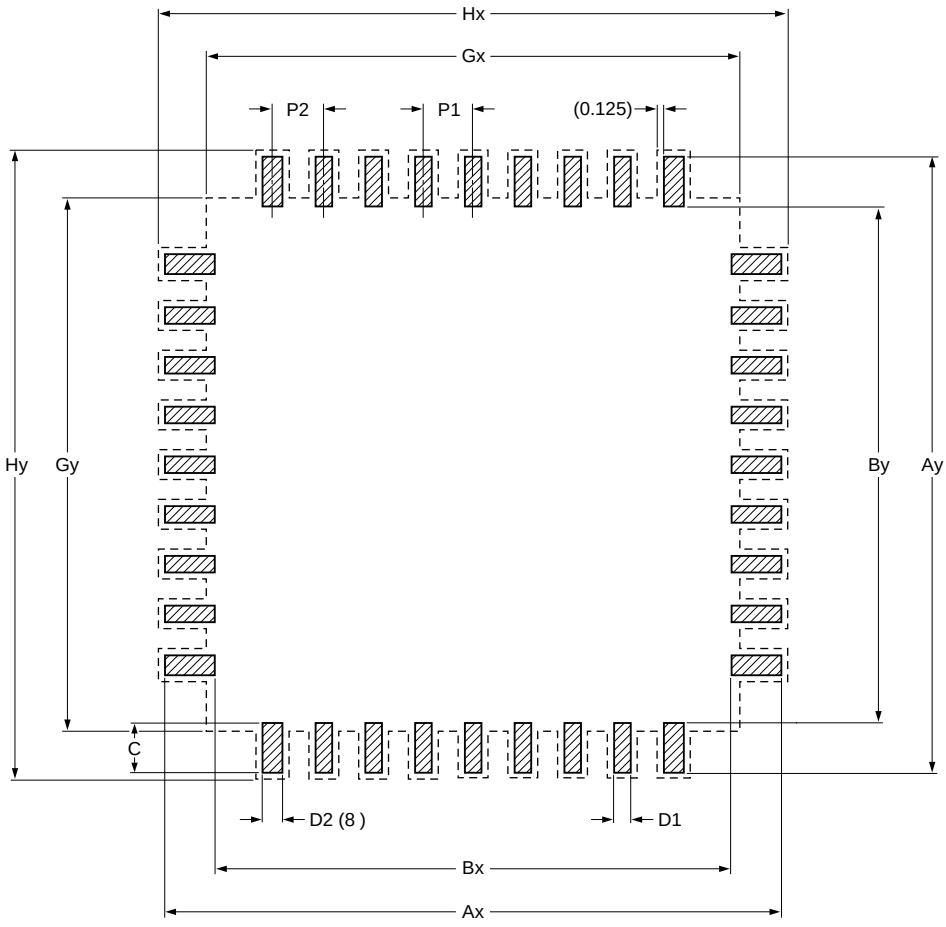
sot314-2_fr

Fig 46. Reflow soldering for the LQFP64 package

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Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 47. Reflow soldering for the LQFP100 package

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17. Abbreviations

Table 31. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter

18. References

[1] LPC11U6x/E6x User manual UM10732:
http://www.nxp.com/documents/user_manual/UM10732.pdf

[2] LPC11E6x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC11E6X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

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19. Revision history

Table 32. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11U6x v.1.5	20200812	Product data sheet	-	LPC11U6x v.1.4
Modifications:	• Updated Section 14.5 “RTC oscillator component selection” with minor wording alteration.			
LPC11U6x v.1.4	20200724	Product data sheet	-	LPC11U6x v.1.3
Modifications:	• Updated Section 14.5 “RTC oscillator component selection” with frequency recommendation.			
LPC11E6X v.1.3	20160906	Product data sheet	-	LPC11E6X v.1.2
Modifications:	• Section 14.9 “ElectroMagnetic Compatibility (EMC)” added. • Replaced CT16B0_CAP1 with CT16B0_CAP2 for pin PI01_21. See Table 3 “Pin description”. • Replaced CT32B0_CAP1 with CT32B0_CAP2 for pin PIO1_6 and pin PIO1_29. See Table 3 “Pin description”. • Updated Figure 7 “AHB multilayer matrix”: HS GPIO connects with M0+ Core, not with DMA or USB.			
LPC11E6X v.1.2	20140521	Product data sheet	-	LPC11E6X v.1.1
Modifications:	• Parts added: LPC11E68JBD48, LPC11E67JBD100, LPC11E67JBD64, LPC11E66JBD48. • Section 14.6 “Connecting power, clocks, and debug functions” added. • Section 14.7 “Termination of unused pins” added. • Section 14.8 “Pin states in different power modes” added. • Changed recommendation for VBAT connection if unused: Tie to VDD. See Table 3 “Pin description”.			
LPC11E6X v.1.1	20140417	Product data sheet	-	LPC11E6X v.1
Modifications:	• Data sheet status changed to product data sheet. • Section 5 “Marking” updated with revision information.			
LPC11E6X v.1	20140326	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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