Resonant-Switching Driver Controller for LED Lighting

Check for Samples: TPS92020

FEATURES

- **LLC Resonant Switching Driver Controller for Multi-String LED Lighting Applications**
- **Half-Bridge Topology**
- **Fixed or Variable Switching Frequency Control**
- **Programmable Soft-Start Time**
- **Programmable Dead Time for Best Efficiency**
- **Easy ON/OFF Control**
- **Overcurrent Protection**
- **Over-Temperature Protection**
- **Bias Voltage UVLO and OVP**
- **Integrated Gate Driver With 0.4-A Source and 0.8-A Sink Capability**
- **Operating Temperature Range: –40°C to 125°C**
- **SOIC 8-Pin Package**

APPLICATIONS

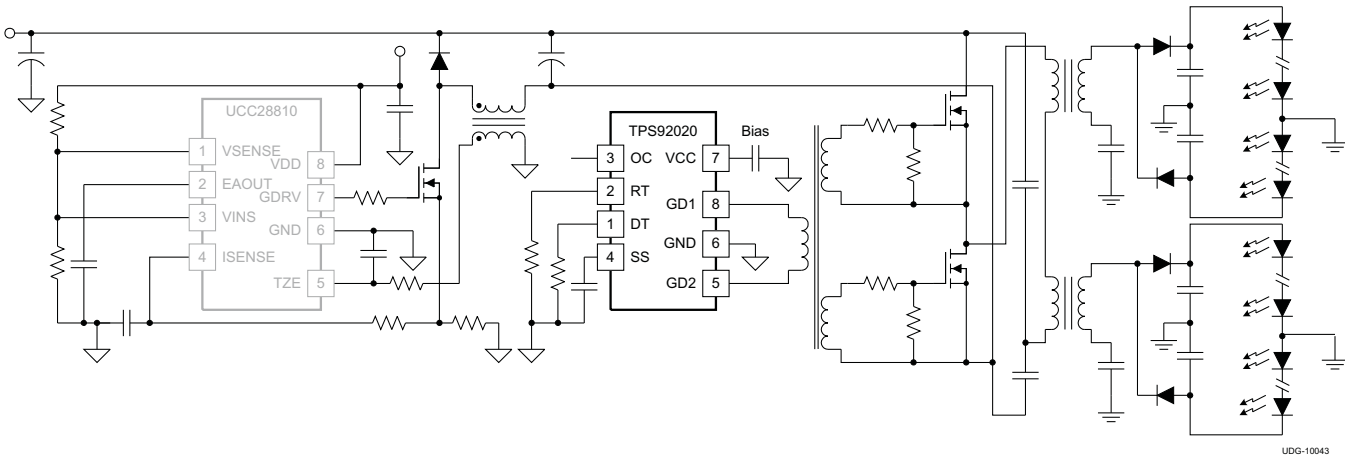
- **Commercial / Industrial LED Lighting Drivers**
- **High Bay LED Lighting**
- **Low Bay LED Lighting**
- **Street LED Lighting**
- **Area LED Lighting**
- **Stadium LED Lighting**
- **LED Wall Washing**
- **LED DTV and Monitor Back-lighting**
- **Electronic Lighting Ballasts**

DESCRIPTION

The TPS92020 is a high-performance resonant-switching LED driver controller. It is designed for use in higher power LED lighting systems. The TPS92020 uses resonant switching in an LLC topology to achieve a very high efficiency compared to traditional half-bridge converters.

The programmable dead time enables zero-voltage switching with minimum magnetizing current, maximizing system efficiency across a variety of applications.

The TPS92020 can operate in two switching frequency modes. Fixed frequency allows for simple design when the load current is constant while variable switching allows for optimal closed-loop control for loads with varying currents. The internal oscillator supports the switching frequencies from 30 kHz to 350 kHz. This high-accuracy oscillator realizes the minimum switching frequency limiting with 4% tolerance, allowing the designer to avoid *over-design* of the power stage and, thus, further reducing overall system cost.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The programmable soft-start timer maximizes design flexibility demanded by the varied requirements of end equipments utilizing a half-bridge topology. The TPS92020 incorporates a 0.4-A source and 0.8-A sink for driving a low-cost gate driver transformer, delivering complete system protection functions including overcurrent, UVLO, bias supply OVP and OTP.

Table 1. PACKAGE INFORMATION(1)

DEVICE	PACKAGE	OPERATING FREQUENCY	OPERATING TEMPERATURE
TPS92020D	8-Pin SOIC	Variable	-40°C to 125°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2) (3) (4)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNITS
		MIN	MAX	
Voltage range	VCC		22	V
	GD1, GD2	-0.5	V_{VCC} + 0.5	
Gate drive current – continuous	GD1, GD2		± 25	mA
Current range	RT		–5	
	DT		-0.7	
Operating junction temperature	T_J	−40	125	°C
Storage temperature	T_{stg}	−65	150	
Electrostatic Discharge	Human Body Model (HBM)		2,000	V
	Charged Device Model (CDM)		500	
Lead temperature (10 seconds)			260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) In normal use, terminals GD1 and GD2 are connected to an external gate driver and are internally limited in output current.

DISSIPATION RATINGS

PACKAGE	THERMAL IMPEDANCE, JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
8-Pin SOIC	150°C/watt (1) (2)	667 mW (1)	267 mW (1)

(1) Thermal resistance is a strong function of board construction and layout. Air flow will reduce thermal resistance. This number is only a general guide.
(2) Thermal resistance calculated with a low-K methodology.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{VCC}	VCC input voltage from a low-impedance source	11.5		18.0	V
R_{RT}	RT resistor	1		8.666	kΩ
R_{DT}	DT resistor	3.3		39	
C_{SS}	SS capacitor	0.01		1	µF

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, −40°C < T_A < 125°C, T_J = T_A, V_{VCC} = 12 V, GND = 0 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, C_{VCC} = 1 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY (VCC)						
	VCC current, disabled	SS = 0 V		1	1.5	mA
	VCC current, enabled	SS = 5 V, C_{GD1} = C_{GD2} = 1 nF	2.5	5	7.5	
	VCC current, UVLO	VCC = 9 V		100	400	µA
V_{UVLO}	UVLO turn-on threshold	Measured at VCC rising	9.9	10.5	11.1	V
	UVLO turn-off threshold	Measured at VCC falling	8.9	9.5	10.1	
	UVLO hysteresis	Measured at VCC	0.7	1	1.3	
V_{OVP}	OVP turn-off threshold	Measured at VCC rising	18	20	22	
	OVP turn-on threshold	Measured at VCC falling	16	18	20	
	OVP hysteresis	Measured at VCC	1.5	2	2.5	
DEAD TIME (DT)						
t_{DT}	Dead time	R_{DT} = 16.9 kΩ	390	420	450	ns
OSCILLATOR						
$f_{SW(min)}$	Minimum switching frequency at GD1, GD2	-40°C ≤ T_A ≤ 125°C	40.04	41.70	43.36	kHz
		-20°C ≤ T_A ≤ 105°C	40.45	41.70	42.95	
K_{ICO}	Switching frequency gain/I (RT)	R_{RT} = 4.7 kΩ, I_{RT} = 0 to 1 mA	60	80	100	Hz/µA
t	GD1, GD2 on- time mismatching		-50		50	ns
$f_{SW(bm)}$	Switching frequency starting burst mode	V_{SS} = 5 V	300	350	400	kHz
	Switching frequency to come out of burst mode	V_{SS} = 5 V	280	330	380	
$f_{SW(start)}$	Switching frequency at soft start	-40°C ≤ T_A ≤ 125°C	122	142.5	162	
		-20°C ≤ T_A ≤ 105°C	125	142.5	160	
EXTERNAL DISABLE/SOFT START						
	Enable threshold	Measure at SS rising	1.1	1.2	1.3	V
	Disable threshold	Measured at SS falling	0.85	1	1.1	
	Disable hysteresis	Measured at SS	0.15		0.35	
	Disable prop. delay	Measured between SS (falling) and GD2 (falling)	250	500	750	ns
I_{SS}	Source current on SS pin	V_{SS} = 0.5 V	-225	-175	-125	µA
	Source current on SS pin	V_{SS} = 1.35 V	-5.5	-5	-4.5	

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ELECTRICAL CHARACTERISTICS (continued)

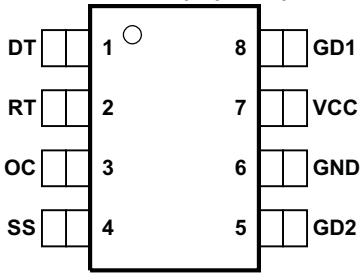
over operating free-air temperature range, −40°C < T_A < 125°C, T_J = T_A, V_{VCC} = 12 V, GND = 0 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, C_{VCC} = 1 μF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
PEAK CURRENT LIMIT						
$V_{OC1(off)}$	Level 1 over current threshold – V_{OC} rising		0.9	1	1.1	V
$V_{OC2(off)}$	Level 2 overcurrent latch threshold – V_{OC} rising		1.8	2.0	2.2	
$V_{OC1(on)}$	Level 1 over current threshold – V_{OC} falling		0.5	0.6	0.7	
t_{dOC}	Propagation delay		60	200	500	ns
I_{OC}	OC bias current	V_{OC} = 0.8 V	-200		200	nA
GATE DRIVE						
	GD1, GD2 output voltage high	I_{GD1} = −20 mA, I_{GD2} = −20 mA	9		11	V
	GD1, GD2 on-resistance high	I_{GD1} = −20 mA, I_{GD2} = −20 mA		12	30	Ω
	GD1, GD2 output voltage low	I_{GD1} = −20 mA, I_{GD2} = 20 mA		0.08	0.2	V
	GD1, GD2 on-resistance low	I_{GD1} = −20 mA, I_{GD2} = 20 mA		4	10	Ω
t_{RISE}	Rise time GDx	V_{VCC} rising from 1 V to 9 V, C_{LOAD} = 1 nF		18	35	ns
t_{FALL}	Fall time GDx	V_{VCC} falling from 9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GD1, GD2 output voltage during UVLO	V_{VCC} = 6 V, I_{GD1} = 1.2 mA, I_{GD2} = 1.2 mA	0.5		1.75	V
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			160		°C
	Thermal shutdown recovery threshold			140		

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DEVICE INFORMATION

TPS92020 (Top View)

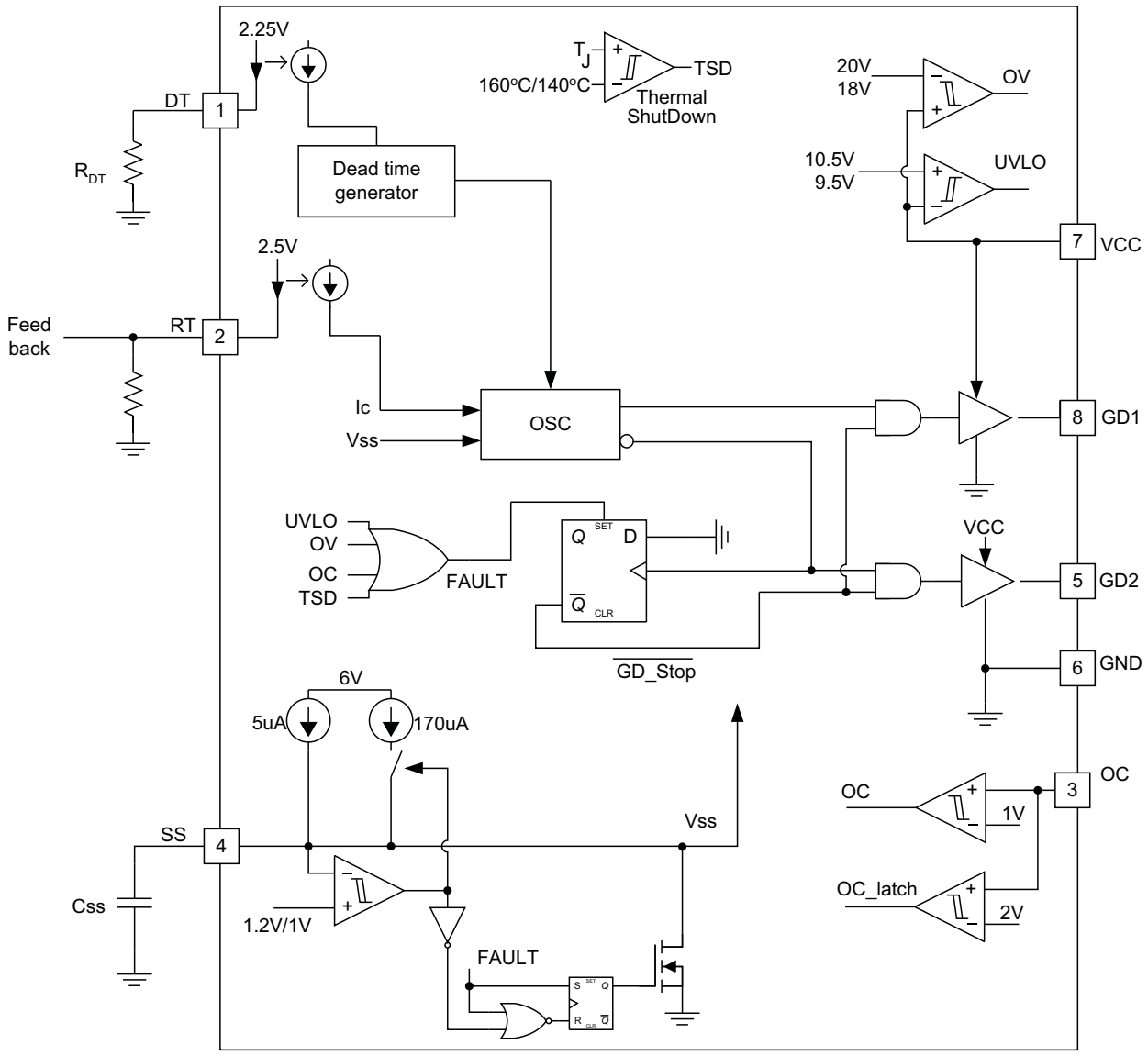


TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
DT	1	I	Sets the dead time of high-side and low-side switch driving signals. Connect a resistor to ground. With internal 2.25-V voltage reference, the current flowing through the resistor sets the dead time. To prevent shoot through when this pin is accidentally short to ground, the minimum dead time is set to 120 ns. Any dead time setting less than 120 ns defaults to 120-ns dead time.
GD1	8	O	High-side and low-side switch gate driver. Connect gate driver transformer primary side to these two pins to drive the half bridge.
GD2	5	O	
GND	6	-	Ground.
OC	3	I	Overcurrent protection. When the voltage on this pin is above 1 V, gate driver signals are actively pulled low. After the voltage falls below 0.6 V, the gate driver signal recovers with soft start. When OC pin voltage is above 2 V, the device is latched off. Bringing VCC below UVLO level resets the overcurrent latch off.
RT	2	I	The current flowing out of this pin sets the frequency of the gate driver signals. Connect the opto-coupler collector to this pin to control the switching frequency for regulation purpose. Parallel a resistor to ground to set the minimum current flowing out of the pin and set the minimum switching frequency. To set the maximum switching frequency limiting, place a resistor in series with the opto-coupler transistor. This resistor sets the maximum current flowing out of the pin and limits the maximum switching frequency.
SS	4	I	Soft-start. This pin sets the soft-start time of the system. Connect a capacitor to ground. Pulling this pin below 1 V disables the device to allow easy ON/OFF control. The soft-start function is enabled after all fault conditions, including bias supply OV, UVLO, overcurrent protection and over-temperature protection.
VCC	7	-	Bias supply. Connect this pin to a power supply less than 20 V. Place a 1-μF capacitor in parallel to ground to filter out noise.

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BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS

At V_{VCC} = 12 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, V_{SS} = 5 V, V_{OC} = 0 V; all voltages are with respect to GND, T_J = T_A = 25°C, unless otherwise noted.

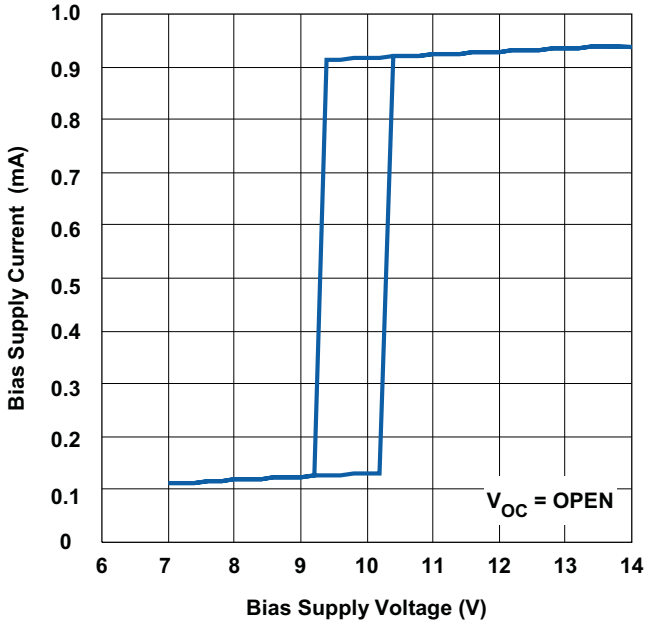


Figure 1. Bias Supply Current vs. Bias Supply Voltage

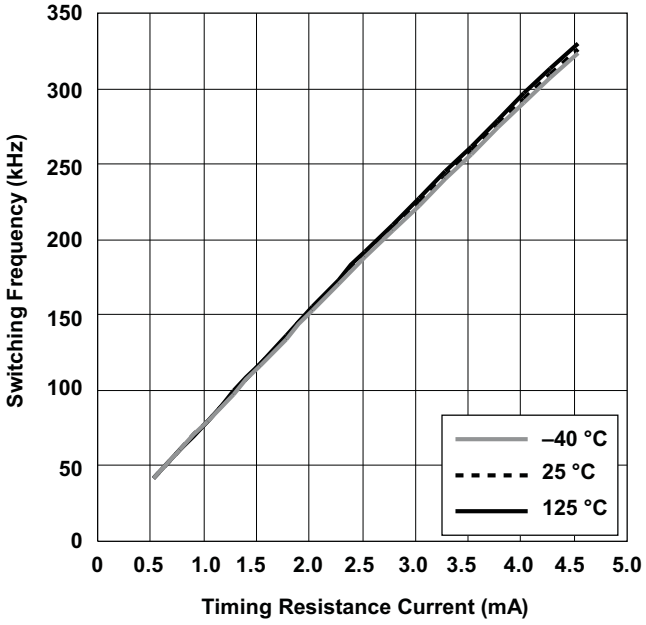


Figure 2. Switching Frequency vs. Timing Resistance

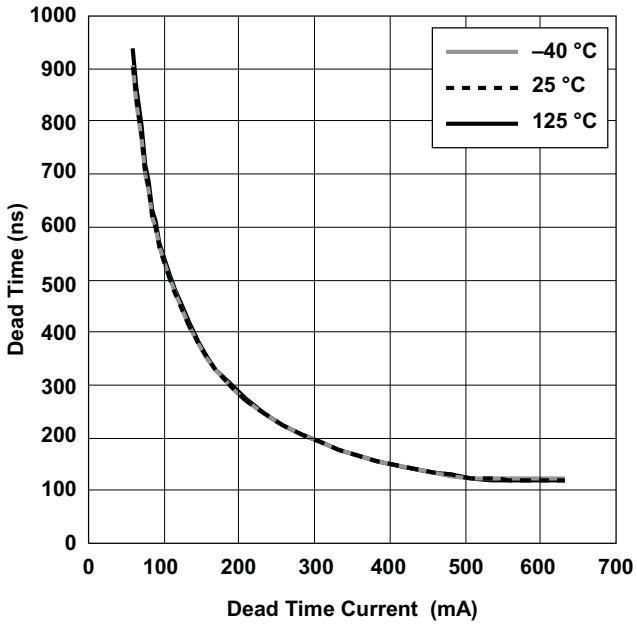


Figure 3. Dead Time vs. Dead Time Current

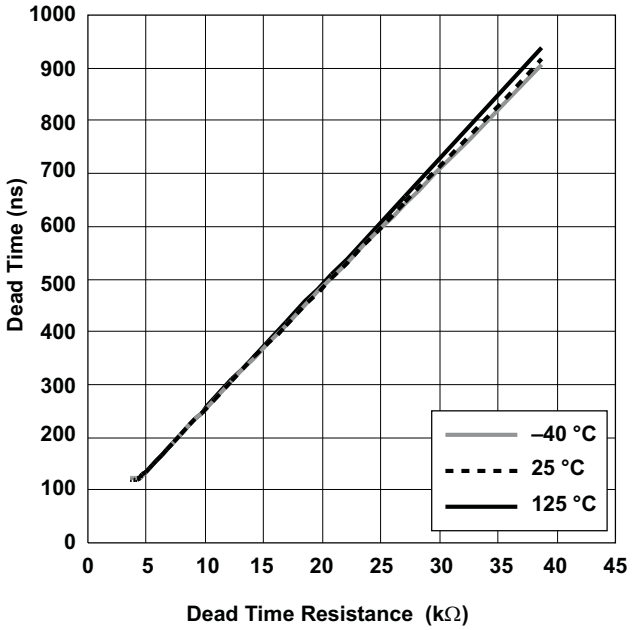


Figure 4. Dead Time vs. Dead Time Resistance

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TYPICAL CHARACTERISTICS (continued)

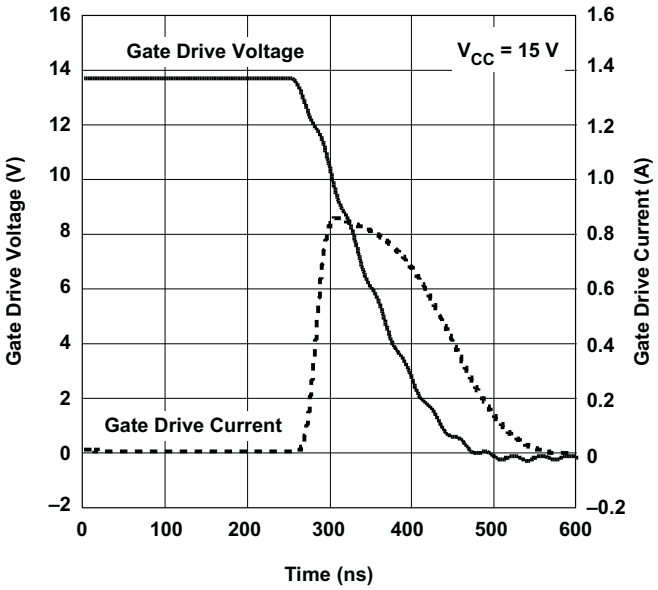


Figure 5. Gate Drive Voltage vs. Gate Drive Current vs. Time

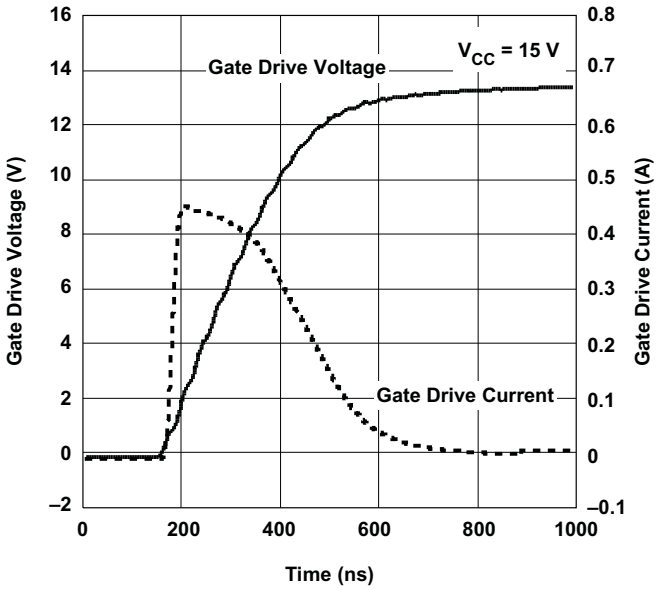


Figure 6. Gate Drive Voltage vs. Gate Drive Current vs. Time

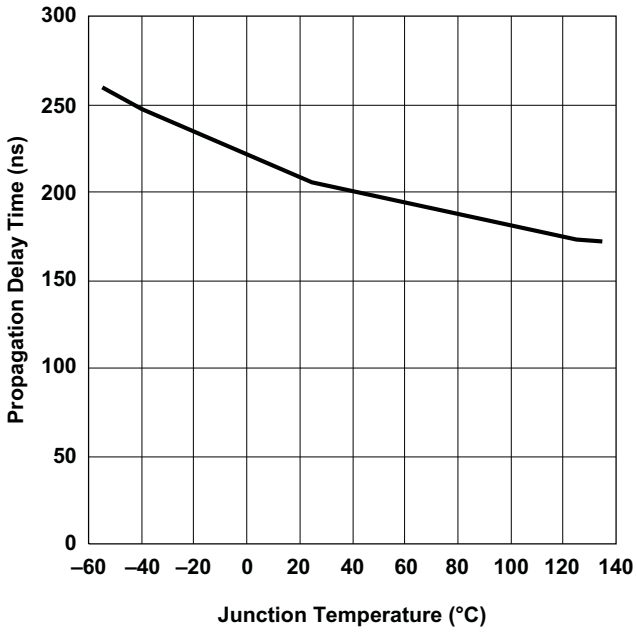


Figure 7. Propagation Delay Time vs. Temperature

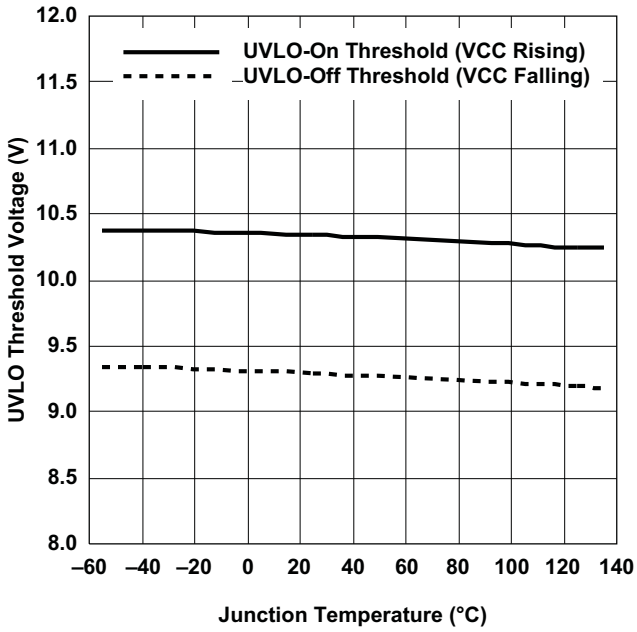


Figure 8. UVLO Threshold Voltage vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

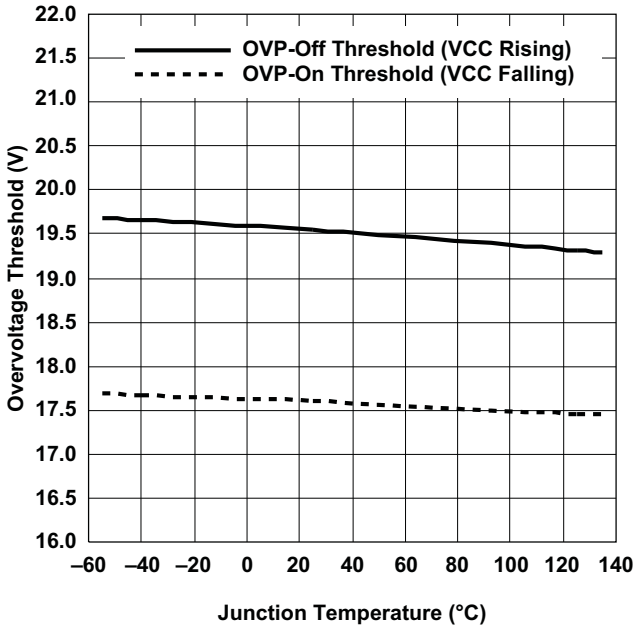


Figure 9. Overvoltage Threshold vs. Temperature

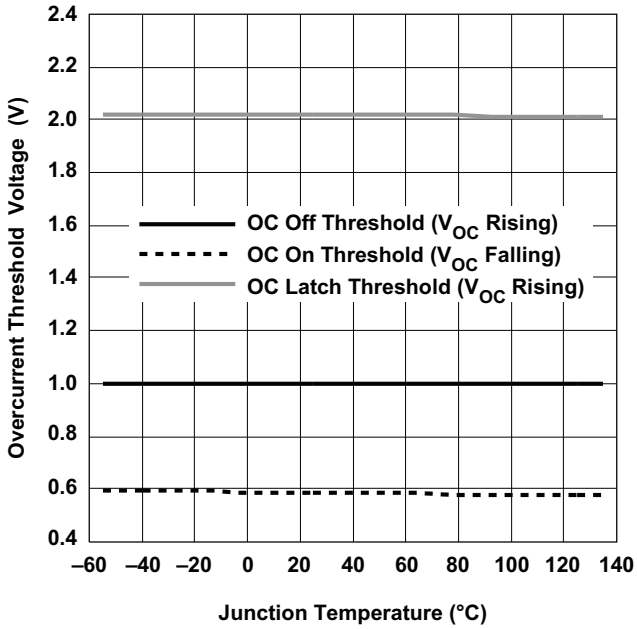


Figure 10. Overcurrent Threshold Voltage vs. Temperature

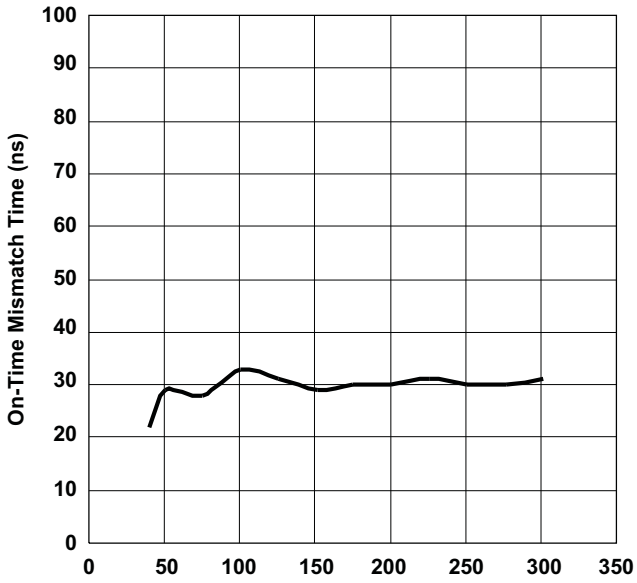


Figure 11. On-Time Mismatch vs. Switching Frequency

APPLICATION INFORMATION

Principle of Operation

The soft-switching capability, high efficiency and long holdup time make the LLC resonant converter attractive for many applications, such as digital TV, ac/dc adapters and computer power supplies. Figure 12 shows the schematic of the LLC resonant converter.

The LLC resonant converter is based on the series resonant converter (SRC). By using the transformer magnetizing inductor, zero-voltage switching can be achieved over a wide range of input voltage and load. As a result of multiple resonances, zero-voltage switching can be maintained even when the switching frequency is higher or lower than resonant frequency. This simplifies the converter design to avoid the zero-current switching region, which can lead to system damage. The converter achieves the best efficiency when operated close to its resonant frequency at a nominal input voltage. As the switching frequency is lowered the voltage gain is significantly increased. This allows the converter to maintain regulation when the input voltage falls low. These features make the converter ideally suited to operate from the output of a high-voltage boost PFC pre-regulator, allowing it to hold up through brief periods of ac line-voltage dropout.

Due to the nature of resonant converter, all the voltages and currents on the resonant components are approximately sinusoidal. The gain characteristic of LLC resonant converter is analyzed based on the First Harmonic Approximation (FHA), which means all the voltages and currents are treated as sinusoidal shape with the frequency same as switching frequency.

According to the operation principle of the converter, the LLC resonant converter can be draw as the equivalent circuit as shown in Figure 13.

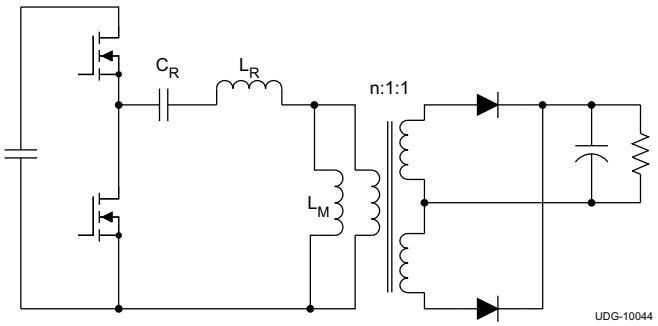


Figure 12. LLC Resonant Converter

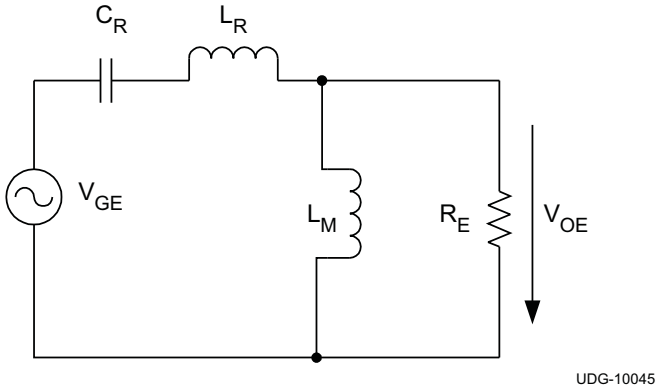


Figure 13. LLC Resonant Converter Equivalent Circuit

In this equivalent circuit, the V_{ge} and V_{oe} are the fundamental harmonics of the voltage generated by the half bridge and the voltage on the transformer primary side, respectively. These voltages can be calculated through Fourier analysis. The load resistor R_e is the equivalent resistor of the load, and it can be calculated as:

$$R_E = \left(\frac{8}{(\pi)^2}\right) \times (n)^2 \times R \tag{1}$$

Based on this equivalent circuit, the converter gain at different switching frequencies can be calculated as:

$$\left(\frac{V_{OUT}}{\left(\frac{V_{DC}}{2}\right)}\right) = \left| \frac{\frac{j\omega \times L_M \times R_E}{(j\omega \times L_M) + R_E}}{\frac{j\omega \times L_M \times R_E}{(j\omega \times L_M) + R_E} + \frac{1}{j\omega \times C_R} + j\omega \times L_R} \right| \tag{2}$$

where

- $V_{DC}/2$ is the equivalent input voltage due to the half-bridge structure

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Table 2. Circuit Definition Calculations

NORMALIZED GAIN	RESONANT FREQUENCY	QUALITY FACTOR	NORMALIZED FREQUENCY	INDUCTOR RATIO
$M = \left(\frac{V_{OUT}}{\left(\frac{V_{DC}}{2} \right)} \right)$ (3)	$f_0 = \frac{1}{2\pi \times \sqrt{L_R \times C_R}}$ (4)	$Q_E = \frac{\sqrt{L_R / C_R}}{R_E}$ (5)	$f_n = \left(\frac{f}{f_0} \right)$ (6)	$L_n = \left(\frac{L_M}{L_R} \right)$ (7)

Following the definitions in Table 2, the converter gain at different switching frequencies can be calculated in Equation 8.

$$M = \frac{L_n \times (f_n)^2}{L_n \times (f_n)^2 + (f_n - 1) \times (f_n + 1 + j \times f_n \times L_n \times Q_e)}$$

where

- M is the converter voltage gain
- Ln is the ratio of the magnetizing inductance to the resonant inductance
- f_n is the normalized switching frequency
- Q_e is the quality factor (8)

Because of the FHA, Equation 8 is an approximation. When the switching frequency moves away from the resonant frequency, the error becomes larger. However, this equation can be used as the design tool. The final results need to be verified by the time based simulation or hardware test.

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From Equation 8, when switching frequency is equal to resonant frequency, f_n = 1 and converter voltage gain is equal to 1. Converter gain at different loads and inductor ratio conditions are shown in Figure 14 through Figure 17.

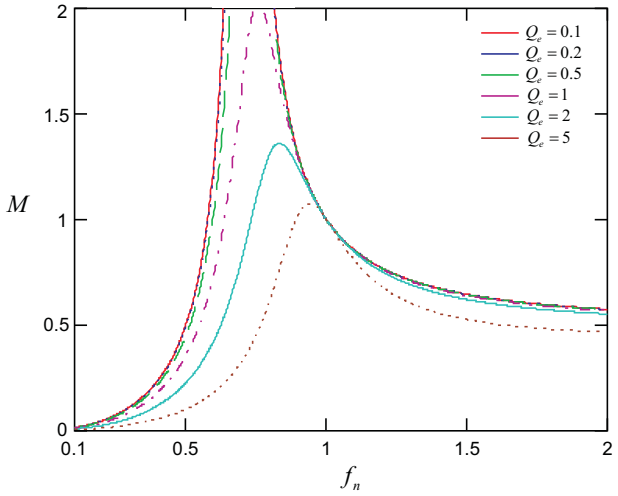


Figure 14. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=1

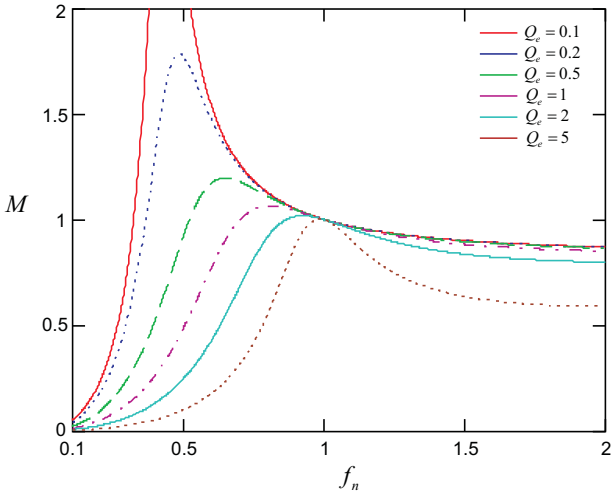


Figure 15. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=5

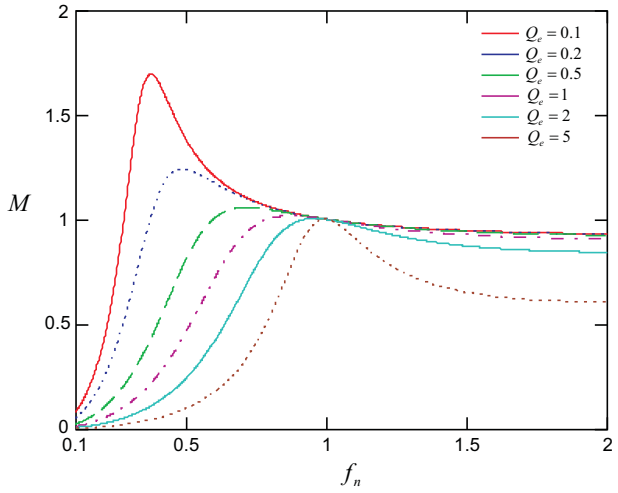


Figure 16. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=10

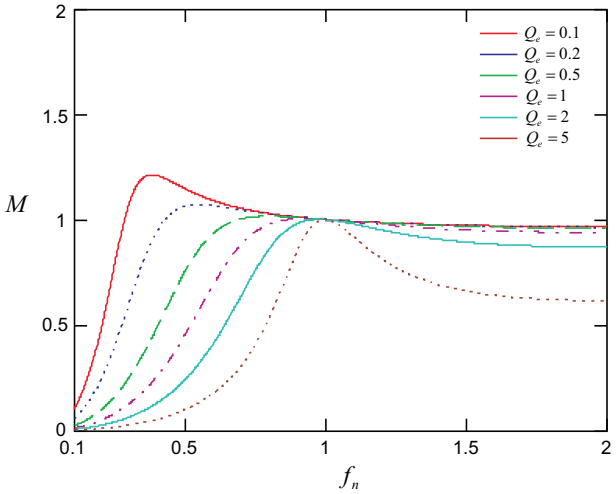


Figure 17. Normalized Switching Frequency vs.Converter Voltage Gain, Ln=20

Based on its theory of operation the LLC resonant converter is controlled through Pulse Frequency Modulation (PFM). The output voltage is regulated by adjusting the switching frequency according to the input and output conditions. Optimal efficiency is achieved at the nominal input voltage by setting the switching frequency close to the resonant frequency. When the input voltage droops low the switching frequency is decreased to boost the gain and maintain regulation.

The TPS92020 resonant half-bridge controller uses variable switching frequency control to adjust the resonant tank impedance and regulate output voltage. This 8-pin package device integrates the critical functions for optimizing the system performance while greatly simplifying the design and layout.

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Adjustable Dead Time

Resonant half-bridge converter relies on the resonant tank current at MOSFETs turn-off to achieve soft switching and reduce switching loss. Higher turn-off current provides more energy to discharge the junction capacitor, while it generates more turn-off loss. Smaller turn-off current reduces turn-off loss, but it requires longer time to discharge MOSFETs junction capacitors and achieve soft switching. By choosing an appropriate dead time, turn-off current is minimized while still maintaining zero-voltage switching, and best system performance is realized.

In TPS92020, dead time can be adjusted through a single resistor from DT pin to ground. With internal 2.25-V voltage reference, the current flow through the resistor sets the dead time.

$$t_D = 20\,ns + R_{DT} \times 24\,ns \tag{9}$$

To prevent shoot through when the DT pin accidentally connects to ground, the two gate driver outputs limit the dead-time to a minimum of 120-ns. Any dead-time setting less than 120-ns, defaults to the minimum 120-ns limit.

Oscillator

With variable switching frequency control, TPS92020 relies on the internal oscillator to vary the switching frequency. The oscillator is controlled by the current flowing out of RT pin. Except during soft start, the relationship between the gate signal frequency and the current flowing out of RT pin can be represented in Equation 10.

$$f_{SW} = \frac{1}{2} \times \frac{1}{\left(\frac{6\,ns \times 1A}{I_{RT}}\right) + 150\,ns} \approx I_{RT} \times 83\,Hz/\mu A \tag{10}$$

Since the switching frequency is proportional to the current, by limiting the maximum and minimum current flowing out of RT pin, the minimum and maximum switching frequency of the converter could be easily limited. As shown in Figure 18, putting a resistor from RT pin to ground limits the minimum current and putting a resistor in series with the opto-coupler limits the maximum current.

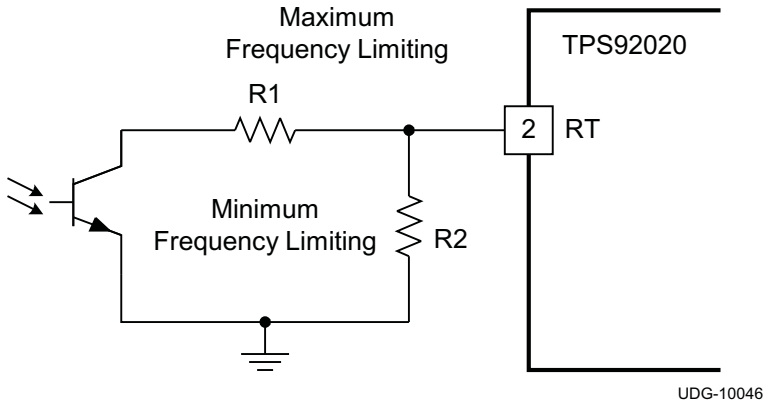


Figure 18. Maximum and Minimum Frequency Setting for TPS92020

The frequency limiting resistor can be calculated in Equation 11 through Equation 14.

$$I_{F(max)} = \frac{6\,ns}{\left(\frac{1}{(2 \times f_{MAX})}\right) - 150\,ns} \tag{11}$$

$$I_{F(max)} = 2.5\,V\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{12}$$

$$I_{F(min)} = \frac{6\,ns}{\left(\frac{1}{(2 \times f_{MIN})}\right) - 150\,ns} \tag{13}$$

$$I_{F(min)} = \frac{2.5\,V}{R_2} \tag{14}$$

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Soft Start

During start up and fault recovery conditions, soft start is always implemented to prevent excessive resonant tank current and ensure Zero-Voltage Switching (ZVS). During soft start, the switching frequency is increased. The soft-start time can be programmed by placing a capacitor from SS pin to ground.

The soft-start pin also serves as an ON/OFF control pin of the device. By actively pulling the SS pin below 1 V, the device is disabled. When the pull down is removed, SS pin voltage is increased because of internal charging current. Once SS pin becomes above 1.2 V, the device starts to generated gate-driver signal and enters soft-start mode. The time sequence of soft start is shown in Figure 19.

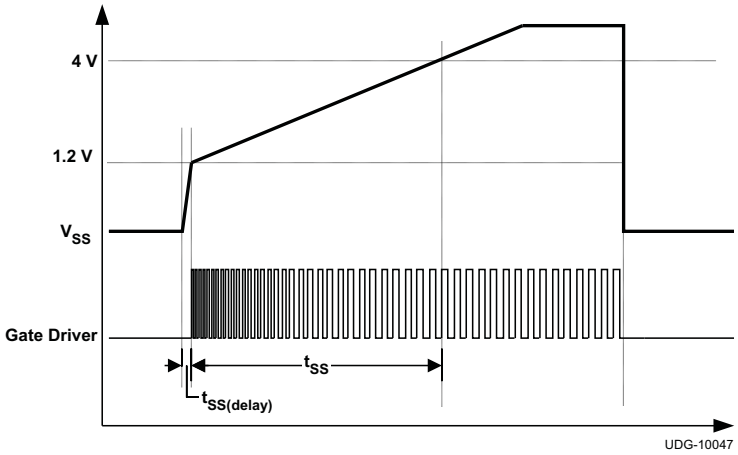


Figure 19. Soft-Start Sequence

To prevent a long delay between the ON command and appearance of a gate driver signal, the SS pin current is set as two different levels. When SS pin voltage is below 1.2 V, its output current is 175 μA. This high current could charge the soft-start pin capacitor to 1.2 V in a short period of time, and reduces the time delay. This time delay is calculated in Equation 15.

$$t_{SS(delay)} = \frac{1.2\,V}{175\,\mu A} \times C_{SS} \tag{15}$$

The switching frequency during soft start is determined by both the current flowing out of the RT pin and the voltage on SS pin. The switching frequency can be calculated based on the Equation 16.

$$f_{SW} = \frac{1}{2} \times \frac{1}{\frac{6\,ns \times 1A}{I_{RT} + \left(1.81mA - \frac{V_{VSS}}{2.2k\Omega}\right)} + 150\,ns} \tag{16}$$

After SS pin voltage reaches 4 V, soft-start period is finished and switching frequency becomes the same as demanded by the RT pin current. The time used to charge SS pin from 1.2 V to 4 V is defined as soft-start time and can be calculated in Equation 17.

$$t_{SS} = \frac{2.8\,V}{5\,\mu A} \times C_{SS} \tag{17}$$

To ensure reliable operation, the gate drivers restart with GD2 turning high. This prevents uncertainty during system start up.

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Burst-Mode Operation

During light load condition, the resonant converter tends to increase its switching frequency and maintain the output voltage regulation. However, due to ringing caused by transformer parasitic capacitor and the rectification-diode-junction capacitors, the energy could be directly transferred to the load through these capacitors. When this power becomes more than the load requires, output voltage become higher than the regulation level. In this case, further increasing the switching frequency will not help the situation because energy transfer to the load is not through the power stage itself.

To prevent output over voltage during this condition, the TPS92020 includes the burst-mode operation function. When the control loop demands switching frequency higher than 350 kHz, the gate driver is disabled and the power stage stops switching. When the output voltage drops, the control loop begins to demand switching frequency less than 330 kHz, the gate driver recovers and the power stage begins to deliver power again. This allows output voltage to be regulated.

This burst mode can be easily disabled by limiting the maximum switching frequency to less than 350 kHz. In this way, the control loop never demands a switching frequency higher than 350 kHz and as a result, burst mode operation does not occur.

Overcurrent Protection

To prevent power stage failure under excessive load current condition, the TPS92020 includes an overcurrent protection function. With a dedicated OC pin, the power stage is shut down when OC pin voltage is above 1 V. Once the OC pin voltage falls below 0.6 V, the gate driver recovers with a soft start. To enhance system safety, the TPS92020 latches up the entire system when the OC pin voltage rises above 2 V. Bringing the VCC voltage below the UVLO voltage level resets the device.

The current can be indirectly sensed through the voltage across resonant capacitor by using the sensing network shown in Figure 20.

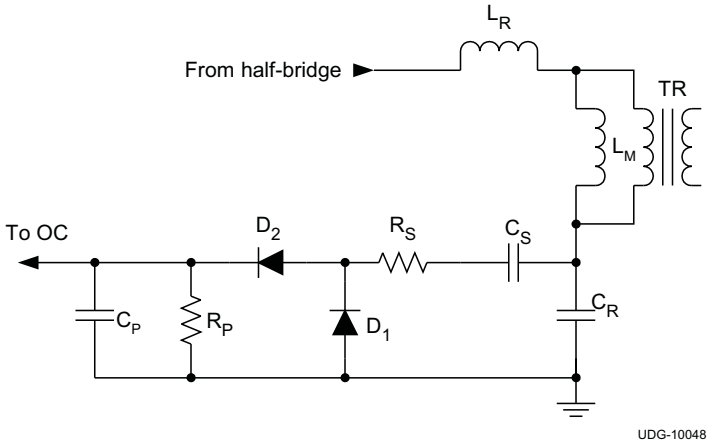


Figure 20. Current Sensing for LLC Resonant Converter

The general concept of this sensing method is that the ac voltage across the resonant capacitor is proportional to load current.

According to the FHA model, peak voltage of the ac component on the resonant capacitor can be calculated in Equation 18.

$$V_{CR(pk)} = \frac{4}{\pi} \times n \times V_{OUT} \left| \frac{j\omega_n \times L_n \times (Q_e + 1)}{(\omega_n)^2 \times L_n} \right| \quad (18)$$

Therefore, the resonant capacitor voltage reaches its maximum value at the minimum switching frequency and maximum load. According to Equation 18, the current sensing network components can be calculated. Due to the nature of FHA, the final circuit parameters must be verified through actual hardware test.

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Table 3. Calculated Current Sensing Network Components

SYMBOL	FUNCTION	DESIGN EQUATION
R_S	Transfer ac voltage across resonant capacitor into current source	$R_s = \frac{\left(V_{CR(pk)MAX}\right)^2}{2 \times P_{RS(max)}}$ (19)
C_S	Blocking dc voltage on resonant capacitor	$C_S = \frac{10}{R_S \times f_{MIN}}$ (20)
R_P	Load resistor of the current source	$R_P = \frac{R_S}{V_{CR(pk)MAX}} \times \frac{\pi}{2}$ (21)
C_P	Filter capacitor	$C_P = \frac{10}{(R_P \times f_{MIN})}$ (22)

Gate Driver

Half-bridge resonant converter is controlled by the nearly 50% duty cycle variable frequency square wave voltage. This allows the half bridge to be easily driven by the gate-driver transformer. Compared with a half-bridge driver device, a gate-driver transformer provides a simple and reliable solution, which:

- Eliminate the need for gate driver power supply
- Enable simplified layout
- Preventing shoot through due to the transformer coupling
- No latch up

The TPS92020 integrates two-gate drivers with 0.4-A source and 0.8-A sink capability to directly drive the gate driver transformer.

For LLC resonant converter, it is critical for the gate-driver signal to be precisely symmetrical. Otherwise, the resonant tank operation will be symmetrical. The load current distribution will be unbalanced for the output rectifiers, which in turn requires over design of the power stages and thermal management.

In TPS92020, the gate-driver output is precisely trimmed to have less than 50 ns mismatch. Although the gate-driver signal is quite symmetrical, it is still recommended to insert the dc blocking capacitor in the gate-driver transformer primary side to prevent transformer saturation during fast transients.

VCC Pin

Connect a regulated bias supply to VCC pin. When VCC becomes above 10.5 V the device is enabled and after all fault conditions are cleared the gate driver starts with soft start. When the VCC voltage drops below 9.5 V, the device enters UVLO protection mode and both gate drivers are actively pulled low. When VCC rises above 20 V the device enters VCC overvoltage protection mode and the device is disabled with both gate drivers actively pulled low. VCC over-voltage protection will recover with soft start when the VCC voltage returns below 18 V.

Over-Temperature Protection

TPS92020 continuously senses its junction temperature. When the junction temperature rises above 160°C the device enters over-temperature protection mode with both gate drivers actively pulled low. When junction temperature drops below 140°C, gate driver restarts with soft start.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92020D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92020D	Samples
TPS92020DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	92020D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

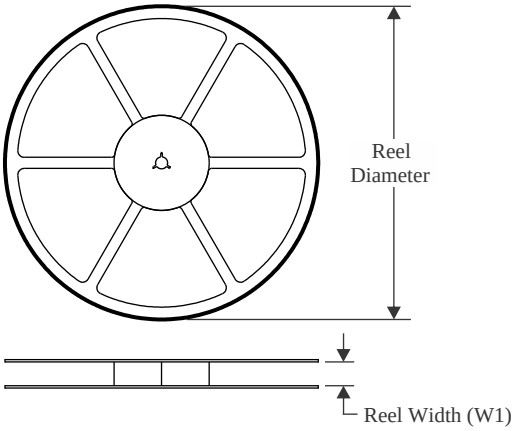
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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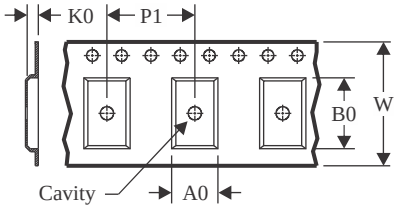
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

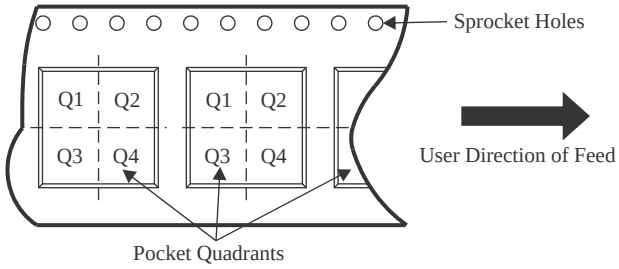


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

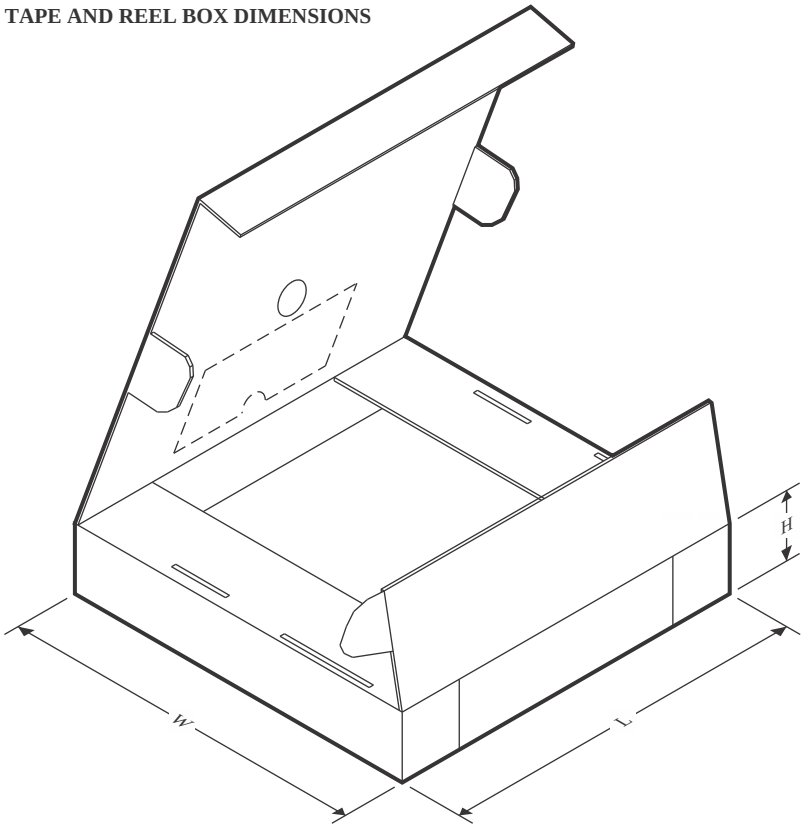
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92020DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

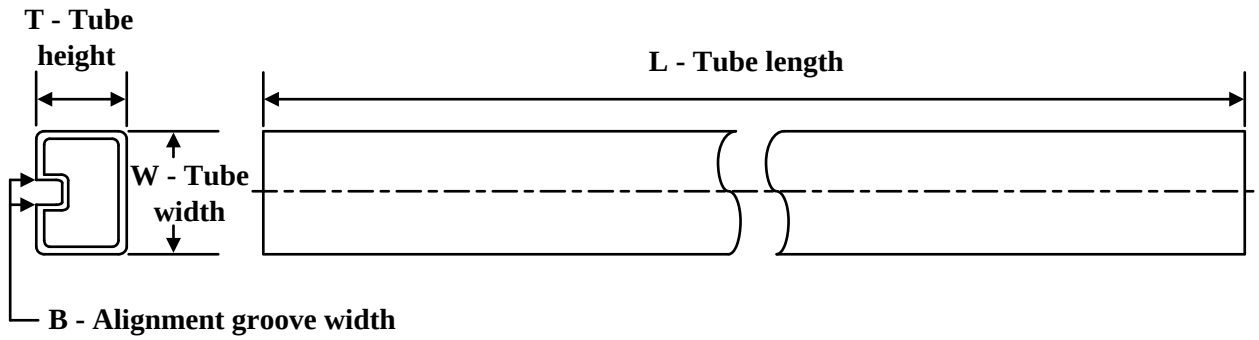
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

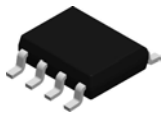
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92020DR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92020D	D	SOIC	8	75	506.6	8	3940	4.32

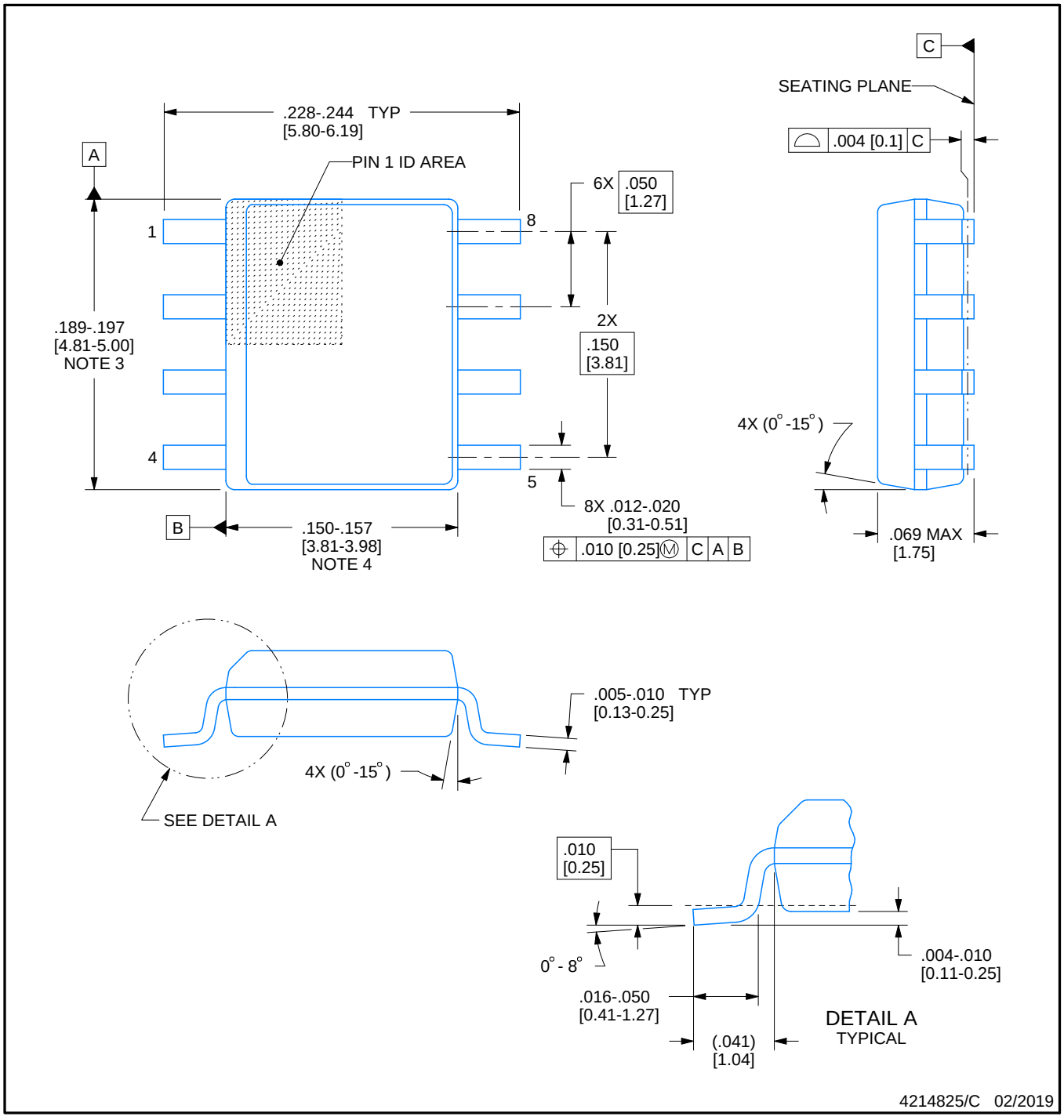


PACKAGE OUTLINE

D0008A

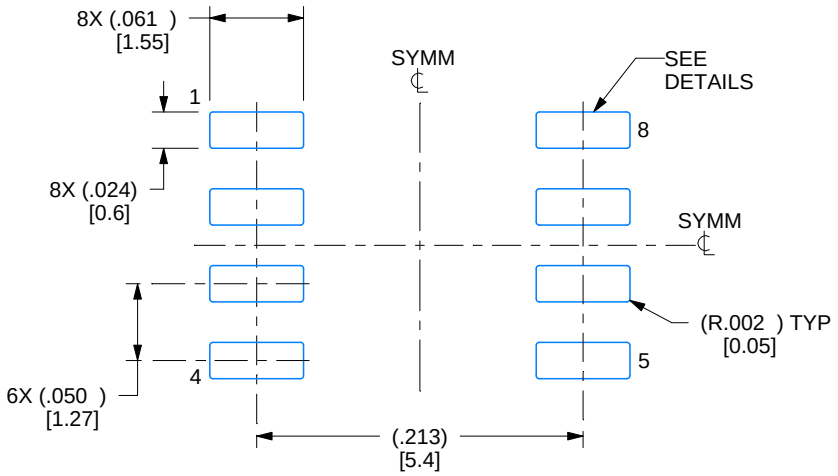
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

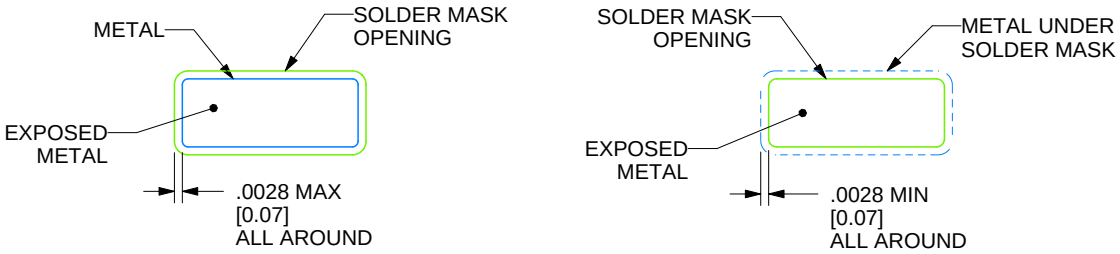


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

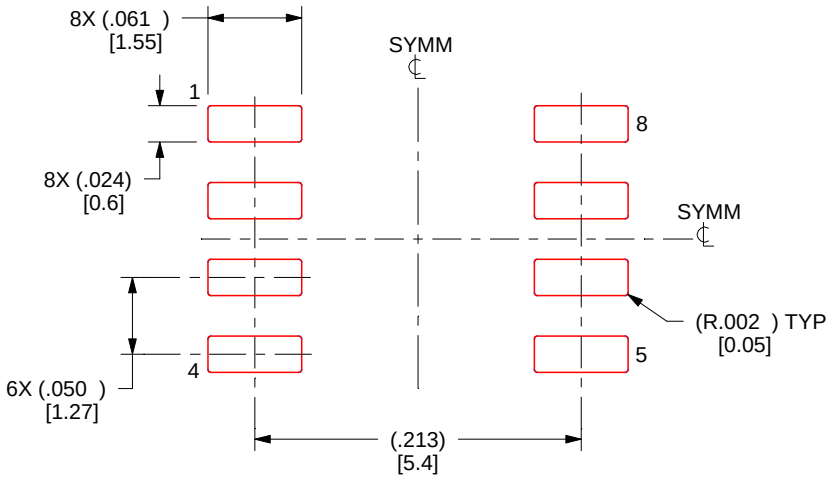
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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