BGF128

HDMI Interface ESD Protection

RF & Protection Devices

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BGF128

Revision History: 2009-04-01, V2.1

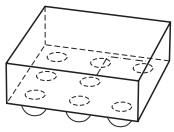
Previous Version: 2009-03-02, V2.0

Page	Subjects (major changes since last revision)
4	Marking updated
6	**Figure 3** added

BGF128

Features

- ESD protection circuit for control data lines of an HDMI interface
- ESD protection according to IEC61000-4-2 for ±15 kV contact discharge on external IOs
- Wafer level package with SnAgCu solder balls
- 400 µm solder ball pitch
- RoHS and WEEE compliant package



WLP-8-9-N-3D

RoHS

Description

BGF128 is an ESD protection circuit for control data lines of an HDMI interface. All external IOs are protected against ESD pulses of ±15 kV contact discharge according to IEC61000-4-2. The wafer level package is a green lead-free and halogen-free package with a size of only 1.15 mm x 1.15 mm and a total height of 0.6 mm.

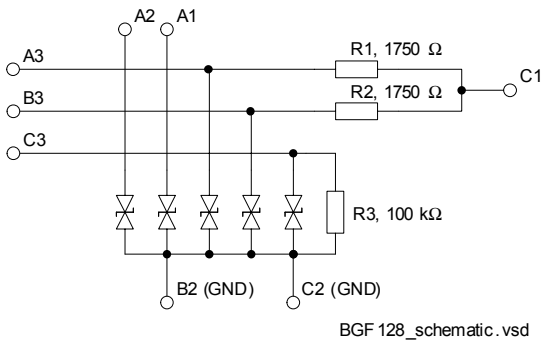


Figure 1 Schematic

Type	Package	Marking	Chip
BGF128	WLP-8-9	28	N0747

Table 1 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at all pins to GND	V_P	0	–	5	V	–
Operating temperature range	T_{OP}	-40	–	+85	°C	–
Storage temperature range	T_{STG}	-65	–	+150	°C	–
Summed up input power for all pins	P_{in}	–	–	60	mW	T_S < 70 °C
Electrostatic Discharge According to IEC61000-4-2						
Contact discharge at internal pin C1 to any other pin	V_{ESD}	-2	–	2	kV	–
Contact discharge at external pins A1, A2, A3, B3, C3 to GND	V_{ESD}	-15	–	15	kV	–

Table 2 Electrical Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistors R_1, R_2	$R_{1,2}$	1575	1750	1925	Ω	–
Resistor R_3	R_3	80	100	120	kΩ	–
Leakage current of ESD protection diodes	I_R	– –	1 2	100 200	nA nA	V = 3 V V = 5 V
Breakdown voltage of ESD diodes[2)]	$V_{(BR)}$	–	18.5 -12.5	–	V	$I_{(BR)}$ = 1 mA $I_{(BR)}$ = -1 mA
Line capacitance A1, A2, A3, B3, C3[3)]	C_T	8	10	12	pF	V = 0 V

1) at T_A = 25 °C
2) after snap-back
3) Capacitance measured from designated pin to GND. Pin C1 connected to GND.

Package Outlines

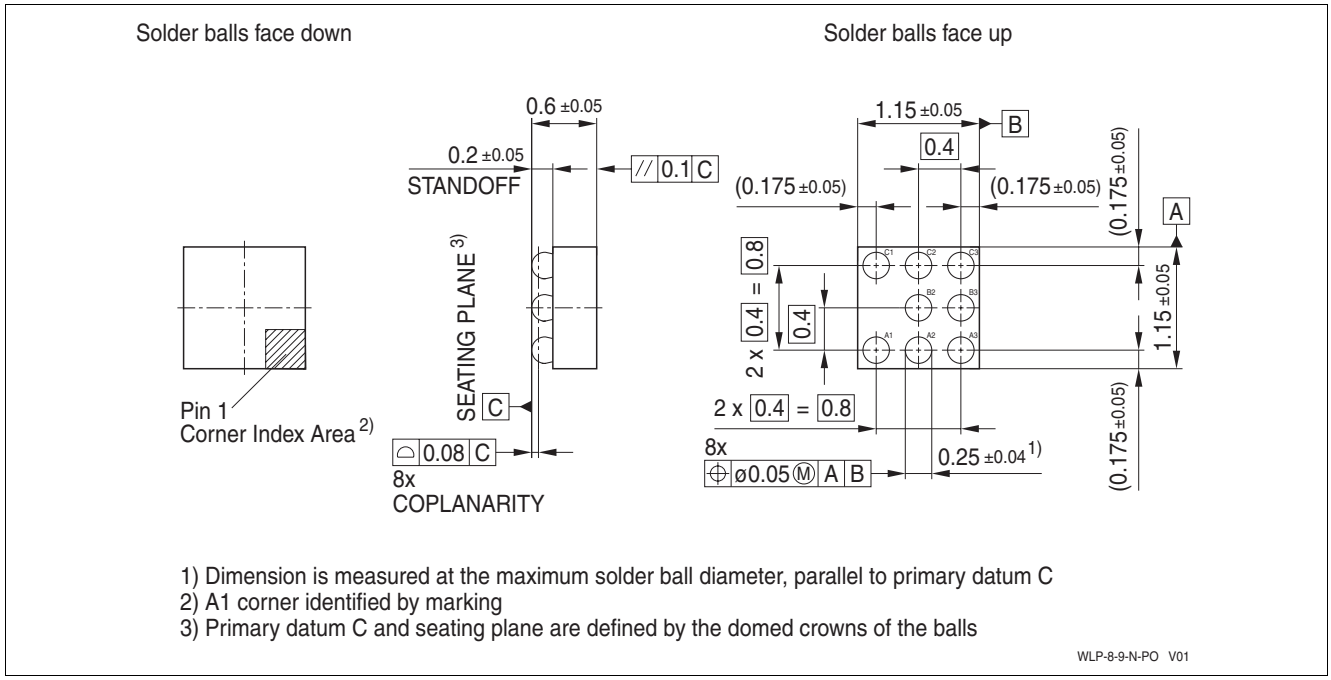


Figure 2 Package WLP-8-9

Footprint

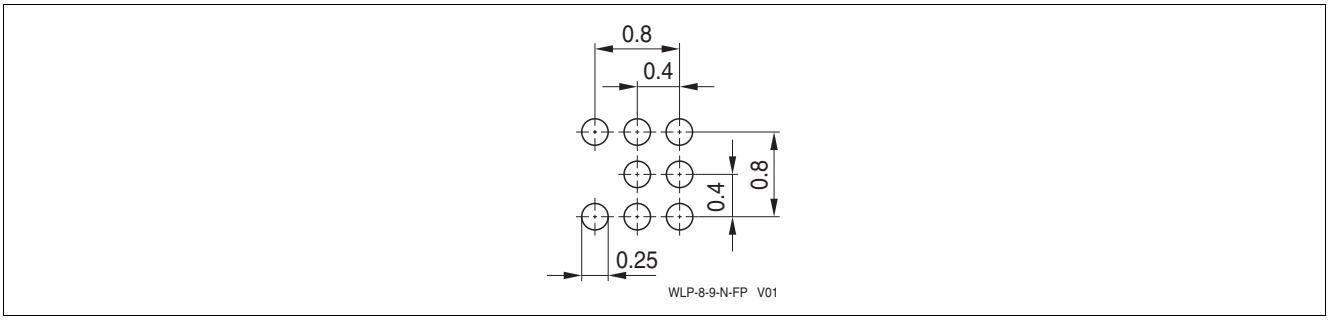


Figure 3 Recommended PCB pad design for reflow soldering

Tape

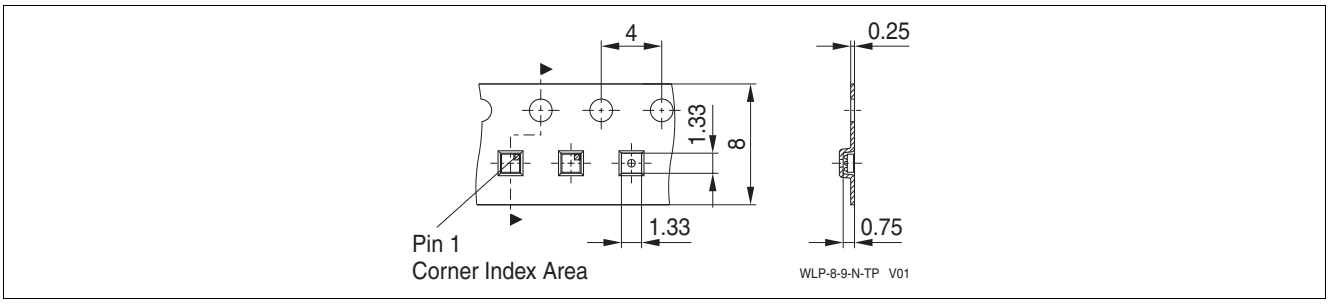


Figure 4 Tape for WLP-8-9

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