SONY

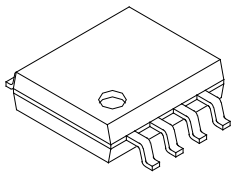
CXL5513M/P

CMOS-CCD 1H Delay Line for NTSC

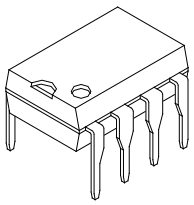
Description

The CXL5513M/P are CMOS-CCD delay line ICs designed for processing video signals. This ICs provide a 1 H delay time for NTSC chroma signals including the external lowpass filter.

CXL5513M
8 pin SOP (Plastic)



CXL5513P
8 pin DIP (Plastic)



Features

- Single 5 V power supply
- Low power consumption
- Built-in peripheral circuit
- Built-in tripling PLL circuit
- Center bias mode

Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5513M	350	mW
	CXL5513P	480	mW

Recommended Operating Range (Ta=25 ˚C)

V_{DD} 5 V±5 %

Recommended Clock Conditions (Ta=25 ˚C)

- Input clock amplitude V_{CLK} 400 mVp-p (Typ.)
- Clock frequency f_{CLK} 3.579545 MHz
- Input clock waveform Sine wave

Input Signal Amplitude

V_{SIG} 500 mVp-p (typ.), 572 mV_{P-P} (max.)

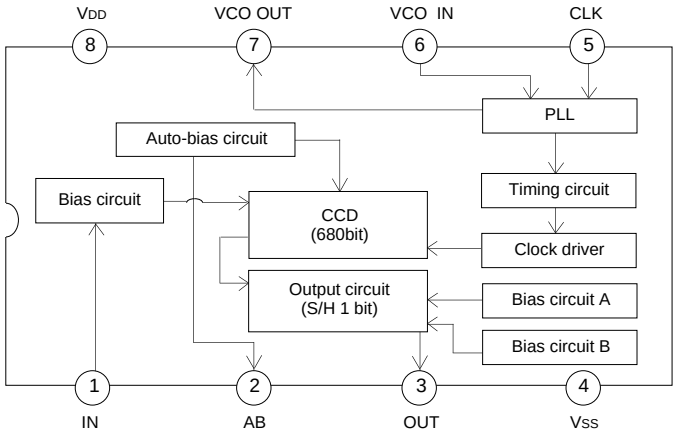
Functions

- 680-bit CCD register
- Clock driver
- Auto bias circuit
- Input center bias circuit.
- Sample and hold circuit
- Tripling PLL circuit
- Inverted output

Structure

CMOS-CCD

Block Diagram and Pin Configuration (Top View)



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E93Y20-TE

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	>10 KΩ
2	AB	O	Auto-bias DC output	
3	OUT	O	Signal output	40 to 500 Ω
4	V_{SS}	–	GND	
5	CLK	I	Clock input (fsc)	>10 KΩ
6	VCO IN	I	VCO input	
7	VCO OUT	O	VCO output (3fsc)	
8	V_{DD}	–	5 V power supply	

Electrical Characteristics

(Ta=25 °C, V_{DD}=5 V, f_{CLK}=3.579545 MHz, V_{CLK}=400mVp-p, sine wave)
See “Electrical Characteristics Test Circuit”.

Item	Symbol	Conditions	SW conditions		Min.	Typ.	Max.	Unit	Note
			1	2					
Supply current	I_{DD}	———	a	–	6	12	20	mA	1
Low frequency gain	GL	200 kHz 500mVp-p Sine wave	a	b	-2	0	2	dB	2
Frequency response	fR	200 kz ↔ 3.57 MHz 150mVp-p Sine wave	b ↔ c	b	–2.5	–1.5	–0.5	dB	3
Differential gain	DG	5-staircase wave (See Note 4.)	d	c	0	3	5	%	4
Differential phase	DP	5-staircase wave (See Note 4.)	d	c	0	3	5	degree	4
S/H pulse coupling	CP	No signal input	f	a	—	—	350	mVp-p	5
S/N ratio	SN	50 % white video signal (See Note 6.)	e	d	52	56	—	dB	6

NOTE

1 This is the IC supply current value during clock and signal input.

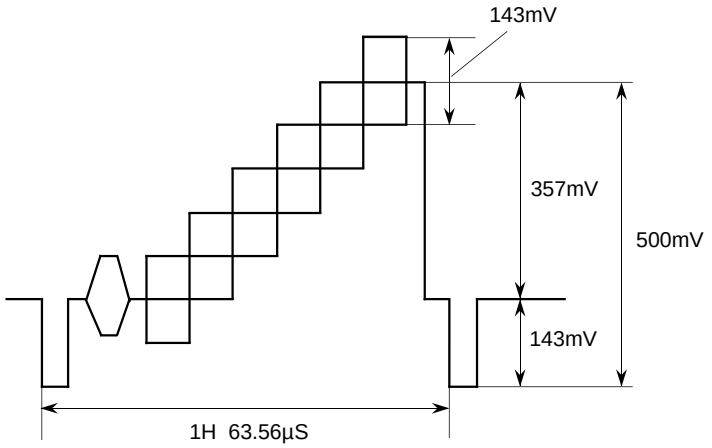
2 GL is the output gain of OUT pin when a 500 mVp-p, 200 kHz sine wave is fed to IN pin.

$$GL = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{500 \text{ [mVp-p]}} \text{ [dB]}$$

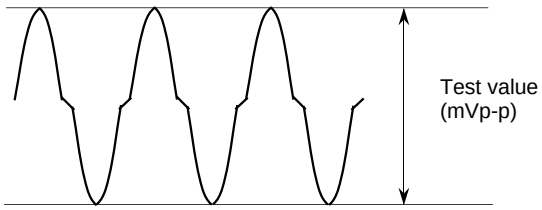
3 Indicates the dissipation at 3.58 MHz in relation to 200 kHz. From the output voltage at OUT pin when a 150 mVp-p, 200 kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150 mVp-p, 3.58 MHz sine wave is fed to the same, calculation is made according to the following formula.

$$fR = 20 \log \frac{\text{OUT pin output voltage (3.58 MHz) [mVp-p]}}{\text{OUT pin output voltage (200 kHz) [mVp-p]}} \text{ [dB]}$$

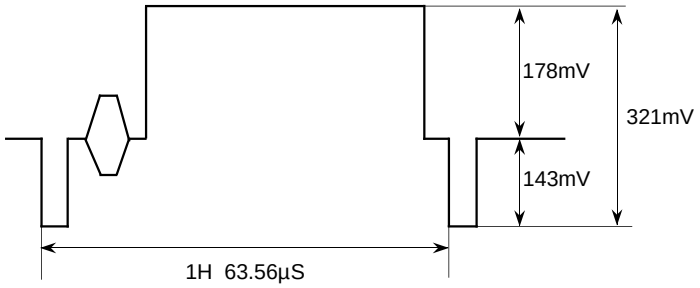
4 In Fig. below, the differential gain (DG) and the differential phase (DP), are tested with a vector scope when the 5-staircase wave is fed.



5 Leakage of internal clock components and related high frequency component to the output signal, during no signal input, is tested.

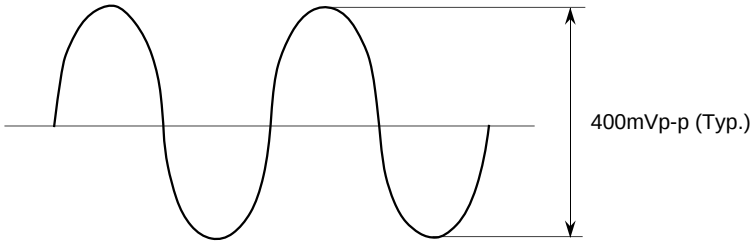


6 S/N ratio during a 50 % white video signal input shown in Fig. below is tested at the video noise meter, in BPF 100 kHz to 4 MHz, Sub Carrier Trap mode.

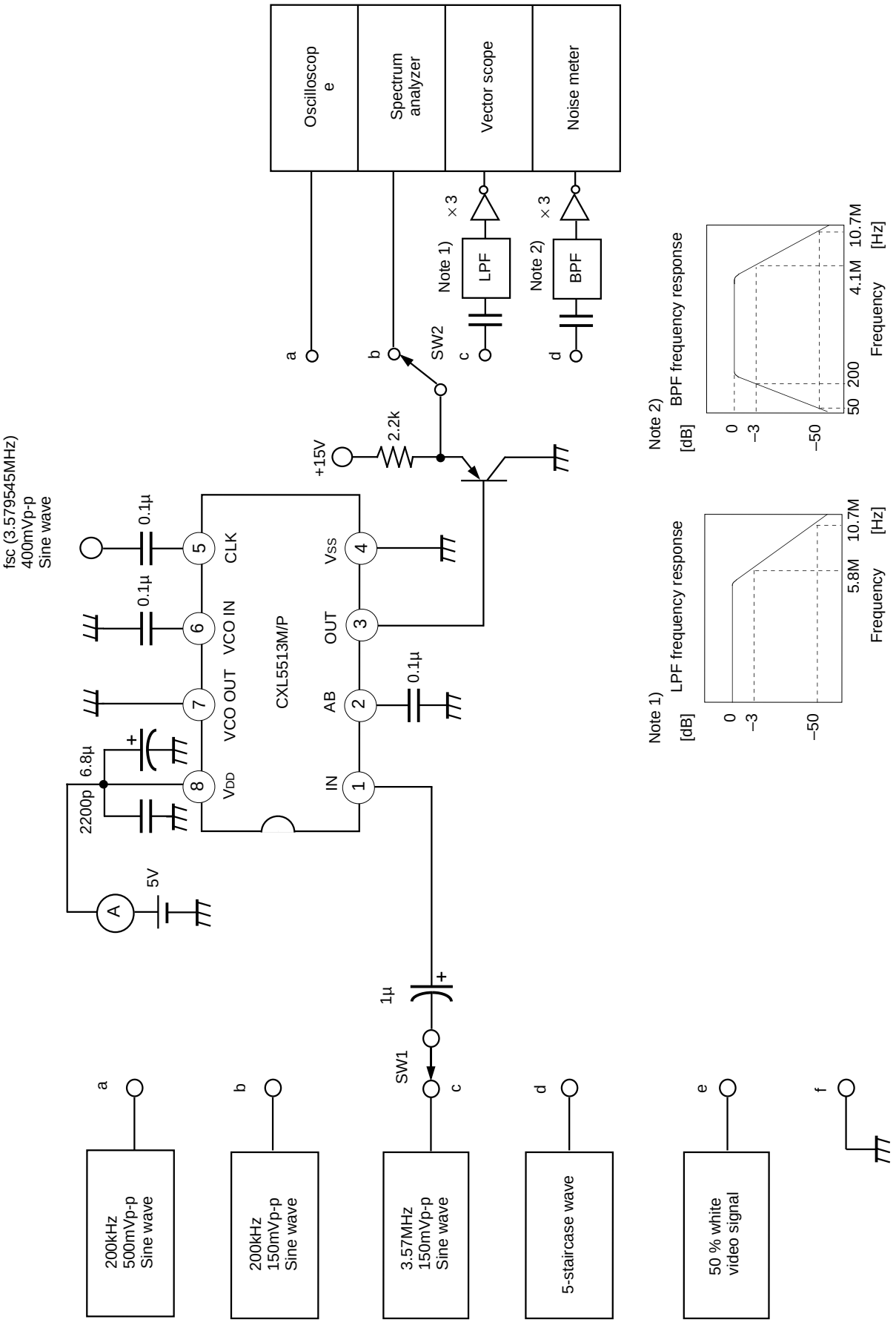


CLOCK

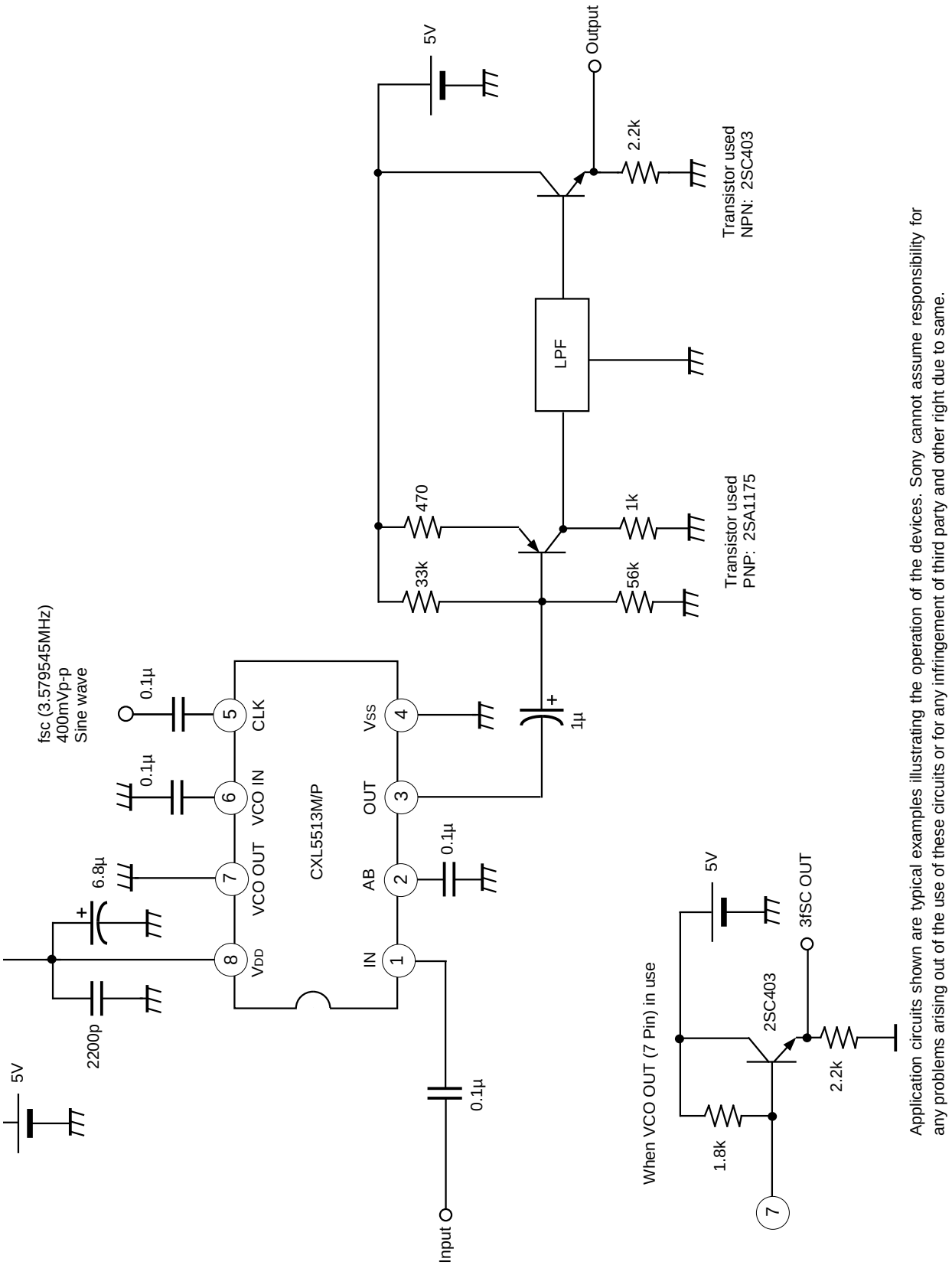
fSC (3.579545MHz) Sine wave



Electrical Characteristics Test Circuit

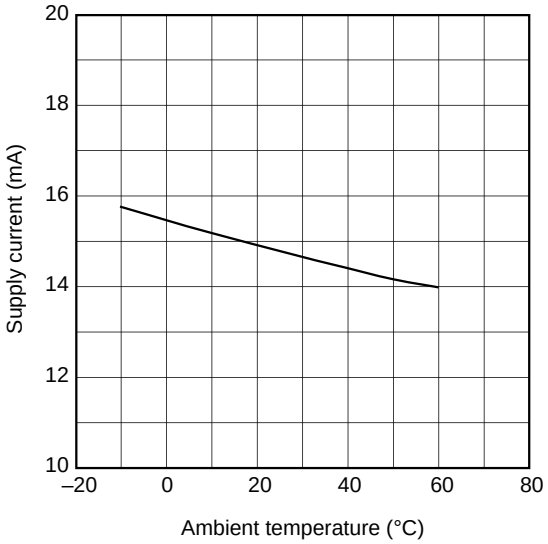


Application Circuit

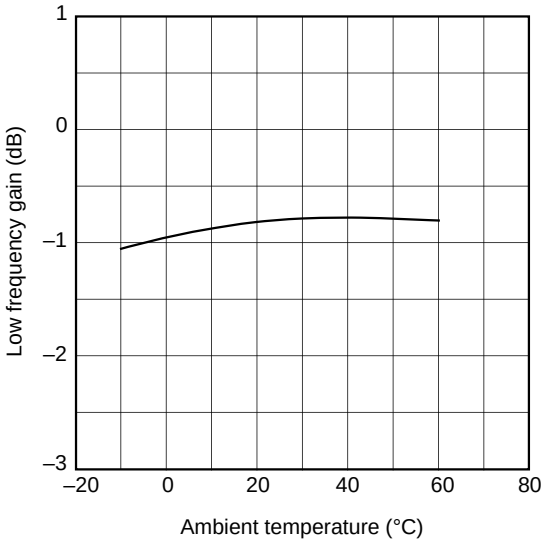


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

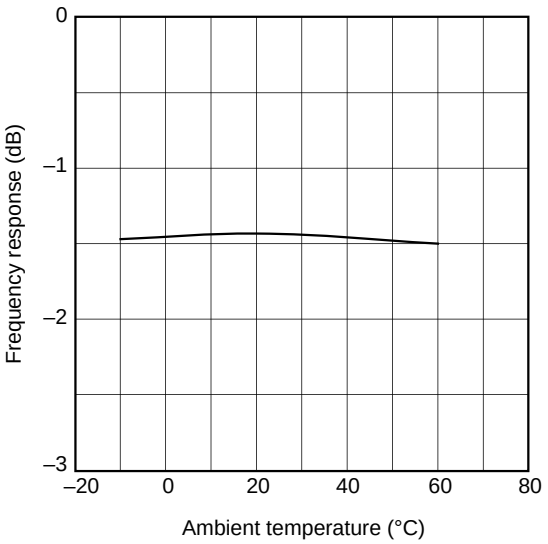
Supply current vs. Ambient temperature



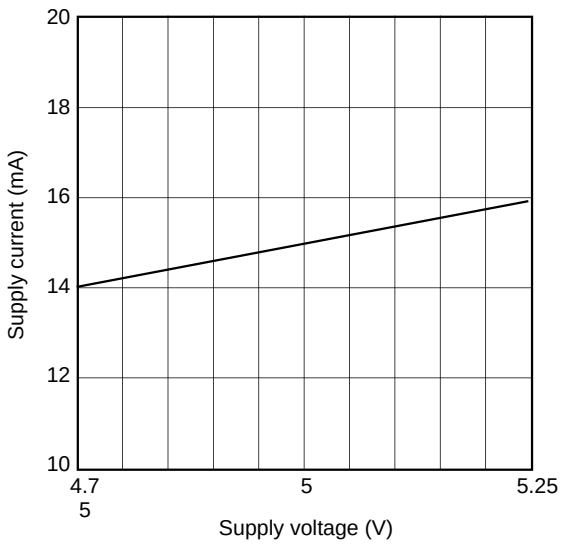
Low frequency gain vs. Ambient temperature



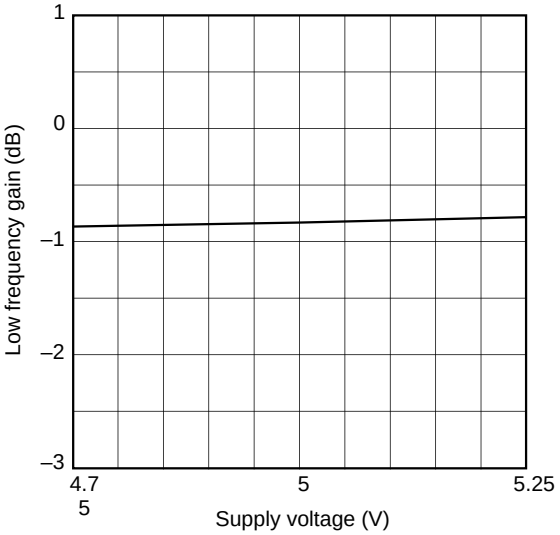
Frequency response vs. Ambient temperature



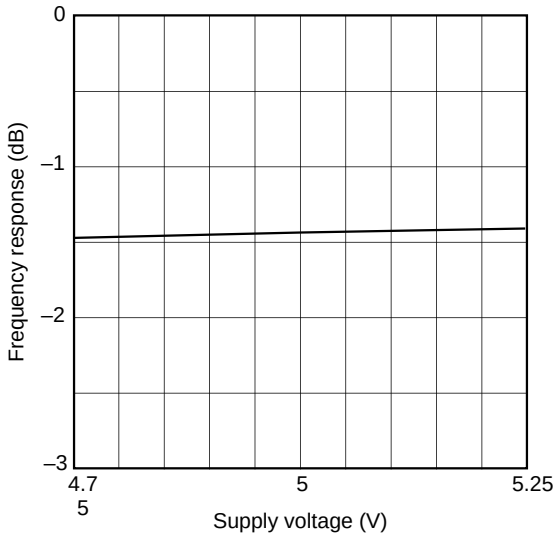
Supply current vs. Supply voltage



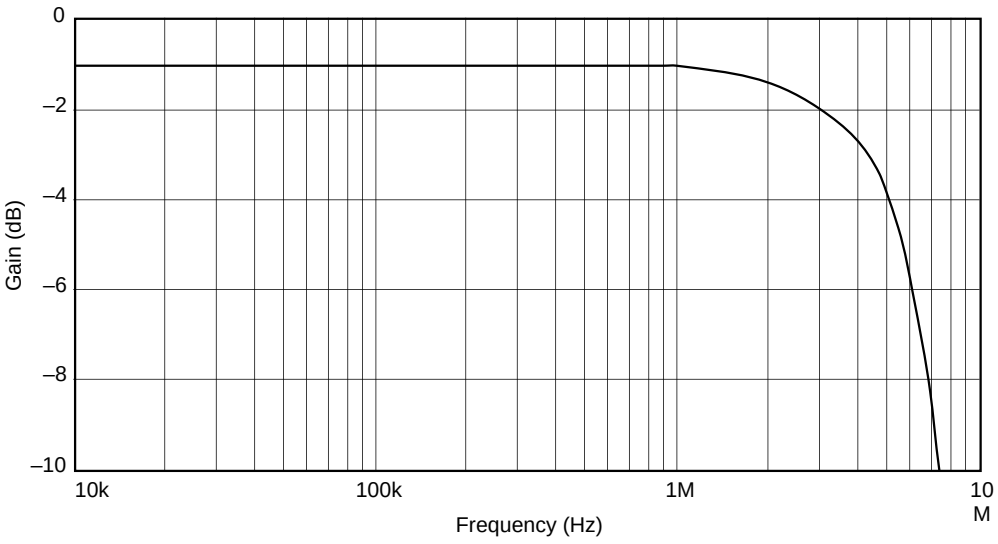
Low frequency gain vs. Supply voltage



Frequency response vs. Supply voltage



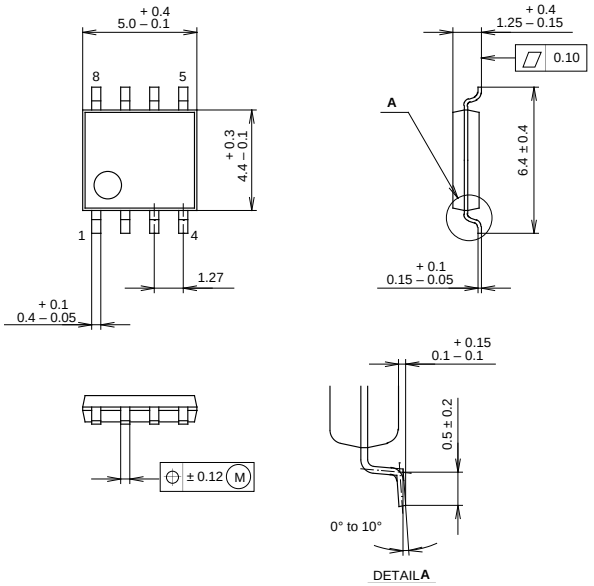
Frequency response



Package Outline Unit : mm

CXL5513M

8PIN SOP (PLASTIC)



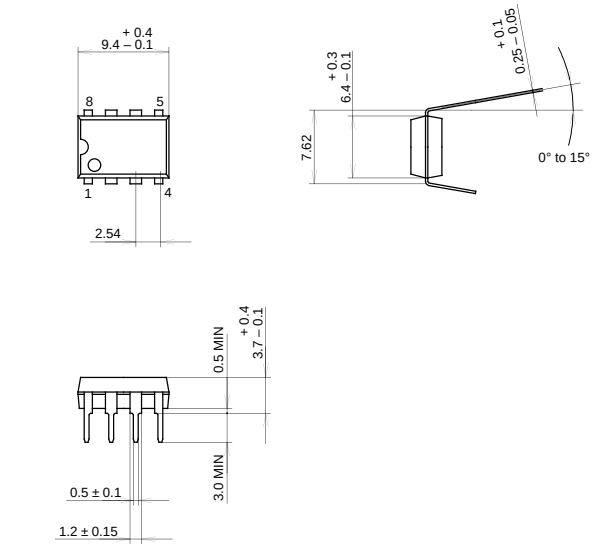
PACKAGE STRUCTURE

SONY CODE	SOP-8P-L03
EIAJ CODE	*SOP008-P-0225-A
JEDEC CODE	

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.1g

CXL5513P

8PIN DIP (PLASTIC) 300mil



PACKAGE STRUCTURE

SONY CODE	DIP-8P-01
EIAJ CODE	*DIP008-P-0300-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.5g