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PortMakerII AAL5 Firmware

CX27470 Traffic Stream Processor

OC-12 Adaptation Layer 5 SAR

PortMakerII firmware provides proven, reliable and fully supported binary applications for the CX27470 Traffic Stream Processor. The ATM adaptation layer 5 (AAL5) application provides a bi-directional OC-12 throughput ITU I.363.5 SAR, traffic shaping and a rich feature set. The firmware is also available with a source code license to allow customization and product differentiation.

KEY FEATURES

- Bi-directional OC-12 throughput
- ITU I.363.5 compliant AAL5 SAR
- ATM Forum TM 4.1 traffic shaping
- Per VC queuing
- Choice of segmenter queue admission policies:
  - Weighted random early detection (WRED),
  - Per VC flow control
  - Per VC early packet discard (EPD)
- VP and VC tunnels
- Encapsulation/ De-encapsulation
- Reassembly time-out
- Support for raw cells (AAL0)
- Per PHY and per connection statistics
- Host control via PCI bus and software API
- Traffic shaping rates configurable from 0.006% to 100% of line rate, with 1% accuracy
- Supports 32K bi-directional connections

AAL5 Segmentation and Reassembly (SAR)

The PortMakerII AAL5 firmware application complies with the ITU I.363.5 standard, and also conforms to the ATM Forum PICS Proforma for the AAL Type 5 tests. The firmware provides OC-12 throughput with 32K connections in bi-directional mode. It can also be configured in a uni-directional configuration (i.e., two chip solution) with 2xOC-12 throughput and 64K connections. ATM cell traffic uses the UTOPIA interface on the CX27470, while packet traffic can use either the UTOPIA/POS interface for streaming mode operation, or the PCI bus for shared memory operation. Host based management of the SAR is accomplished via the PCI bus using commands, acknowledgements, indications, and alarms.

Traffic Shaping

Traffic shaping is provided at the output of the segmentation function. Each connection has two generic cell rate algorithms (GCRAs) that support the CBR.1, VBR.1, UBR.1 and UBR.2 conformance definitions in the ATM forum traffic management 4.1 specification. The host selects the shaping parameters and priority on a per VC basis at open channel time. A four level strict priority scoreboard based mechanism is used to schedule cells for transmission, allowing quality of service (QoS) level guarantees. Shaping rates are available from 0.006% to 100% of line rate, with 1% accuracy.

Buffer Management

Two pools of buffers are supported: internal buffers and host buffers. Internal buffers occupy local SDRAM and are 64 bytes in length. Internal buffers are allocated to one of 16 buffer classes during initialization.

Host buffers are configurable in size and can be placed either in local SDRAM or in host memory on the PCI bus. Host buffers are optionally used for packets output from the reassembler, when the shared memory mode of operation is used. Up to 256 Mbytes of local SDRAM are supported for both internal and host buffers.

Congestion Control

Segmenter packets are stored in per VC queues. Queue admission is controlled by one of three methods selected at open channel time: 1) weighed random early discard (WRED), 2) per VC flow control, or 3) per VC early packet discard (EPD). The WRED algorithm discards packets in a manner that optimizes the overall network performance of TCP/IP connections. Up to 128 sets of WRED parameters are supported, selected on a per packet basis. The per VC flow control option sends indications to the host when a configurable high and low threshold are crossed (with hysteresis). Per VC EPD is similar to flow control except that packets are dropped when the high threshold is exceeded, and no indications are sent.

Both the segmenter and reassembler provide per buffer class EPD when a configurable threshold is exceeded, and partial packet discard (PPD) when the buffer class is exhausted.

VP Tunnels with Weighted Round Robin

A segmenter VP tunnel consists of a group of VCs, each of which gains access to the tunnel using a weighted round robin scheme. This allows proportional bandwidth sharing among the VCs. The tunnel itself is then shaped in the same manner as ordinary VCs.

VC Tunnels with Weighted Fair Queuing

A segmenter VC tunnel provides up to 8 class of service (CoS) queues, allowing packets from each CoS queue to be multiplexed onto a single channel. The CoS queues are serviced using a weighted fair queuing (WFQ) algorithm. Fairness is measured on a per cell basis, however full packets are transmitted at a time. The tunnel itself is then shaped in the same manner as ordinary VCs.

Encapsulation/De-encapsulation

The segmenter offers optional 8- or 10-byte encapsulation, intended to support routed IPv4 and Ethernet PDUs as defined in RFC 2684. The reassembler offers optional stripping of 0 to 31 bytes. All encapsulation and de-encapsulation parameters are determined on a per channel basis.

Statistics

The segmenter provides the following counters on both a per channel and per port basis: bytes transmitted, packets transmitted, packets discarded during queue admission, and packets discarded due to error conditions.

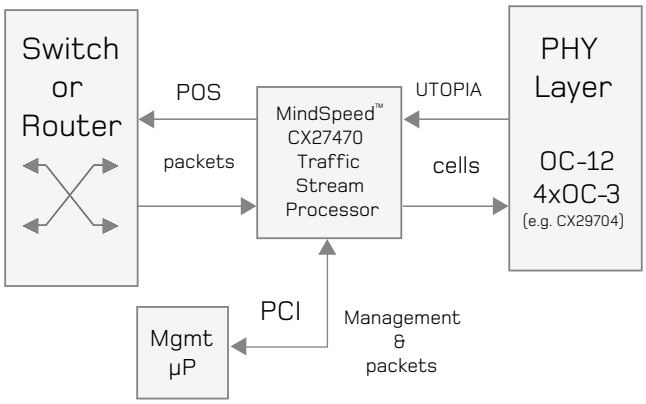
The reassembler provides the following counters on both a per channel and per port basis: bytes received, packets received, packets discarded during queue admission, and packets discarded due to error conditions.

Memory Requirements

The PortMakerII AAL5 application supports up to 256 Mbytes of SDRAM used for data buffers. Program and context storage require 4 or 8 Mbytes of SRAM to support either 16K or 32K connections, respectively.

Applications

The PortMakerII AAL5 firmware is intended for use in enterprise, aggregation, edge, and core routers, multi-service edge switches, optical edge equipment, and DSLAMS. A typical application using the CX27470 running PortMakerII AAL5 firmware is shown below.

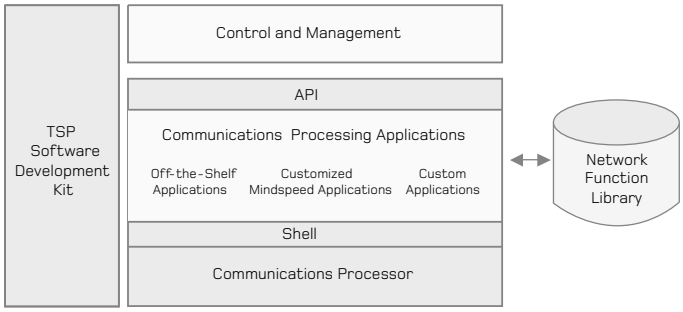


Application Block Diagram

Source Code Development Environment

PortMakerII AAL5 is based on a modular architecture using a system management kernel (or 'shell'), and a set of transfer functions. The shell communicates with external host processors, dispatches commands and performs background task scheduling. The transfer functions consist of initialization routines, command handlers and event handlers, which provide the segmentation and reassembly processing. An event driven architecture is used to dispatch the appropriate handler to service incoming data or commands.

The Network function library contains the source code modules used to implement the off-the-shelf transfer functions. These fully tested routines are available to source code developers wishing to customize or enhance existing applications. The modular PortMakerII architecture also facilitates the addition of completely new features, allowing developers to concentrate their efforts on the value added functions of their application.



Modular PortMakerII Architecture

Development Tools

The TSP software development kit (SDK) is intended for source code developers. It provides a full-featured set of hardware and software co-development tools for the TSP product family. A significant reduction in design cycle time is achieved by enabling hardware integration, software integration, and debugging to start early in the product development cycle. The SDK consists of a hardware and software co-simulator, an assembler/linker, a debugger and TSP board developers kit (BDK).

The BDK is intended for both source and binary customers. It provides hardware simulation models (SWIFT and Verilog), test benches, bus functional models, IBIS models and a reference design. Reference code is provided to facilitate host application integration. A comprehensive set of diagnostics is provided to assist with testing.

Product Features

Functions

- ITU I.363.5 AAL5 SAR
- OC-12 throughput
- 32K bi-directional connections
- Traffic shaping – dual GCRA per connection
- Supports the following traffic shaping conformance definitions:
  - CBR.1
  - VBR.1
  - UBR.1
  - UBR.2
- VP tunnels with WRR access
- VC tunnels with WFQ access
- Congestion control:
  - Weighted random early detection (WRED)
  - Per VC flow control
  - Per VC early packet discard (EPD)
- Reassembly time-out
- Encapsulation/De-encapsulation
- Support for raw cells (AAL0)
- Host control via PCI bus
- Per connection and per port statistics
  - Bytes transmitted/received
  - Packets transmitted/received
  - Packets discarded due to resource exhaustion
  - Packets discarded due to error conditions
- Memory requirements:
  - 16 to 256 Mbytes of SDRAM
  - 4 Mbytes of SRAM

See the CX27470 data sheet for a description of the hardware interfaces and device characteristics.

Ordering Information

- Binary: MXA-pm2a5-bn
- Source: MXA-pm2a5-sc

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