Features

- 5 Smart Card Interfaces
  - Compliance with ISO 7816, EMV2000, GIE-CB and GSM Standards
  - Direct Connection to the Smart Cards
    - Logic Level Shifters
    - Short Circuit Current Limitation
    - 4kV+ ESD Protection (MIL/STD 883 Class 3)
  - 1 or 2 Master Smart Card interfaces
    - Synchronous Card support (with C4 and C8 Contacts)
    - Card Detection and Automatic de-activation sequence on card extraction
  - 1 to 4 SAM/SIM cards (15 to 30mA each)
  - Programmable Voltage for each smart card
    - Class A: 5V ±0.4V at 60 mA (±0.25V at 65 mA with VCC= 5V±10%)
    - Class B: 3V ±0.2V at 60 mA
    - Class C: 1.8V ±0.14V at 40mA
  - Low Ripple Noise: < 200 mV
  - Programmable Activation Sequence
  - Automatic de-activation on card power-fail or over-current and system power-fail
  - Card Clock Stop High or Low for Card Power-down Modes
- Versatile Host Interface
  - Two Wire Interface (TWI) Link at 400kbit/s
    - Programmable Address allow up to 4 AT83C26 on the bus
  - Programmable Interrupt Output
- Reset Output Includes
  - Power-On Reset (POR)
  - Power-Fail Detector (PFD)
- Extended Voltage Operation: 3 to 5.5V
- Low Power Consumption
  - 5 mA Maximum Operating Current (without Smart Card)
  - 150 mA Maximum In-rush Current (each DC/DC)
  - 30 µA Typical Power-down Current (without Smart Card)
- 4 to 48 MHz Clock Input
- System clock derived from the external clock input
- Industrial Temperature Range: -40 to +85°C
- Packages: QFN48, VQFP48

Description

The AT83C26 is a smart card reader interface IC for smart card reader/writer applications such as EFT/POS terminals and set top boxes. It enables the management of any type of smart card from any kind of host. Up to 4 AT83C26 can be connected in parallel thanks to the programmable TWI address.

Its high efficiency DC/DC converters and low quiescent current in stand-by mode make it particularly suited to low power and portable applications. The reduced bill of material allows to lower significantly the system size and cost. A sophisticated protection system guarantees timely and controlled shutdown upon error conditions.

Multiple Smart Card Reader Interface With Power Management

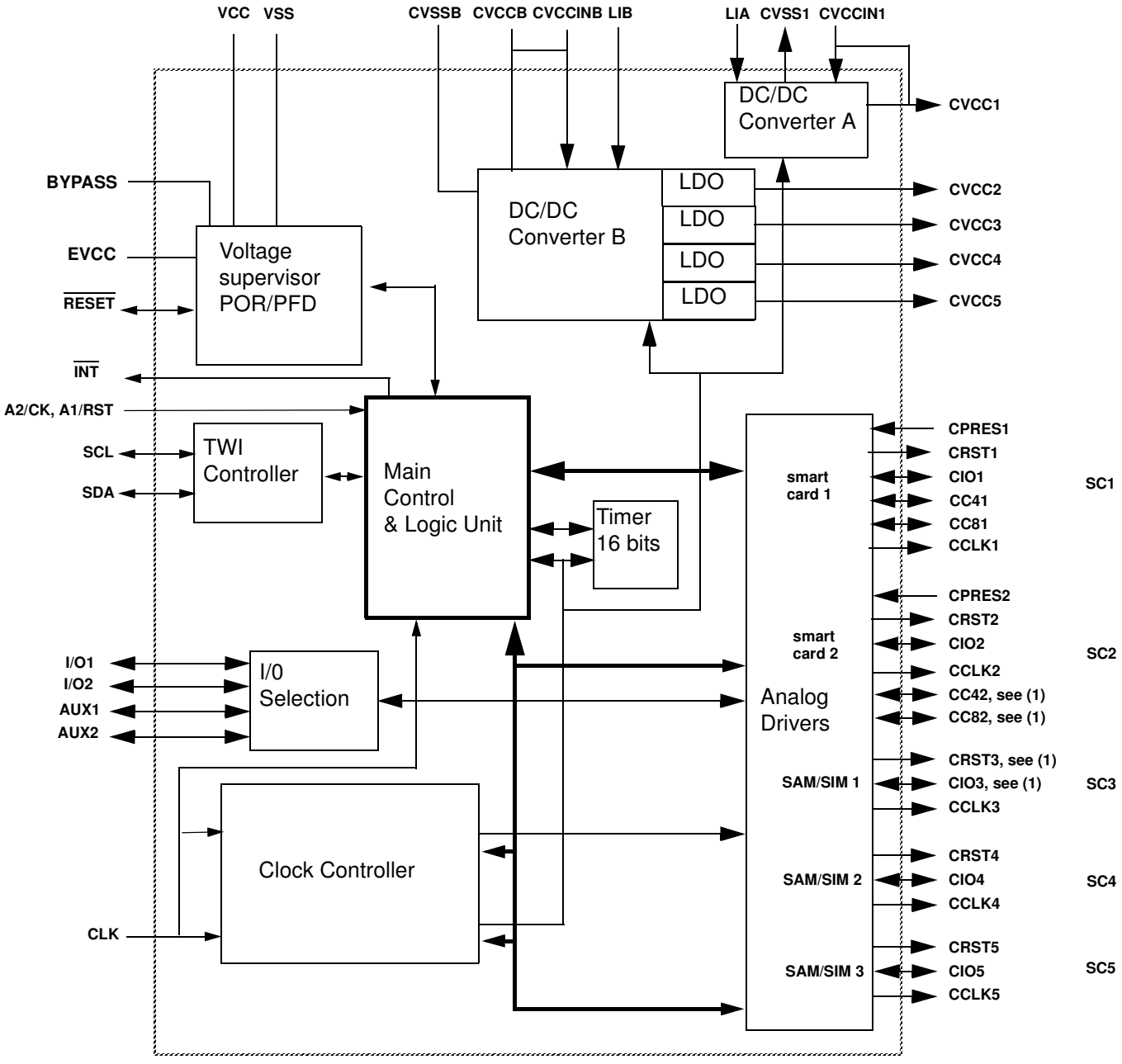
AT83C26

7511D–SCR–02/07

Acronyms

TWI: Two Wire Interface
POR: Power On Reset
PFD: Power Fail Detect
ART: Automatic Reset Transition
ATR: Answer To Reset

Block Diagram

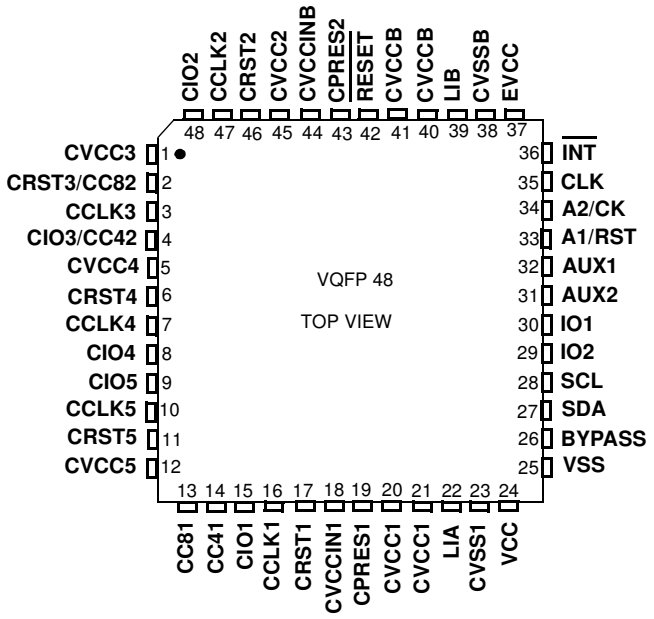


Note: 1. CRST3/CC82 are on the same pin. CIO3/CC42 are on the same pin. If complete Smart card 2 interface is used, SAM/SIM3 isn't available. Respectively, if SAM/SIM3 is used, complete Smart card 2 isn't available.

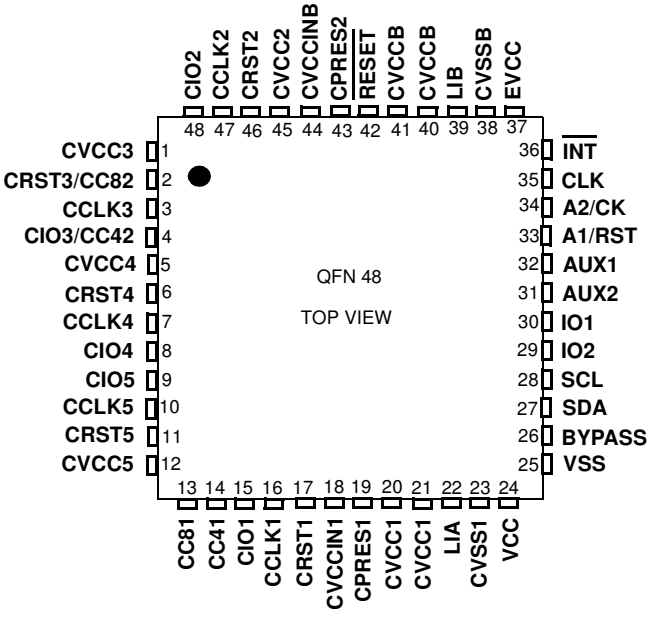
Pin Description

Pinout (Top View)

VQFP48 Pinout



QFN48 Pinout



Signals

Table 1. Ports Description

VQFP48 or QFN48 Pin number	Pad Name	Pad Internal Power Supply	Pad Type	Description
1	CVCC3		PWR	VCC pin for SC3 interface.
2	CRST3/CC82	CVCC3	I/O pull up	See SC2_CFG1 register: If SC2_FULL bit = 0, CRST pin for SC3 interface. If SC2_FULL bit = 1, CC8 pin for SC2 interface.
3	CCLK3	CVCC3	O	CCLK pin for SC3 interface.
4	CIO3/CC42	CVCC3	I/O pull up	See SC2_CFG1 register: If SC2_FULL bit = 0, CIO pin for SC3 interface. If SC2_FULL bit = 1, CC4 pin for SC2 interface.
5	CVCC4		PWR	VCC pin for SC4 interface.
6	CRST4	CVCC4	O	RST pin for SC4 interface.
7	CCLK4	CVCC4	O	CCLK pin for SC4 interface.
8	CIO4	CVCC4	I/O pull up	CIO pin for SC4 interface.
9	CIO5	CVCC5	I/O pull up	CIO pin for SC5 interface.
10	CCLK5	CVCC5	O	CCLK pin for SC5 interface.
11	CRST5	CVCC5	O	RST pin for SC5 interface.
12	CVCC5		PWR	VCC pin for SC5 interface.
13	CC81	CVCC1	I/O pull up	CC8 pin for SC1 interface.
14	CC41	CVCC1	I/O pull up	CC4 pin for SC1 interface.
15	CIO1	CVCC1	I/O pull up	CIO pin for SC1 interface.
16	CCLK1	CVCC1	O	CCLK pin for SC1 interface.
17	CRST1	CVCC1	O	RST pin for SC1 interface.
18	CVCCIN1		PWR	This pin must be connected to CVCC1 pins next to the package.
19	CPRES1	VCC	I pull up	Card presence for SC1 interface. An internal pull up to VCC can be activated in the pad if necessary using PULLUP1 bit in SC1_CFG1 register (activated by default).
20	CVCC1		PWR	VCC pin for SC1 interface. The two CVCC1 pins are connected together near the package. Only one wire goes to the smart card connector. The reason of two CVCC1 pins is to reduce noise.
21	CVCC1		PWR	VCC pin for SC1 interface.

Table 1. Ports Description (Continued)

VQFP48 or QFN48 Pin number	Pad Name	Pad Internal Power Supply	Pad Type	Description
22	LIA		PWR	DC/DCA input. LIA must be tied to VCC pin through an external coil (typically 10µH) and provides the current for the charge pump of the DC/DCA converter. It may be directly connected to VCC if the step-up converter is not used (see STEPREGA bit in SC1_CFG4 register and see minimum VCC values in Table 50.for class A and Table 51. for class B)
23	CVSS1		GND	DC/DCA input. This pin must be directly connected to the VSS of power supply.
24	VCC		PWR	VCC is used to power the internal voltage regulators and I/O buffers.
25	VSS		GND	Ground.
26	BYPASS	VCC	I	A high level on this pin activates a low power consumption mode with internal regulator bypassed.
27	SDA	VCC	I/O open drain	Micro controller interface function: TWI serial data. An external pull up must be connected on SDA pin (4.7kOhms).
28	SCL	VCC	I/O open drain	Micro controller interface function: TWI clock. An external pull up must be connected on SCL pin (4.7kOhms).
29	IO2	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
30	IO1	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
31	AUX2	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
32	AUX1	EVCC	I/O pull up	The behavior of this pin depends on IOSEL[3/0] bits values (see IO_SELECT register).
33	A1/RST	EVCC	I	The TWI address depends on the value present on this pin at reset. If CRST transparent mode is selected, the A1/RST signal is connected to CRST1 or CRST2 pins (see CRST_SEL1 and CRST_SEL2 bits respectively in SC1_CFG4 and SC2_CFG2 registers).
34	A2/CK	EVCC	I	The TWI address depends on the value present on this pin at reset. If CCLKn transparent mode is selected, the A2/CK signal is connected to CCLKn pins (with n=1 to 5). See CKSn[2:0] bits respectively in SC1_CFG1, SC2_CFG2, SC3_CFG2, SC4_CFG2, SC5_CFG2 registers.
35	CLK	EVCC	I	Master clock.
36	$\overline{INT}$	VCC	O open drain	Interruption status. An internal pull up to VCC can be activated in the pin if necessary using INT_PULLUP bit in SC1_CFG4 (deactivated by default).
37	EVCC		PWR	Extra supply voltage (Micro controller power supply). EVCC is used to supply the internal level shifters of host interface pins. EVCC is connected to the host power supply. EVCC voltage can be directly connected to VCC if the host power supply and the AT83C26 power supply is the same.

Table 1. Ports Description (Continued)

VQFP48 or QFN48 Pin number	Pad Name	Pad Internal Power Supply	Pad Type	Description
38	CVSSB		GND	DC/DCB input. This pin must be directly connected to the VSS of power supply.
39	LIB		PWR	DC/DCB input. LIB must be tied to VCC pin through an external coil (typically 10µH) and provides the current for the charge pump of the DC/DCB converter. It may be directly connected to VCC if the step-up converter is not used (see STEPREGB bit in DCDCB register and see minimum VCC values in Table 53.for class A and Table 54. for class B)
40	CVCCB		PWR	DC/DCB output. The two CVCCB pins are connected together near the package. CVCCB pin is only used for DC/DCB voltage measurements.The reason of two CVCCB pins is to reduce noise.
41	CVCCB		PWR	DC/DCB output.
42	$\overline{\text{RESET}}$	VCC	I/O open drain	Micro controller interface function: reset signal. • power on reset • A low level on this pin keeps the AT83C26 under reset even if applied on power-on. It also resets the AT83C26 if applied when the AT83C26 is running. • Asserting $\overline{\text{RESET}}$
43	CPRES2	VCC	I pull up	Card presence for SC2 interface. An internal pull to VCC can be activated in the pad if necessary using PULLUP2 bit in SC2_CFG1 register (activated by default).
44	CVCCINB		PWR	This pin must be connected to CVCCB pins next to the package.
45	CVCC2		PWR	VCC pin for SC2 interface.
46	CRST2	CVCC2	O	CRST pin for SC2 interface.
47	CCLK2	CVCC2	O	CCLK pin for SC2 interface.
48	CIO2	CVCC2	I/O pull up	CIO pin for SC2 interface.

Note: The ESD limit is 4kV for smart card pins and 2kV for others.

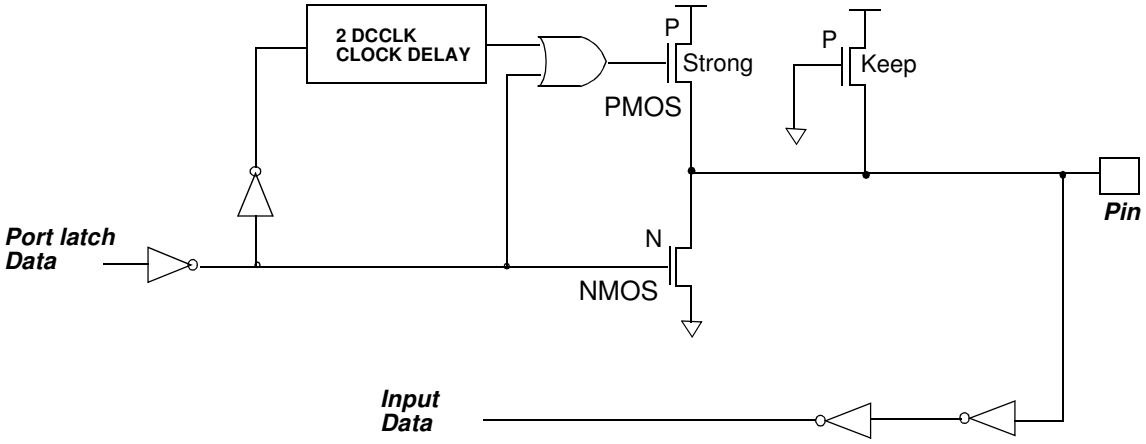
Pad Type Description

To simplify the understanding of Figure 1. to Figure 8., a shortcut is possible by replacing the weak transistor by a 100k Ohms pull-up resistor, the medium transistor by a 10k Ohms pull-up resistor and the strong transistor by a 1k Ohms pull-up resistor.

Input/Output with Pull-up Configuration (IO1, IO2, AUX1, AUX2)

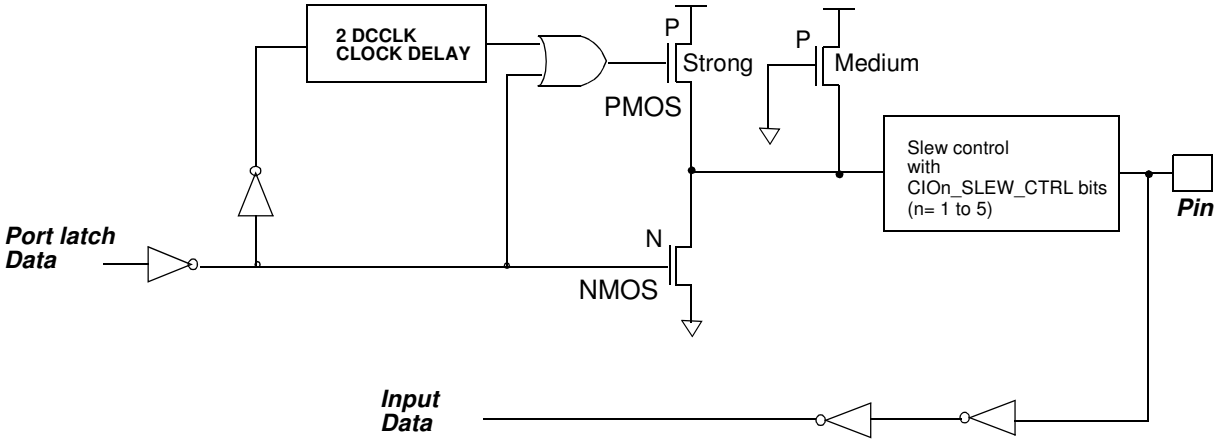
This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the port outputs a logic low state, it is driven strongly and able to sink a fairly large current.

Figure 1. Input/Output with Pull-up Configuration



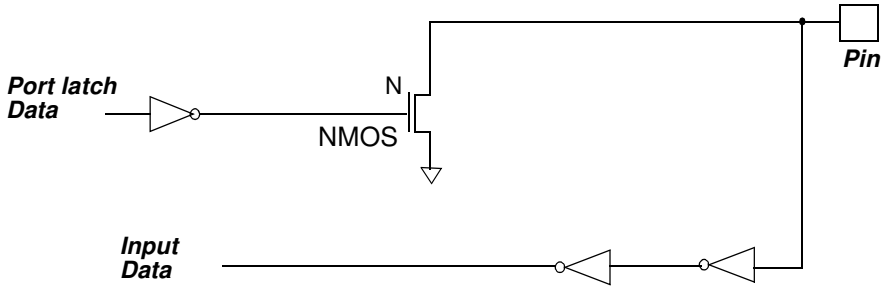
Input/Output with Pull-up Configuration (ClOn with n = 1, 2, 3, 4, 5) and (CC4n, CC8n with n = 1, 2)

Figure 2. Input/Output with Pull-up Configuration



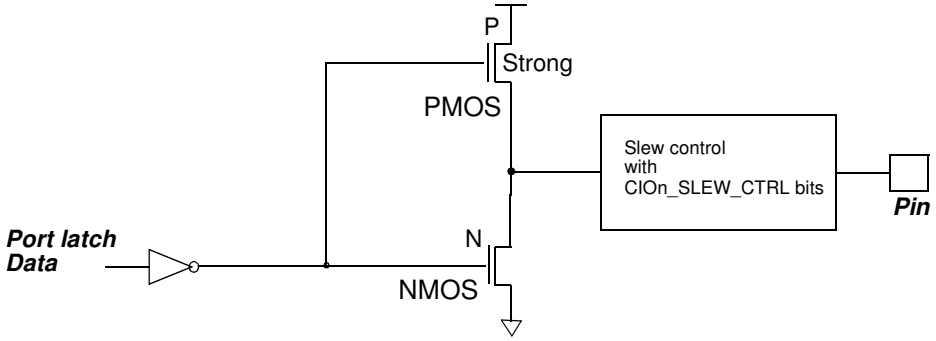
Input/Output with Open Drain Configuration (SDA, SCL, $\overline{\text{RESET}}$)

Figure 3. Input/Output with Open Drain Configuration



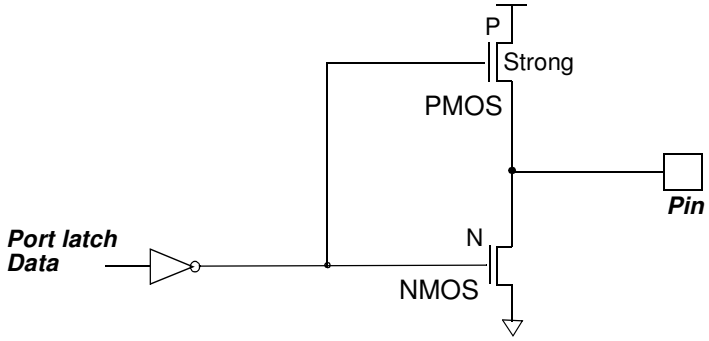
Output Configuration (CCLKn with n = 1, 2, 3, 4, 5)

Figure 4. Output Configuration



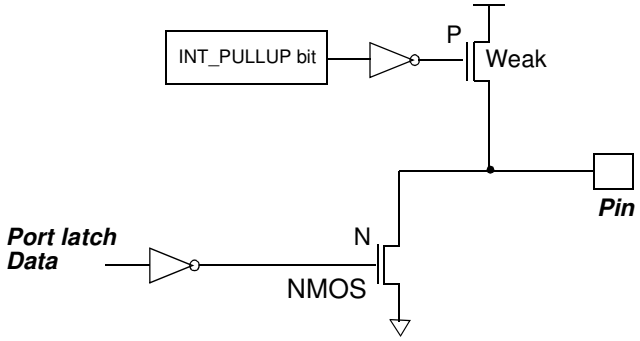
Output Configuration (CRSTn with n = 1, 2, 3, 4, 5)

Figure 5. Output Configuration



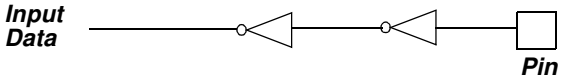
Open drain Output with programmable pull-up Configuration ($\overline{INT}$)

Figure 6. Open Drain Output with programmable pull-up



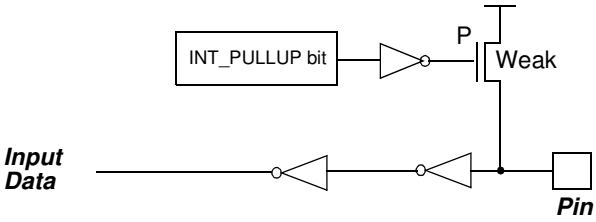
Input Configuration (A1, A2, CLK, BYPASS)

Figure 7. Input



Input with programmable pull-up Configuration (CPRES1, CPRES2)

Figure 8. Input with programmable pull-up



Operational Modes

TWI Bus Control

The Atmel Two-Wire Interface (TWI) interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds of up to 400 Kbits per second, based on a byte-oriented transfer format.

The TWI-bus interface can be used:

- To configure the AT83C26
- To select interface
- To select the operating mode of the card: 1.8V, 3V or 5V
- To configure the automatic activation sequence
- To start or stop sessions (activation and de-activation sequences)
- To initiate a warm reset
- To control the clock to the card in active mode
- To control the clock to the card in stand-by mode (stop LOW, stop HIGH or running)
- To enter or leave the card stand-by or power-down modes
- To select the interface (connection to the host I/O/C4/C8)
- To request the status (card present or not, over-current and out of range supply voltage occurrence)
- To drive and monitor the card contacts by software
- To accurately measure the ATR delay when automatic activation is used
- Re-use the AT83C24 command set for the first DC/DC and smart card interface with the following changes:
  - CKS extended to CONFIG2[0:3], CKS=8 selects CLK/3 and CKS>8 is reserved
  - The slave address byte for TWI write commands is 0100 $A_2A_1$10 and 0100 $A_2A_1$11 for TWI read commands

TWI Commands

Frame Structure

The structure of the TWI bus data frames is made of one or a series of write and read commands completed by STOP.

Write commands to the AT83C26 have the structure:

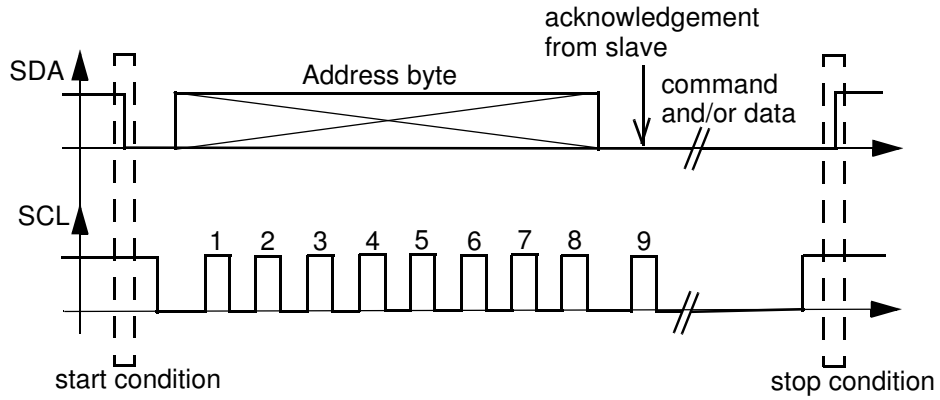
ADDRESS BYTE + COMMAND BYTE + DATA BYTE(S)

Read commands to the AT83C26 have the structure:

ADDRESS BYTE + DATA BYTE(S)

The ADDRESS BYTE is sampled on A2/CK and A1/RST **after each reset** (hard/soft/general call) but A2/CK, A1/RST can be used for transparent mode after the reset.

Figure 1. Data transfer on TWI bus

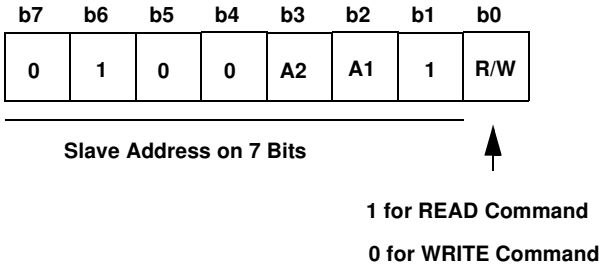


Address Byte

The first byte to send to the device is the address byte. The device controls if the hardware address (A2/CK, A1/RST pins on reset) corresponds to the address given in the address byte (A2, A1 bits).

If the level is not stable on A2/CK pin at reset, the user has to manage the possible address taken by the device.

Figure 2. Address Byte



Up to 4 devices can be connected on the same TWI bus. Each device is configured with a different combination on A2/CK, A1/RST pins. The address byte of each device for read/write operations are listed below.

Table 2. Address Byte Values

A2 (A2/CK pin)	A1 (A1/RST pin)	Address Byte for Read Command	Address Byte for Write Command
0	0	0x43	0x42
0	1	0x47	0x46
1	0	0x4B	0x4A
1	1	0x4F	0x4E

$\overline{\text{RESET}}$ pin

The TWI ADDRESS BYTE is sampled on A2/CK and A1/RST after a rising edge on $\overline{\text{RESET}}$ pin. The delay between the rising edge and the sampling of A2/CK and A1/RST is t1.

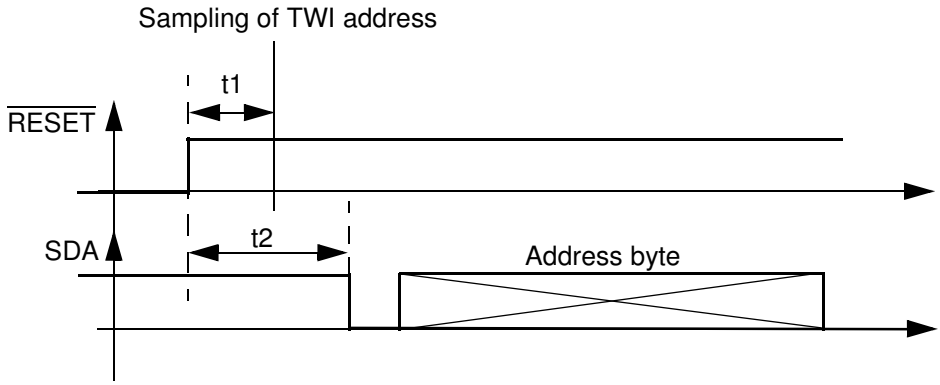
The value for t1 is 22 CLK period.

The minimum value for t2 is 40 CLK period. During the t2 time, the TWI bus is not ready to receive a command.

The CLK period depends on the frequency of the signal on CLK pin.

The $\overline{\text{RESET}}$ pin is an I/O with Open Drain. The host IO pin connected to $\overline{\text{RESET}}$ must be an I/O open drain (with external pull-up) or an I/O open drain with internal pull up.

Figure 3. Timings after reset



BYPASS pin

A high level on this pin activates a low power consumption mode.

At reset, the level on this pin must be fixed (VSS or VCC).

Before to set BYPASS pin, SHUTDOWNA and SHUTDOWNB bits must be set.

If SHUTDOWNA bit is set, DCDCA is switched off.

If SHUTDOWNB bit is set, DCDCB is switched off.

If SHUTDOWNA and SHUTDOWNB bits are set, the regulator is switched off.

If BYPASS pin is at a high level, the bandgaps are switched off.

Smart Card Interfaces

The AT83C26 enables the management of up to 5 smart card interfaces. Due to shared IOs between SC2 and SC3, the user should choose between a full SC2 interface (with CC4 and CC8) or SC3 interface.

The SC2_FULL bit in SC2_CFG1 register is used to select the SC2/SC3 interfaces configuration.

Table 3. SC2 and SC3 shared IOs

Pin name	SC2_FULL = 1 SC3 interface not available	SC2_FULL = 0 SC2 without CC4and CC8 + SC3 interface
CPRES2	CPRES2	CPRES2
CRST2	CRST2	CRST2
CIO2	CIO2	CIO2
CCLK2	CCLK2	CCLK2
CRST3/CC82	CC82	CRST3
CIO3/CC42	CC42	CIO3
CCLK3	unused	CCLK3

DCDC Converters

The DC/DC A converter is used to provide smart card voltage for the SC1 interface (CVCC1).

The DC/DC B converter is used to provide smart card voltage for the SCn interfaces (n=2, 3, 4, 5).

DC/DC converters need a clock of 4MHz (see Section “Clock Controller”). Two internal oscillators (one for each converter) provide the DC/DC clocks.

The DC/DCB output is connected on 4 LDO regulators (Low Drop Output) to generate CVCCn voltage (n=2, 3, 4, 5).

Clock Controller

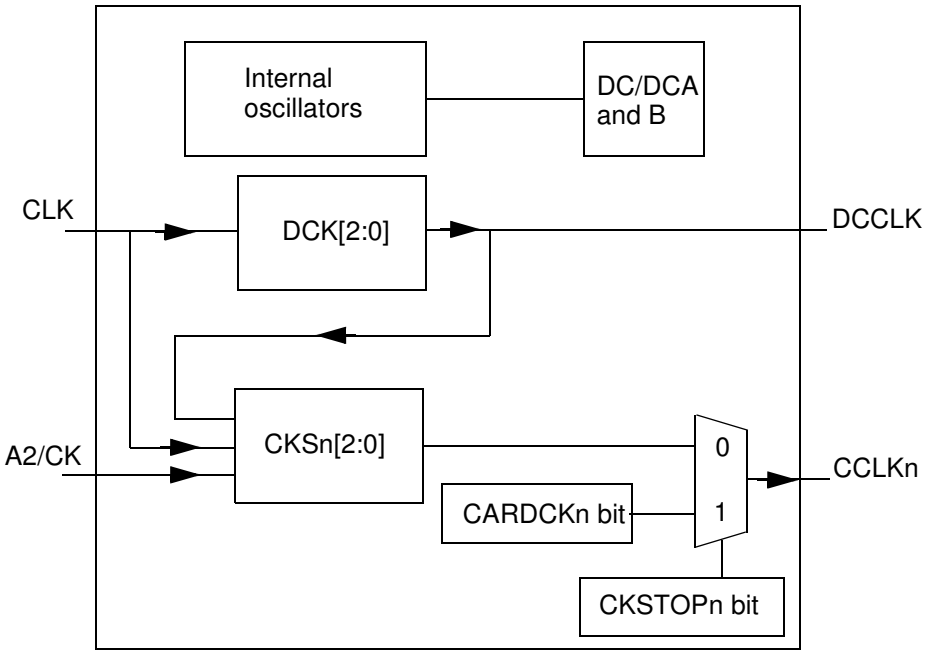
The clock controller outputs six clocks:

1. Five clocks for CCLK1, CCLK2, CCLK3, CCLK4 and CCLK5. Four different sources can be used: CLK pin, DCCLK signal, CARDCKn bit (n=1, 2, 3, 4, 5) or A2/CK.
2. A DCCLK clock used for pads and deactivation sequence.

Clock controller for SCn (n=1, 2, 3, 4, 5)

The transparent mode with A2/CK pin is available on SCn interface. The CKSn[2:0] register is used to select this transparent mode between A2/CK and CCLKn. The bit CKSTOPn must be cleared to have CCLKn running according to CKSn[2:0].

Figure 4. Clock Block Diagram with Software Activation



CRST controller

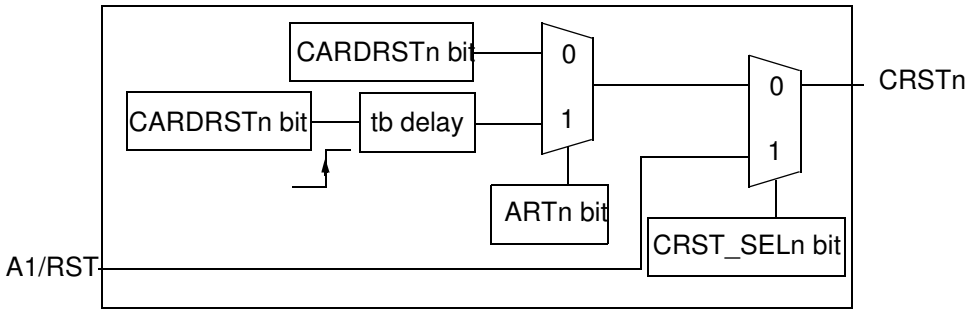
CRSTn for SCn interface (n=1, 2)

The CRSTn output pin is driven by the CARDRSTn bit value or by A1/RST pin.

Three modes are available:

- If the ARTn bit is reset, CRSTn pin is driven by CARDRSTn bit.
- If the ARTn bit is set, CRSTn pin is controlled and follows the “Automatic Reset Transition” (see Activation sequence page 25).
- A transparent mode with A1/RST pin.

Figure 5. CRSTn Block Diagram



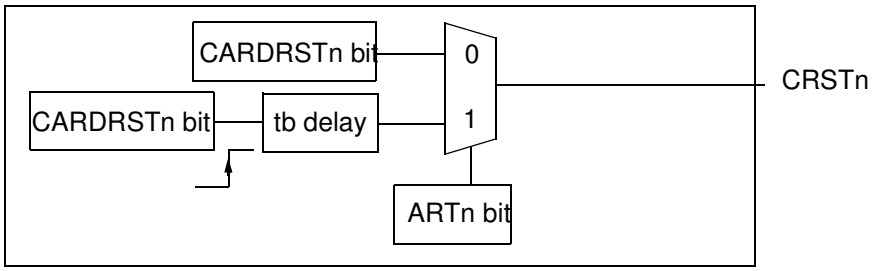
CRSTn for SCn interface (n= 3, 4, 5)

The CRSTn output pin is driven by the CARDRSTn bit value (see SCn_CFG2 register).

Two modes are available:

- If the ARTn bit is reset, CRSTn pin is driven by CARDRSTn bit.
- If the ARTn bit is set, CRSTn pin is controlled and follows the “Automatic Reset Transition” (see Activation sequence page 25).

Figure 6. CRSTn Block Diagram



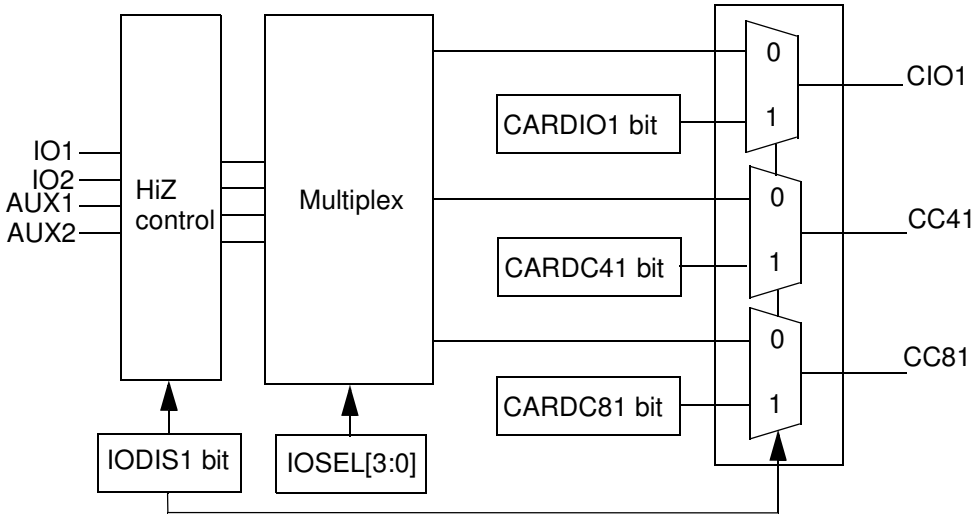
If SC2_FULL=1, the SC3 interface is not available.

CIO, CC4, CC8 controller

CIO1, CC41, CC81 controller for SC1 interface

The CIO1, CC41, CC81 output pins are driven respectively by CARDIO1, CARDC41, CARDC81 bits values or by I/O1, I/O2, AUX1or AUX2 signals. This selection depends of the IODIS1 bit value (SC1_INTERFACE register) and of IOSEL[3:0] bits value (IO_SELECT register).

Figure 7. CIO1, CC41, CC81 Block Diagram

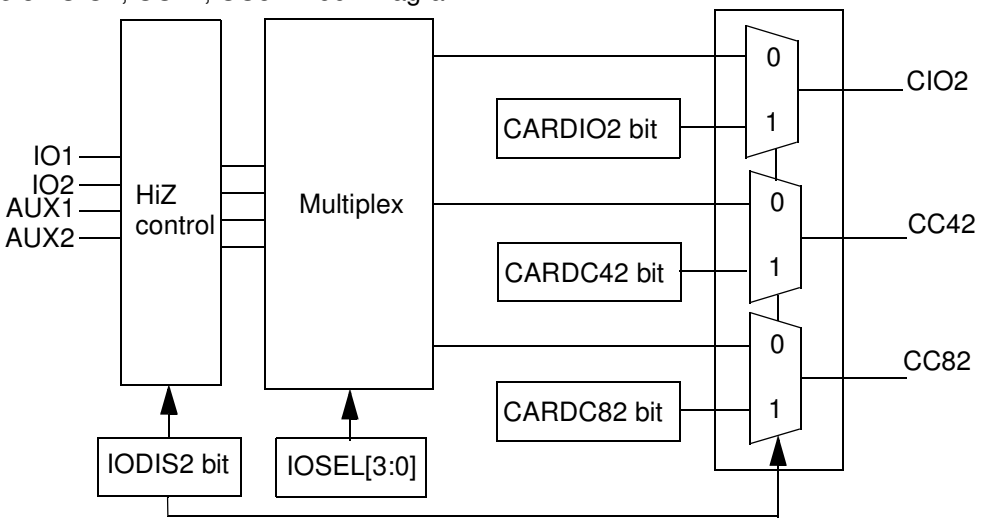


If IODIS1 is set, the CARDIO1 bit value is output on CIO1.The input selected by IOSEL for CIO1 is in High impedance state. CC41 and CC81 have the same behavior.

If IODIS1 is reset, data are bidirectional between the I/O1, I/O2, AUX1, AUX2 pins (see IO_SELECT register) and CIO1, CC41, CC81 pins.

CIO2, CC42, CC82 controller for SC2 interface

Figure 8. CIO2, CC42, CC82 Block Diagram

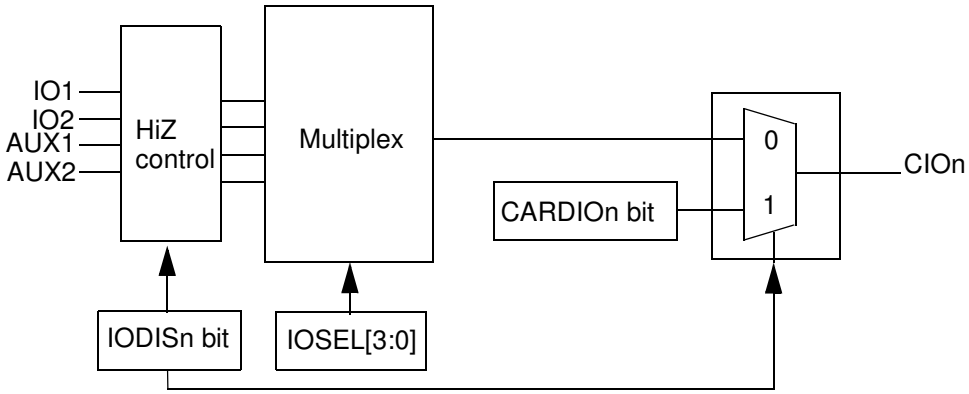


The SC2_FULL bit must be set to use CC42 and CC82.

CIOn controller for SCn interface (n=3, 4, 5)

The CIOn output pin is driven by CARDIOn bit values or by I/O1, I/O2, AUX1 or AUX2 signals. This selection depends of the IODISn bit value. If IODISn is reset, data are bidirectional between the I/O1, I/O2, AUX1, AUX2 pins (see IO_SELECT register) and CIOn pins.

Figure 9. CIOn Block Diagram



CIOn (n=1 to 5), CC41, CC81, CC42, CC82 transparent mode description

Two modes are available on CIOn, CC4n, CC8n signals:

- Bit control (a bit controls the output pin)
- Transparent mode (IO signal and CIO are linked after level shifter)

According to IO_SELECT register value and IODISn bits values, one of 4 input pins (IO1, IO2, AUX1 or AUX2) is linked to the selected output.

The idle state is the high level. Each signal is bidirectional.

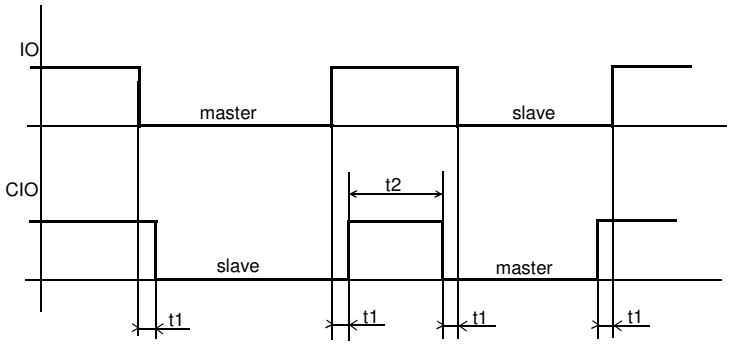
Transparent mode arbitration system

The first between IO and CIO to force a low level becomes the master.

The slave signal is grounded after t1 delay:

t1 max = 2* (CLK period).

Figure 10. Bidirectional mode



The minimum delay for a pulse at 0 or 1 to be detected is between 0.5 and 1.5 CLK period (depending on arrival time).

If IO and CIO are both grounded, CIO becomes the master.

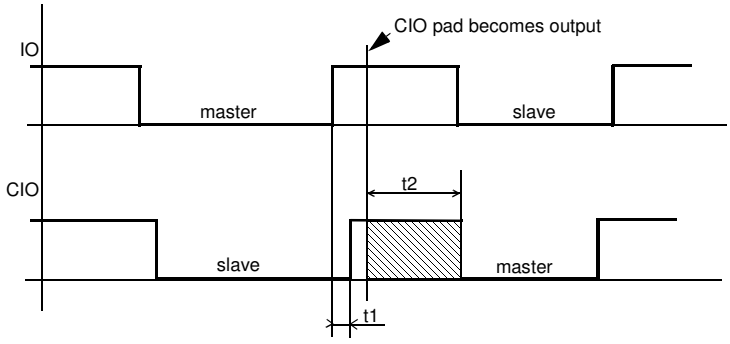
The minimum delay to switch of master without electrical conflict is equal to:

t2 min = 4 * (CLK period) + 2 * (DCCLK period) * (CLK period).

If a master switch appears before this minimum delay, the electrical conflict delay is:

t2 = 2 * (DCCLK period) * (CLK period)

Figure 11. Electrical conflict



CCLKn and CIOn (n=1 to 5) slew rate control

Three registers SLEW_CTRL_1, SLEW_CTRL_2 and SLEW_CTRL_3 control the slew rate of the CIOn and CCLKn signals. Each signal has 2 control bits.

An automatic mode is proposed. The VCARDn[1:0] value is used to automatically adjust the slew rate.

For specific cases, like long wires between AT83C26 and smart card connector for example, the user can forced the slew rate.

The rising edge and the falling edge are modified with the slew rate control for CCLKn.

Only the rising edge is modified on CIOn with the slew rate control.

See Table 63. to Table 68. in Electrical Characteristics.

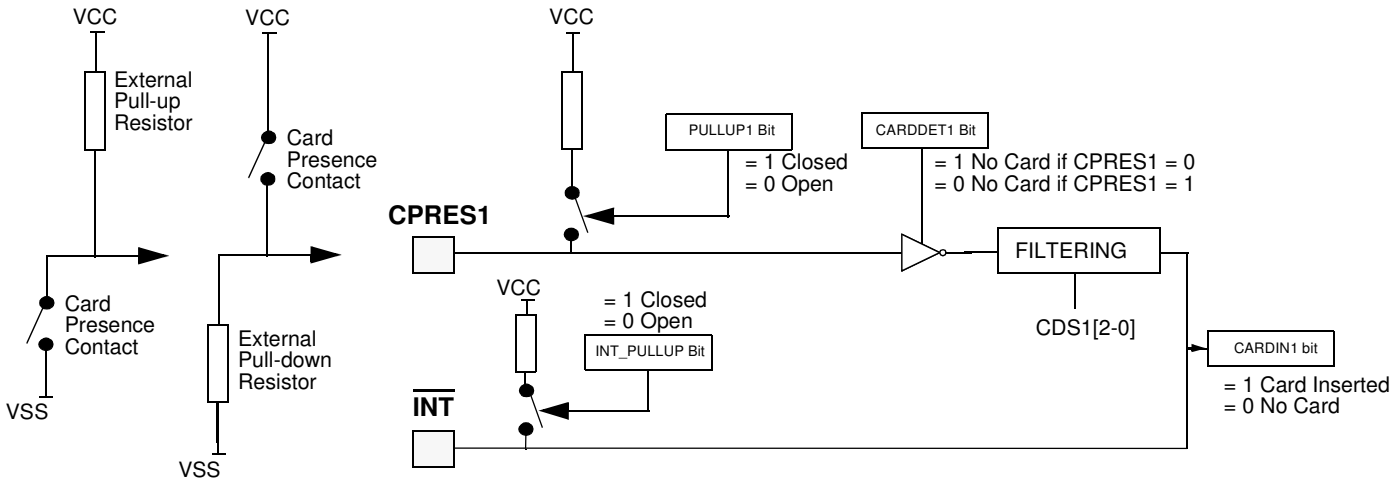
Card Presence Detection

Card presence detection for SC1 interface

The card presence signal is connected on the CPRES1 pin. The polarity of card presence contact is selected with the CARDDET1 bit (see SC1_CFG1 register). A programmable filtering is controlled with the CDS1[2-0] bits.

The internal pull-up on the CPRES1 pin can be disconnected in order to reduce the consumption. An external pull-up must be connected to Vcc. The PULLUP1 bit (see SC1_CFG1 register) controls this feature.

Figure 12. SC1 presence Input

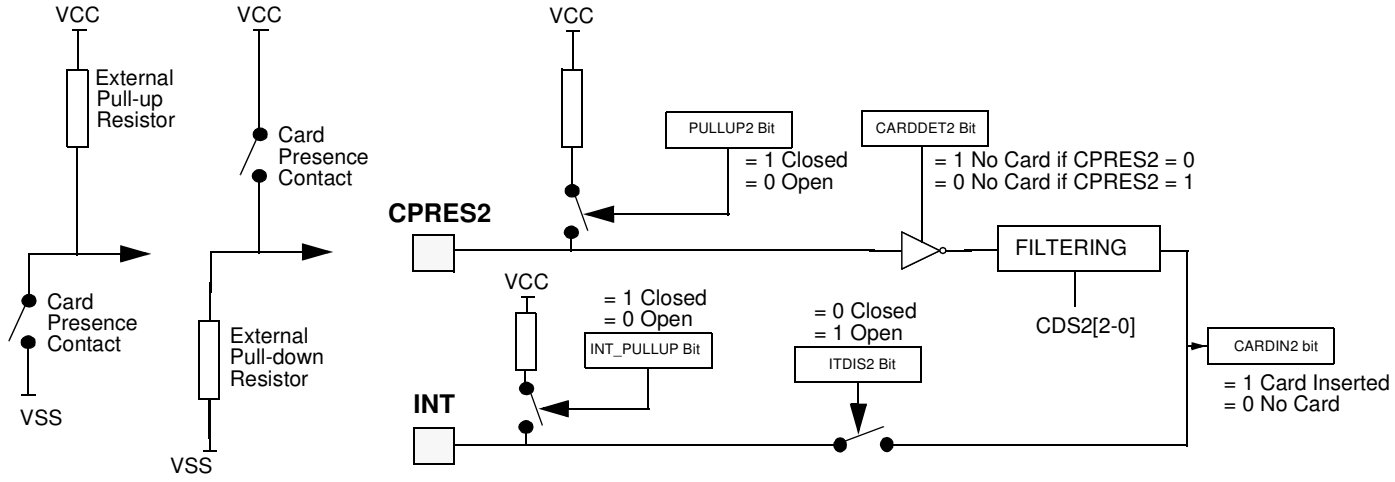


If the card presence contact is connected to Vcc, the internal pull-up must be disconnected and an external pull-down must be connected to the CPRES1 pin.

An interrupt can be generated if a card is inserted or extracted (see Section “Interrupts”, page 30).

Card Presence Detection for SC2 interface

Figure 13. SC2 presence Input



DC/DC converters

DC/DC A converter

The DC/DC A converter is controlled by VCARD1[1:0], SHUTDOWNA, ICCADJA, STEPREGA, VCARD_OK1 and DEMBOOSTA[1:0] bits.

The DC/DC A converter cannot be switched on while the CPRES1 pin remains inactive. If CPRES1 pin becomes inactive while the DC/DC A converter is operating an automatic shut down sequence of the DC/DC A converter is initiated by the electronics.

A write operation in VCARD1[1:0] (0x01, 0x02, 0x03) starts the DC/DC. When the output voltage remains within the voltage range specified by VCARD1[1:0], the VCARD_OK1 bit is set.

After a deactivation sequence (card extraction, DC/DC output voltage out of range, SHUTDOWNA bit =1...) the DC/DC A converter is automatically stopped.

It is mandatory to switch off the DC/DC A converter before entering in Power-down mode.

The DC/DC A Converter can work in two different modes which are selected by STEPREGA bit:

- Pump Mode (STEPREGA = 0): an external inductance of 10 µH must be connected between pins LIA and VCC. VCC can be higher or lower than CVCC1.
- Regulator mode (STEPREGA = 1): no external inductance is required but VCC must be always higher than CVCC+0.3V.

The current drawn from power supply by the DC/DC A converter is controlled during the startup phase in order to avoid high transient current mainly in Pump Mode which could cause the power supply voltage to drop dramatically. This control is done by means of bits DEMBOOSTA[1:0], which increases progressively the startup current level.

The DC/DCA sensitivity to any overflow current can be modified (20%) by using the ICCADJA bit (SC1_CFG3 register).

Initialization Procedure for DC/DC A converter

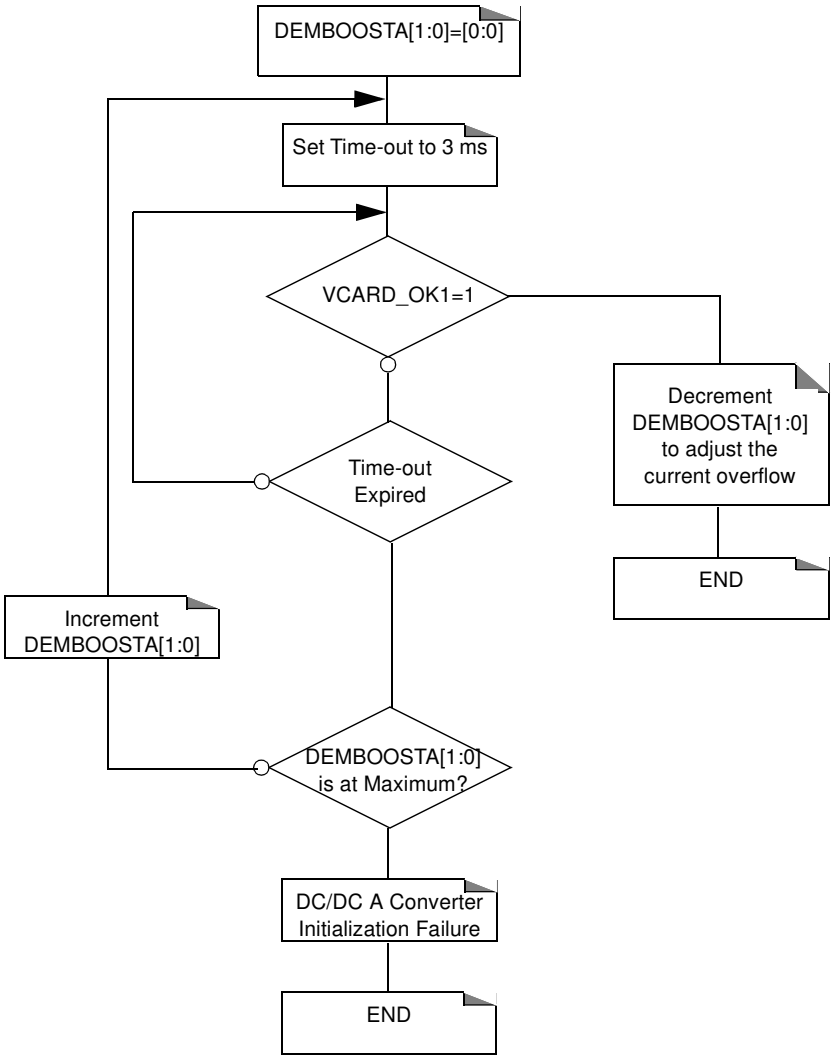
The initialization procedure is described in flow chart:

- Select the CVCC1 level by means of bits VCARD1[1:0] in SC1_CFG0 register,
- Set bits DEMBOOSTA[1:0] in SC1_CFG4 register following the current level control wanted.
- Monitor VCARD_OK1 bit in SC1_STATUS register in order to know when the DC/DC A Converter is ready (CVCC1 voltage has reached the expected level)

While VCC1 remains higher than 3.6V and startup current lower than 30 mA (depending on the load type), the DC/DC A converter should be ready without having to increment DEMBOOSTA[1:0] bits beyond [0:0] level. If at least one of the two conditions are not met (VCC < 3.6V or startup current > 30 mA), it will be necessary to increment the DEMBOOSTA[1:0] bits until the DC/DC converter is ready.

Increment of DEMBOOSTA[1:0] bits increases at the same time the current overflow level in the same proportion as the startup current. So once the DC/DC converter is ready it advised to decrement the DEMBOOSTA[1:0] bits to restore the overflow current to its normal or desired value.

Figure 9. DC/DC A Converter Initialization Procedure



DC/DC B converter

The DC/DC B converter is controlled by DCDCB register.

The DC/DC B converter can be switched on even if CPRES2 pin remains inactive.

A write operation in VDCB[1:0] (0x01, 0x02, 0x03) starts the DC/DC. When the output voltage remains within the voltage range specified by VDCB_OK[1:0], the VDCB_OK bit is set.

The DC/DC B Converter can work in two different modes which are selected by STEPREGB:

- Pump Mode (STEPREGB = 0): an external inductance of 10 µH must be connected between pins LIB and VCC. VCC can be higher or lower than selected voltage.
- Regulator mode (STEPREGB = 1): no external inductance is required but VCC must be always higher than selected voltage+0.3V.

The current drawn from power supply by the DC/DC B converter is controlled during the startup phase in order to avoid high transient current mainly in Pump Mode which could cause the power supply voltage to drop dramatically. This control is done by means of bits DEMBOOSTB[1:0], which increases progressively the startup current level.

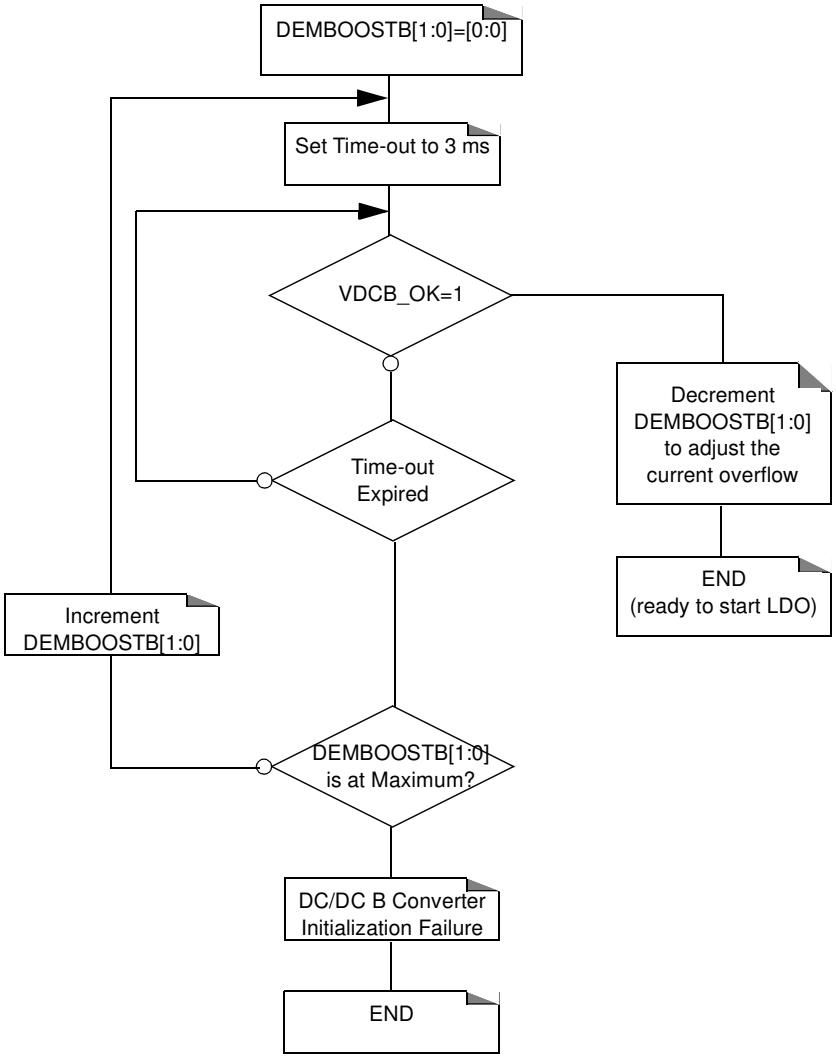
The DC/DCB sensitivity to any overflow current can be modified (20%) by using the ICCADJB bit (DC/DCB register).

Initialization Procedure for DC/DC B converter

The initialization procedure is described in flow chart:

- Select the DC/DC B level by means of bits VDCB[1:0] in DCDCB register,
- Set bits DEMBOOSTB[1:0] in INTERFACEB register following the current level control wanted.
- Monitor VDCB_OK bit in DCDCB register in order to know when the DC/DC B Converter is ready

Figure 10. DC/DC B Converter Initialization Procedure



Increment of DEMBOOSTB[1:0] bits increases at the same time the current overflow level in the same proportion as the startup current. So once the DC/DC B converter is ready it advised to decrement the DEMBOOSTB[1:0] bits to restore the overflow current to its normal or desired value.

LDO initialization Procedure

When the DC/DC B voltage rises the selected voltage (VDCB_OK=1), the card voltage selection on CVCC2, CVCC3, CVCC4 or CVCC5 starts the corresponding LDO.

The CVCC2 card voltage must be started in first (if needed). When the VCARD_OK2 is set, the CVCC3,CVCC4, CVCC5 card voltage are started one after each other (if needed) with the same procedure.

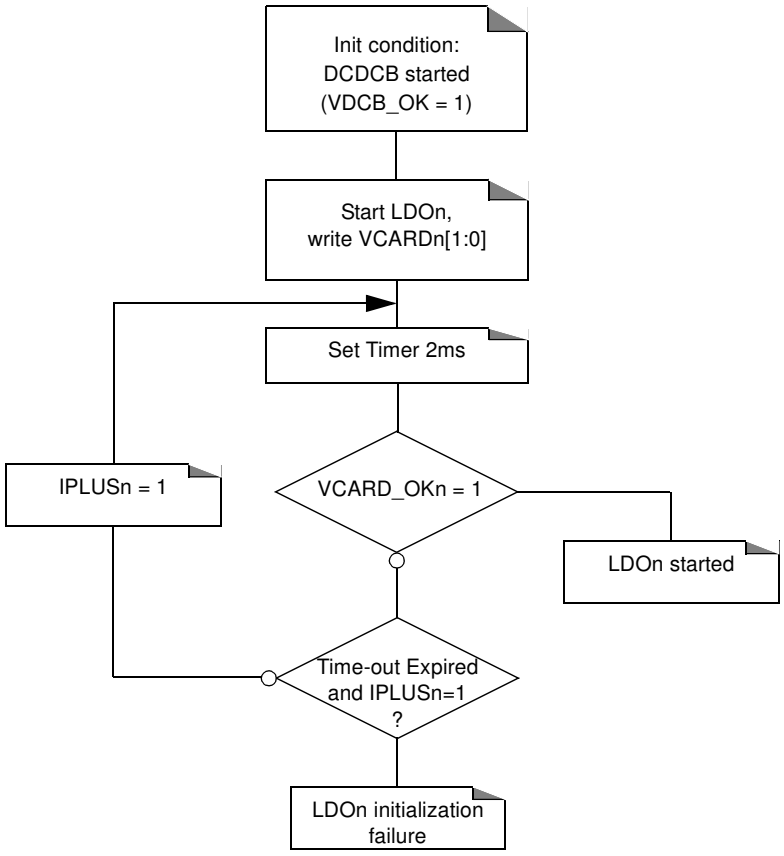
The LDO2, LDO3, LDO4 and LDO5 share the DC/DCB output current, for example 75mA max when CVCCB is pregrammed to 5V. (see Table 62.)

The SC2_FULL bit must be set to use SC2 full interface:

CIO3/CC42 is CC42 and CRST3/CC82 is CC82.

As the power supply of CIO3/CC42 and of CRST3/CC82 is CVCC3, when SC2_FULL=1, CVCC3 = CVCC2. The SC3 interface is disable and LDO3 receives LDO2 command (VCARD3[1:0] = VCARD2[1:0]).

Figure 11. LDOn Initialization Procedure (n = 2, 3, 4, 5)



The LDOn output voltage must be at 0V before to program 1.8V/3V/5V.

Activation Sequence Overview (n=1, 2, 3, 4, 5)

The activation sequence on SC1 is only available if a card is detected on CPRES1 (CARDIN1 bit = 1).

The activation sequence on SC2 is only available if a card is detected on CPRES2 (CARDIN2 bit = 1).

The activation sequence on SC3, SC4, SC5, is only available if DC/DC B is started (VDCB_OK = 1).

The SCn interface starts the activation sequence after a TWI write command in VCARDn[1:0] bits to program the CVCCn voltage.

The SC3, SC4, SC5 interfaces (SIM/SAM interfaces) don't have card presence detector.

After the DC/DC start, the user application will check the ATR to detect if a SIM/SAM is present in the connector.

The automatic reset transition mode (ART=1) controls the CRST pin and check if the first start bit of the ATR respects ISO7816 timings.

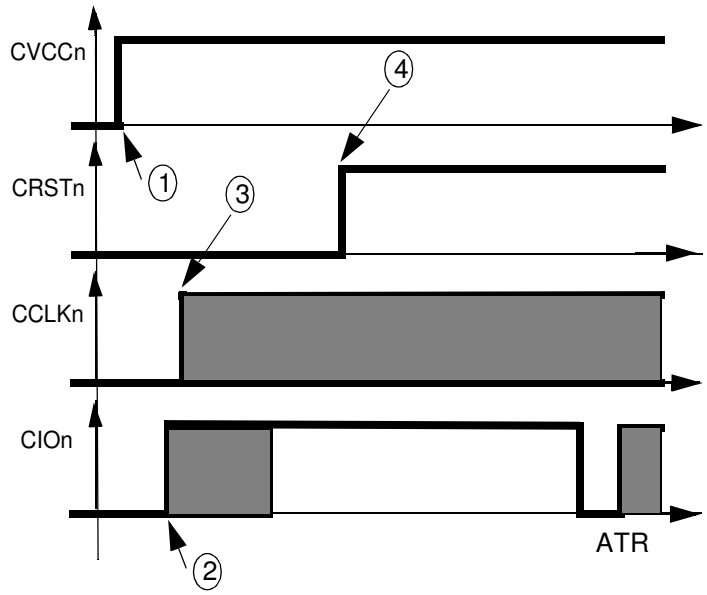
All status bits of an interface (see bits in registers with "This bit is cleared by hardware when this register is read") must be cleared before to start an activation sequence.

Software Activation for SCn interfaces (n=1, 2, 3, 4, 5) with ARTn bit = 0

The activation sequence is controlled by software using TWI commands, depending on the cards to support. For ISO 7816 cards, the following sequence can be applied:

1. Card Voltage is set by software to the required value (VCARDn[1:0] bits). The TWI writing command in VCARDn[1:0] starts the DC/DC (or LDO).
2. Wait of the end of the DC/DC (or LDO) init with a polling on VCARD_OKn bit or wait for $\overline{\text{INT}}$ to go Low. When VCARD_OKn bit is set (by hardware), CARDIOn bit should be set by software.
3. CKSTOPn, IODISn are programmed by software. CKSTOPn bit is reset to have the clock running. IODISn (see IO_SELECT for SC2, SC3, SC4, SC5) is reset to enable the transparent mode on CIOn,CC4n, CC8n.
4. CRSTn pin is controlled by software using CARDRSTn bit.

Figure 14. Software activation without automatic control (ARTn bit = 0)



Note:

– It is assumed that initially VCARDn[1:0], CARDCKn, CARDIOn and CARDRSTn bits are cleared, CKSTOPn and IODISn are set (those bits are further explained in the registers description)

– The user should check the AT83C26 status and possibly resume the activation sequence if one TWI transfer is not acknowledged during the activation sequence.

Software activation for SCn (n=1, 2, 3, 4, 5) interfaces and ARTn bit = 1

The following sequence can be applied:

1. Card Voltage is set by software to the required value (VCARDn1:0] bits in SCn_CFG0 register). This writing starts the DC/DC converter (or LDO).
2. Wait of the end of the DC/DC init (or LDO) with a polling on VCARD_OKn bit or wait for $\overline{\text{INT}}$ to go Low. When VCARD_OKn bit is set (by hardware), CARDIOn bit should be set by software.
3. CKSTOPn, IODISn are programmed by software. CKSTOPn bit is reset to have the clock running. IODISn is reset to enable the transparent mode on CIOn,CC4n, CC8n.
4. CARDRSTn bit is set by software.

Automatic Reset Transition description:

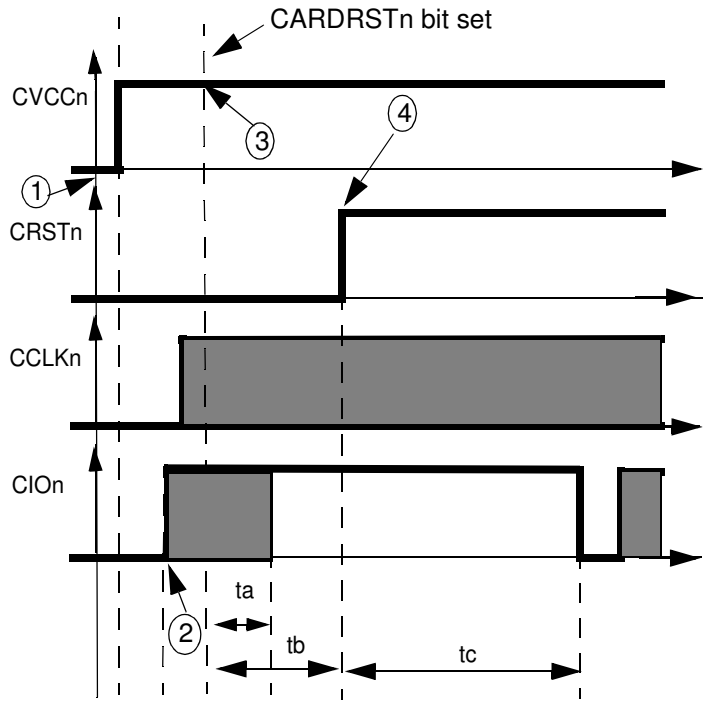
A 16-bit counter starts when CARDRSTn bit is set. It counts card clock cycles. The CRSTn signal is set when the counter reaches the TIMER_MSB and TIMER_LSB value which corresponds to the “tb” time (Figure 15).The counter is reseted when the CRSTn pin is released and it is stopped at the first start bit of the Answer To Request (ATR) on CIOn pin.

The CIOn pin is not checked during the first 200 clock cycles (ta, Figure 15). If the ATR arrives before the counter reaches TIMER_MSB and TIMER_LSB values, the activation sequence fails,

the CRSTn signal is not set and the CAPTURE_MSB and CAPTURE_LSB registers contain the value of the counter at the arrival of the ATR.

If the ATR arrives after the rising edge on CRSTn pin and before the card clock counter overflows (65535 clock cycles), the activation sequence completes. The CAPTURE_MSB and CAPTURE_LSB registers contain the value of the counter at the arrival of the ATR (tc time on Figure 15).

Figure 15. Software activation with ARTn bit = 1



ISO 7816 constraints: ta = 200 card clock cycles

400 card clock cycles< = tb

400 card clock cycles< = tc < = 40000 card clock cycles

Timer[1-0] reset value is 400.

Warm reset (n=1, 2, 3, 4, 5)

The AT83C26 offers a simple and accurate way to control the CRSTn signal during a warm reset.

After an activation sequence (cold reset), a warm reset is started with a low level on CRST during a define delay (between 40000 and 45000 clock cycles for example).

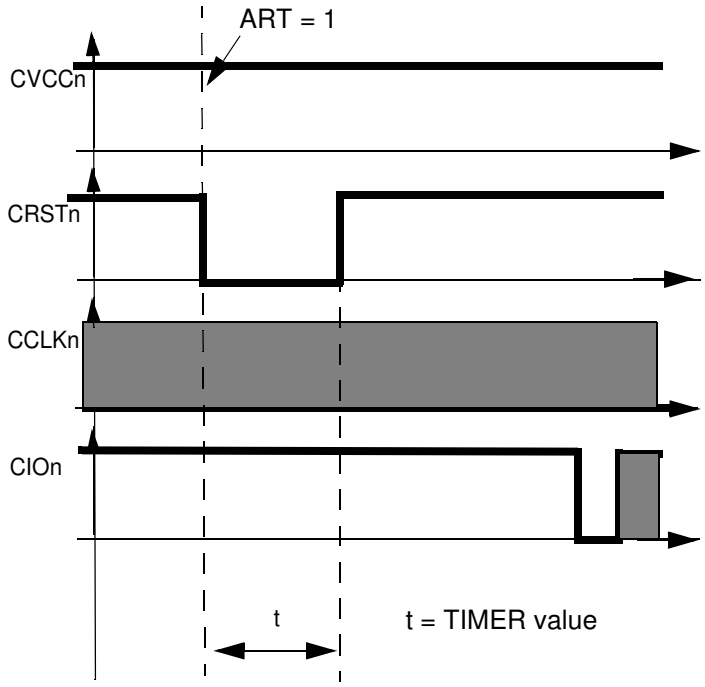
The ARTn bit, the TIMER_MSB and the TIMER_LSB are used to control CRSTn.

The first step is to load the number of CCLK cycles with CRSTn=0 in TIMER registers.

The warm reset is started by setting ART bit (if ART bit is already set, reset ART before).

The CRST signal will be equal to 0 during the number of clock cycles programmed in TIMER_MSB and TIMER_LSB. Then, the CRST signal will be at 1.

Figure 16. Warm reset with ARTn bit = 1



Deactivation Sequence Overview

The deactivation sequence should follows the order defined in ISO7816-3 specification. The AT83C26 has two deactivation modes:

- Standard deactivation mode: This mode is used to stop exchange with smart card when the AT83C26 power supply is present. The DCCLK signal is used for deactivation sequence timings.
- Emergency deactivation mode: This mode is used when the AT83C26 power supply is took off.

Deactivation sequence on SCn interface (n=1, 2, 3, 4, 5)

The card automatic deactivation is triggered when one the following condition occurs:

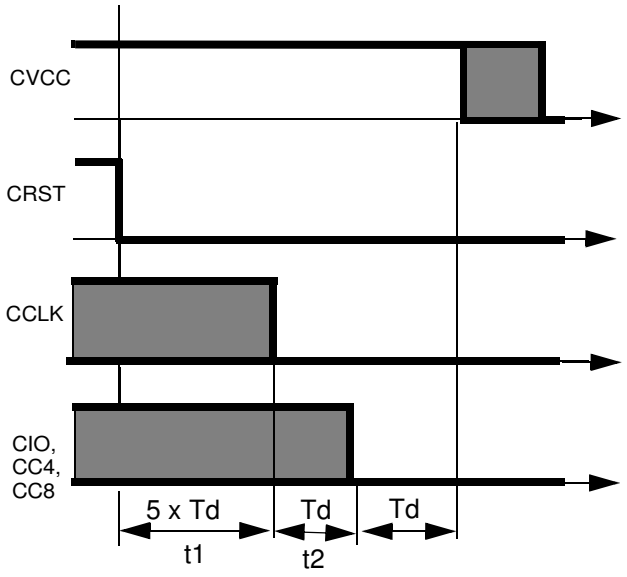
- ICARDERR1 bit is set by hardware (SC1)
- VCARDERRn bit is set by hardware (or by software)
- INSERT1 is set and CARDIN1 is cleared (SC1)
- INSERT2 is set and CARDIN2 is cleared (SC2)
- SHUTDOWNA bit is set by software (SC1)
- SHUTDOWNB bit is set by software (SC2, SC3, SC4, SC5)

- Reset pin going low (SC1, SC2, SC3, SC4, SC5)
- Power Fail (VPFDP)

It is a self-timed sequence which cannot be interrupted when started (see Figure 17). Each step is separated by a delay based on Td equal to 8 periods of DCCLK, typically 2 to 2.4 µs:

1. T0: CARDRSTn is cleared, SHUTDOWNA (for SC1) bit is set.
2. T0 + 5 x Td:CARDCKn is cleared, CKSTOPn, CARDIOn and IODIS are set.
3. T0 + 6 x Td: CARDIOn is cleared.
4. T0 + 7 x Td: VCARDn[1:0] = 00.

Figure 17. Deactivation Sequence



Notes:
1. Setting ICARDERR1 by software does not trigger a deactivation on SC1. VCARDERRn can be used to deactivate the card by software.
2. If CCLKn=A2 or A2/2, deactivation follows fig13 with 2 timing modifications: t1=5.5*Td and t2=0.5*Td.
3. Td is based on DCCLK clock.

Emergency deactivation sequence on SCn interface (n=1, 2, 3, 4, 5)

The card emergency automatic deactivation is triggered when one the following condition occurs:

- Software TWI Reset (SC1, SC2, SC3, SC4, SC5)
- Power fail on VCC (SC1, SC2, SC3, SC4, SC5)

If the power supply is disconnected, a standard deactivation is started when VCC = VPFDP. When VCC is equal to VPFDM, the emergency deactivation occurs and eventually ends the standard deactivation.

Figure 18. Power Fail Detection

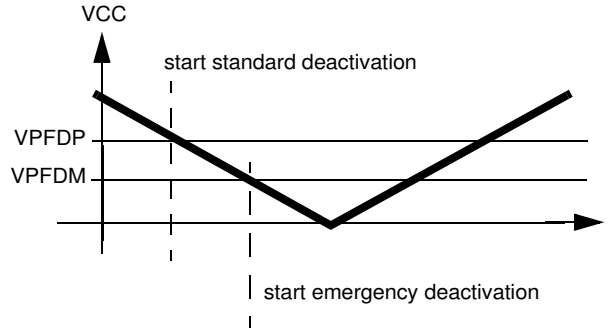
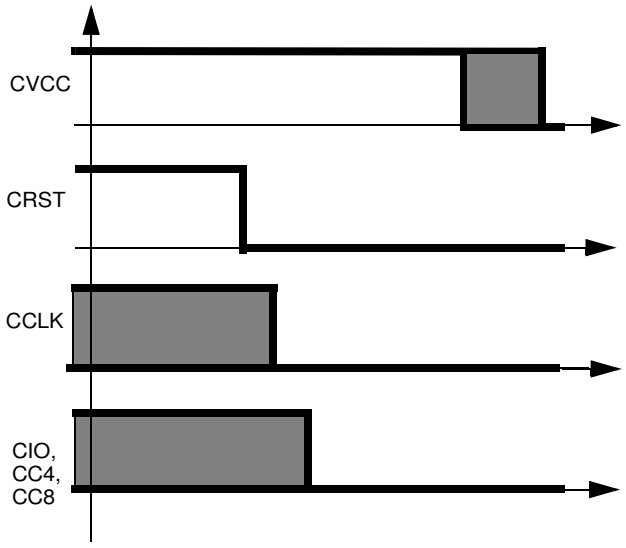


Figure 19. Emergency deactivation sequence



During an emergency deactivation, the signals fall according to the order described in Fig18.

Transparent mode

Full transparent mode on SCn interfaces (n=1, 2)

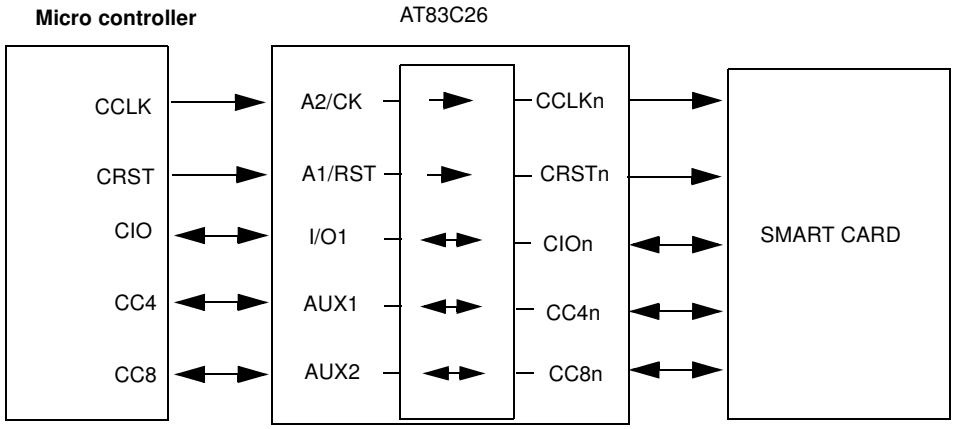
If the micro controller outputs ISO 7816 signals, a transparent mode allows to connect, CCLK, CIO, CRST, CC4 and CC8 signals on outputs after an electrical level control. The AT83C26 level shifters adapt the card signals to the smart card voltage selection.

The CCLK micro controller signal can be connected to the A2/CK pins (see CKSn[2:0]).

CKSn[2:0] bits allow to select standard or transparent configuration for the CCLKn pin. A2/CK inputs always give the TWI address at reset.

If A2/CK input is tied to the host micro controller and its reset value is unknown, a general call on the TWI bus allows to reset all the AT83C26 devices and set its address after A2/CK input is fixed.

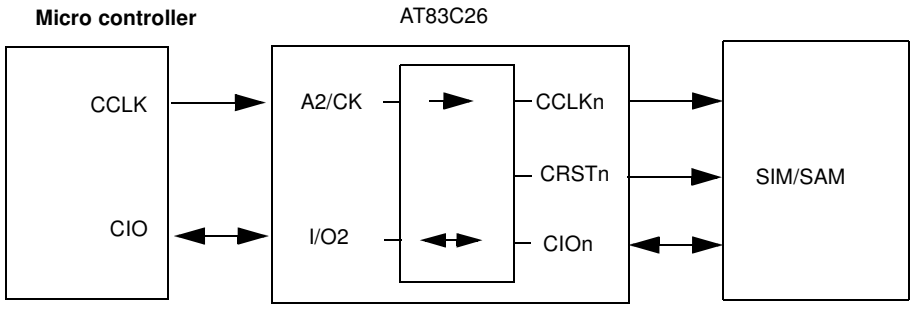
Figure 20. Transparent Mode Description



Full transparent mode on SCn interfaces (n= 3, 4, 5)

The transparent mode with A2/CK is also available for SC3, SC4 and SC5 interfaces without CC4 and CC8.

Figure 21. Transparent Mode Description



Interrupts

The $\overline{INT}$ output is High by default. $\overline{INT}$ is driven Low by at least one of the following event:

- INSERT1 or INSERT2 bits set (card insertion/extraction or bit set by software)
- VCARD_INTn (n=1,2,3,4,5) bits set (the DC/DC A or LDO2 to LDO5 output voltage has settled)
- VDCB_INT bit set (the DC/DC B output voltage has settled)
- over-current detection on CVCC1
- VCARDERRn bit set (out of range voltage on CVCCn or bit set by software) (n=1,2,3,4,5)
- ATRERRn bit set (no ATR before the card clock counter overflows or bit set by software) (n=1,2,3,4,5)

Several AT83C26 devices can share the same interrupt pin and the micro controller can identify the interrupt sources by polling the interrupt bits of the AT83C26 devices using TWI commands.

A TWI read command of the interrupt bit corresponding to the IT clears the bit. When all IT bits are cleared, the $\overline{INT}$ output becomes high.

The ITDIS register contains 4 bits to control SCn interrupts (n= 2,3,4,5). If ITDISn bit is set, the flags are set but the $\overline{INT}$ pin isn't driven low if an interrupt event appears.

Table 4. Interrupt bits description

Bit name	Register name	Mask on $\overline{INT}$ pin	Remark
INSERT1	SC1_CFG0		Smart card inserted/extracted in SC1
INSERT2	SC2_CFG0	ITDIS2	Smart card inserted/extracted in SC2
VCARD_INT1	SC1_STATUS		VCARD_OK1 is set
VCARD_INT2	SC2_CFG0	ITDIS2	VCARD_OK2 is set
VCARD_INT3	SC3_CFG0	ITDIS3	VCARD_OK3 is set
VCARD_INT4	SC4_CFG0	ITDIS4	VCARD_OK4 is set
VCARD_INT5	SC5_CFG0	ITDIS5	VCARD_OK5 is set
VDCB_INT	DCDCB		VDCB_OK is set
ICARDERR1	SC1_CFG0		Over current on DCDCA.
VCARDERR1	SC1_CFG0		Ouput voltage out of range on DCDCA
VCARDERR2	SC2_CFG0	ITDIS2	Ouput voltage out of range on LDO2
VCARDERR3	SC3_CFG0	ITDIS3	Ouput voltage out of range on LDO3.
VCARDERR4	SC4_CFG0	ITDIS4	Ouput voltage out of range on LDO4
VCARDERR5	SC5_CFG0	ITDIS5	Ouput voltage out of range on LDO5
ATRERR1	SC1_CFG0		Error on SC1 for ATR reception in automatic mode
ATRERR2	SC2_CFG0	ITDIS2	Error on SC2 for ATR reception in automatic mode
ATRERR3	SC3_CFG0	ITDIS3	Error on SC3 for ATR reception in automatic mode
ATRERR4	SC4_CFG0	ITDIS4	Error on SC4 for ATR reception in automatic mode
ATRERR5	SC5_CFG0	ITDIS5	Error on SC5 for ATR reception in automatic mode

After the reading and the clear of the interrupt bits, several bits are used to control the status.

Table 5. Status bits description

Bit name	Register name	Remark
CARDIN1	SC1_STATUS	Smart card presence in SC1
CARDIN2	SC1_STATUS	Smart card presence in SC2
VCARD_OK1	SC1_STATUS	CVCC1 voltage in range programmed in VCARD1[1:0]
VCARD_OK2	SC2_CFG0	CVCC2 voltage in range programmed in VCARD2[1:0]
VCARD_OK3	SC3_CFG0	CVCC3 voltage in range programmed in VCARD3[1:0]
VCARD_OK4	SC4_CFG0	CVCC4 voltage in range programmed in VCARD4[1:0]
VCARD_OK5	SC5_CFG0	CVCC5 voltage in range programmed in VCARD5[1:0]
VDCB_OK	DCDCB	CVCCB voltage in range programmed in VDCB[1:0]

The status for the ICARDERR1 and VCARDERRn (n= 1 to 5) bits is controlled with VCARD_OKn bits.

The status for the ATRERRn (n= 1 to 5) is controlled by reading of values in CAPTURE_MSB and CAPTURE_LSB.

Slew rate control

The AT83C26 proposed a slew rate control on CIOn and CCLKn pins (n=1, 2, 3, 4, 5). The control operates on rising and falling edges of CCLKn and only on rising edge of CIOn.

Four modes are available:

- Automatic mode: The slew rate depends on VCARDn[1:0] value. The slew rate value is optimized according to CVCCn.
- Mode 1, 2 , 3 (1.8V, 3V, 5V): The user can forced the slew rate if needed. For example if CVCCn = 5V, the user can program 1.8V or 3V to speed up the slew rate in case of long wire connection between AT83C26 and smart cards.

Power down mode

SHUTDOWNA bit and SHUTDOWNB bit must be set to activate power down mode on DCDCA and DCDCB converters.

If SHUTDOWNA = SHUTDOWNB = 1, the AT83C26 internal regulator also enters in power down mode. The consumption is then about 30µA.

To exit from power down mode, TWI commands are needed to clear SHUTDOWNA and SHUTDOWNB.

Write Commands

The write commands are:

1. General Call Reset:

   A general call followed by the value 06h has the same effect as a Reset command.

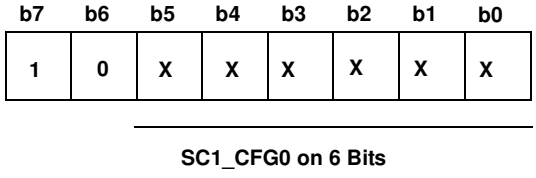
2. Reset:

   Initialize all the logic and the TWI interface as after a power-up or power-fail reset. If the interface is activated, an emergency de-activation sequence is also performed. This is a one-byte command.

3. Write SC1_CFG0, SC1_CFG1, SC1_CFG2, SC1_CFG3, SC1_CFG4:

   Configure the device according to the last six bits in the SC1_CFG0 register and to the following four bytes in SC1_CFG1, SC1_CFG2, SC1_CFG3 then SC1_CFG4 registers. This is a five bytes command.

Figure 22. Command byte format for Write SC1_CFG0 command



4. Write TIMER_MSB, TIMER_LSB:

   Program the 16-bit automatic reset transition timer with the following two bytes. This is a three bytes command.

5. Write SC1_INTERFACE:

   Program the interface byte. This is a one-byte command. The MSB of the command byte is fixed at 0.

6. Write common config smart cards:

   IO_SELECT, INTERFACE_B, ITDIS:

   Configuration of parameters for smart card interfaces.

7. Write SC2 interface: SC2_CFG0, SC2_CFG1, SC2_CFG2

   Configuration of smart card interface 2.

8. Write SC3 interface: SC3_CFG0, SC3_CFG2

   Configuration of SIM/SAM interface 3.

9. Write SC4 interface: SC4_CFG0, SC4_CFG2

   Configuration of SIM/SAM interface 4.

10. Write SC5 interface: SC5_CFG0, SC5_CFG2
    Configuration of SIM/SAM interface 5.

11. Write DCDCB config: DCDCB, LDO
    Configuration of DCDCB converter.

12. Write SLEW_CTRL config: SLEW_CTRL_1, SLEW_CTRL_2, SLEW_CTRL_3
    Configuration of slew rate for CCLKn and CIOn (n = 1, 2, 3, 4, 5).

Table 6. Write Commands Description

	Address Byte (See Table 2)	**Command Byte**	**Data Byte 1**	**Data Byte 2**	**Data Byte 3**	**Data Byte 4**
		[0]	[1]	[2]	[3]	[4]
1. General Call Reset	0000 0000	0000 0110				
2. Reset	0100 XX10	1111 1111				
3. Write config	0100 XX10	(10 + SC1_CFG0 6 bits)	SC1_CFG1	SC1_CFG2	SC1_CFG3	SC1_CFG4
4. Write Timer	0100 XX10	1111 1100	TIMER_MSB	TIMER_LSB		
5. Write Interface	0100 XX10	(0+SC1_INTERFACE 7 bits)				
6.Write Config SC on DCDCB	0100 XX10	1111 1000	IO_SELECT	INTERFACE_B	ITDIS	
7. Write SC2 interface	0100 XX10	1111 1001	SC2_CFG0	SC2_CFG1	SC2_CFG2	
8. Write SC3 interface	0100 XX10	1111 1010	SC3_CFG0	SC3_CFG2		
9. Write SC4 interface	0100 XX10	1111 1011	SC4_CFG0	SC4_CFG2		
10. Write SC5 interface	0100 XX10	1111 1101	SC5_CFG0	SC5_CFG2		
11. Write DCDCB config	0100 XX10	1111 1110	DCDCB	LDO		
12. Write SLEW_CTRL config	0100 XX10	1111 0111	SLEW_CTRL_1	SLEW_CTRL_2	SLEW_CTRL_3	

Read Command

After a write command, even with a length of 0 byte, the next read operation is performed on the corresponding byte. The write command sets the “read pointer”.

After the reset, the “read pointer” is on SC1 registers

FFh is completing the transfer if the micro controller attempts to read beyond the last byte.

Flags are only reseted after the corresponding byte read has been acknowledged by the master.

Figure 23. Read command byte

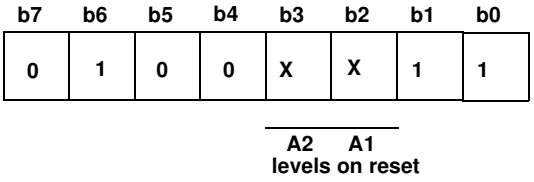


Table 7. Read Commands Description

	1. After reset or write command number 2, 3, 4	2. After write command number 6	3. After write command number 7	4. After write command number 8	5. After write command number 9	6. After write command number 10	7. After write command number 11	8. After write command number 12
[0]	SC1_STATUS	STATUSB	SC2_CFG0	SC3_CFG0	SC4_CFG0	SC5_CFG0	DCDCB	SLEW_CTRL_1
[1]	SC1_CFG0	IO_SELECT	SC2_CFG1	SC3_CFG2	SC4_CFG2	SC5_CFG2	LDO	SLEW_CTRL_2
[2]	SC1_CFG1	INTERFACE_B	SC2_CFG2	0xFF	0xFF	0xFF	0xFF	SLEW_CTRL_3
[3]	SC1_CFG2	ITDIS	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[4]	SC1_CFG3	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[5]	SC1_CFG4	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[6]	SC1_INTERFACE	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[7]	TIMER_MSB	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[8]	TIMER_LSB	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[9]	CAPTURE_MSB	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[10]	CAPTURE_LSB	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
[11]	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

Registers summary

The table below gives a quick view on AT83C26 registers.

Table 8. Smart card 1 interface registers

	7	6	5	4	3	2	1	0
SC1_CFG0	1	0	ATRERR1	INSERT1	ICARDERR1	VCARDERR1	VCARD11	VCARD10
SC1_CFG1	X	ART1	SHUTDOWNA	CARDDET1	PULLUP1	CDS12	CDS11	CDS10
SC1_CFG2	0	DCK2	DCK1	DCK0	X	CKS12	CKS11	CKS10
SC1_CFG3	X	X	X	ICCADJA	X	X	X	X
SC1_CFG4	X	DEMBOOSTA1	DEMBOOSTA0	STEPREGA	INT_PULLUP	X	X	CRST_SEL1
SC1_INTERFACE	0	IODIS1	CKSTOP1	CARDRST1	CARDC81	CARDC41	CARDCK1	CARDIO1
SC1_STATUS	CC81	CC41	CARDIN1	VCARD_OK1	X	VCARD_INT1	CRST1	CIO1

Table 9. Smart card 2 interface registers

	7	6	5	4	3	2	1	0
SC2_CFG0	VCARD_INT2	VCARD_OK2	ATRERR2	INSERT2	X	VCARDERR2	VCARD21	VCARD20
SC2_CFG1	X	X	SC2_FULL	CARDDET2	PULLUP2	CDS22	CDS21	CDS20
SC2_CFG2	ART2	CRST_SEL2	CARDRST2	CARDCK2	CKSTOP2	CKS22	CKS21	CKS20

Table 10. SIM/SAM 3 interface registers

	7	6	5	4	3	2	1	0
SC3_CFG0	VCARD_INT3	VCARD_OK3	ATRERR3	X	X	VCARDERR3	VCARD31	VCARD30
SC3_CFG2	ART3	X	CARDRST3	CARDCK3	CKSTOP3	CK32	CKS31	CKS30

Table 11. SIM/SAM 4 interface registers

	7	6	5	4	3	2	1	0
SC4_CFG0	VCARD_INT4	VCARD_OK4	ATRERR4	X	X	VCARDERR4	VCARD41	VCARD40
SC4_CFG2	ART4	X	CARDRST4	CARDCK4	CKSTOP4	CKS42	CKS41	CKS40

Table 12. SIM/SAM 5 interface registers

	7	6	5	4	3	2	1	0
SC5_CFG0	VCARD_INT5	VCARD_OK5	ATRERR5	X	X	VCARDERR5	VCARD51	VCARD50
SC5_CFG2	ART5	X	CARDRST5	CARDCK5	CKSTOP5	CKS52	CKS51	CKS50

Table 13. Common registers for SC1/SC2/SC3/SC4/SC5

	7	6	5	4	3	2	1	0
TIMER_MSB	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TIMER_LSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CAPTURE_MSB	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CAPTURE_LSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IO_SELECT	X	X	X	X	IOSEL3	IOSEL2	IOSEL1	IOSEL0

Table 14. Common registers for SC2/SC3/SC4/SC5

	7	6	5	4	3	2	1	0
INTERFACEB	X	CARDC82	CARDIO5	CARDIO4	CARDIO3/ CARDC42	CARDIO2	DEMBOOSTB1	DEMBOOSTB0
STATUSB	X	CARDIN2	CIO5	CIO4	CRST3/ CC82	CIO3/ CC42	CRST2	CIO2
ITDIS	IODIS5	IODIS4	IODIS3	IODIS2	ITDIS5	ITDIS4	ITDIS3	ITDIS2

Table 15. DC/DC B registers

	7	6	5	4	3	2	1	0
DCDCB	SHUTDOWNB	VDCB_INT	VDCB_OK	0	ICCADJB	STEPREGB	VDCB1	VDCB0
LDO	IPLUS5	IPLUS4	IPLUS3	IPLUS2	1	1	1	1

Table 16. Slew control registers for CIO and CCLK pins

	7	6	5	4	3	2	1	0
SLEW_CTRL_1	CCLK2_SLEW_CTRL1	CCLK2_SLEW_CTRL0	CIO2_SLEW_CTRL1	CIO2_SLEW_CTRL0	CCLK1_SLEW_CTRL1	CCLK1_SLEW_CTRL0	CIO1_SLEW_CTRL1	CIO1_SLEW_CTRL0
SLEW_CTRL_2	CCLK4_SLEW_CTRL1	CCLK4_SLEW_CTRL0	CIO4_SLEW_CTRL1	CIO4_SLEW_CTRL0	CCLK3_SLEW_CTRL1	CCLK3_SLEW_CTRL0	CIO3_SLEW_CTRL1	CIO3_SLEW_CTRL0
SLEW_CTRL_3	X	X	X	X	CCLK5_SLEW_CTRL1	CCLK5_SLEW_CTRL0	CIO5_SLEW_CTRL1	CIO5_SLEW_CTRL0

Registers

Table 17. SC1_ CFG0(Config Byte 0 for SC1)

7	6	5	4	3	2	1	0
1	0	ATRERR1	INSERT1	ICARDERR1	VCARDERR1	VCARD11	VCARD10

Bit Number	Bit Mnemonic	Description
7-6	1-0	These bits cannot be programmed and are read as 1-0.
5	ATRERR1	Answer to Reset Interrupt for SC1 This bit is set when the card clock counter overflows (no falling edge on CIO1 is received before the overflow of the card clock counter). This bit is cleared by hardware when this register is read. It can be set by software for test purpose.
4	INSERT1	Card Insertion Interrupt This bit is set when a card is inserted or extracted: a change in CARDIN value filtered according to CDS[2-0]. It can be set by software for test purpose. This bit is cleared by hardware when this register is read. It cannot be cleared by software.
3	ICARDERR1	Card Over Current Interrupt This bit is set when an over current is detected on CVCC. It can be set by software for test purpose (no card deactivation is performed). This bit is cleared by hardware when this register is read. It cannot be cleared by software.
2	VCARDERR1	Card Out of Range Voltage Interrupt This bit is set when the output voltage goes out of the voltage range specified by VCARD field. It can be set by software for test purpose and deactivate the card. This bit is cleared by hardware when this register is read. It cannot be cleared by software.
1-0	VCARD1[1:0]	Card Voltage Selection VCARD1[1:0] = 00: 0V VCARD1[1:0] = 01: 1.8V VCARD1[1:0] = 10: 3V VCARD1[1:0] = 11: 5V VCARD1[1:0] writing to 1.8V, 3V, 5V starts the DC/DC if a card is detected. VCARD1[1:0] writing to 0 stops the DC/DC. No card deactivation is performed when the voltage is changed between 1.8V, 3V or 5V. The micro controller should deactivate the card before changing the voltage.

Reset value = 0x 1000 0000

Table 18. SC1_CFG1 (Config Byte 1 for SC1

7	6	5	4	3	2	1	0
X	ART1	SHUTDOWNA	CARDDET1	PULLUP1	CDS12	CDS11	CDS10

Bit Number	Bit Mnemonic	Description
7	X	
6	ART1	Automatic Reset Transition Set this bit to have the CRST1 pin changed according to activation sequence. Clear this bit to have the CRST1 pin immediately following the value programmed in CARDRST1.
5	SHUTDOWNA	Shutdown DC/DCA Set this bit to reduce the power consumption. An automatic de-activation sequence will be done. VCARD[1:0] bits are reset. Clear this bit to enable VCARD1[1:0] selection.
4	CARDDET1	Card Presence Detection Polarity Set this bit to indicate the card presence detector is closed when no card is inserted (CPRES is low). Clear this bit to indicate the card presence detector is open when no card is inserted (CPRES is high).
3	PULLUP1	Pull-up Enable Set this bit to enable the internal pull-up on the CPRES pin. This allows to minimize the number of external components. Clear this bit to disable the internal pull-up and minimize the power consumption when the card detection contact is on. Then an external pull-up must be connected to V_{CC} (typically a 1 MΩ resistor).
2-0	CDS1[2:0]	Card Detection filtering CPRES1 is sampled by the master clock provided on CLK input. A change on CPRES1 is detected after: CDS1[2-0] = 0: no sample(1) CDS1[2-0] = 1: 4 identical samples CDS1[2-0] = 2: 8 identical samples (reset value) CDS1[2-0] = 3: 16 identical samples CDS1[2-0] = 4: 32 identical samples CDS1[2-0] = 5: 64 identical samples CDS1[2-0] = 6: 128 identical samples CDS1[2-0] = 7: 256 identical samples Note: 1. When CDS[2-0] = 0, a card insertion (even if CLK is stopped) puts a low level on $\overline{INT}$ pin. This can be used to wake up the external micro controller and restart CLK when a card is inserted in the AT83C24.

Reset value = 0x X000 1010

Table 19. SC1_CFG2 (Config Byte 2 for SC1)

7	6	5	4	3	2	1	0
0	**DCK2**	**DCK1**	**DCK0**	**X**	**CKS12**	**CKS11**	**CKS10**

Bit Number	Bit Mnemonic	Description
7	0	This bit must be always at 0.
6-4	DCK[2:0]	DCK is the first level of prescaler factor. CLK signal is divided by the prescaler value and outputs DCCLK signal. DCCLK is an input for CCLK prescaler. DCK[2:0] = 0: prescaler factor equals 1 DCK[2:0] = 1: prescaler factor equals 2 DCK[2:0] = 2: prescaler factor equals 4 DCK[2:0] = 3: prescaler factor equals 6 DCK[2:0] = 4: prescaler factor equals 8 DCK[2:0] = 5: prescaler factor equals 10 DCK[2:0] = 6: prescaler factor equals 12 DCK[2:0] = 7: Reserved DCCLK is used for pad management and dectivation sequence.
3	X	
2-0	CKS1[2:0]	Card Clock prescaler factor for CCLK1. CKS1 [2:0] = 0: CCLK1 = CLK (the maximum frequency on CLK is 24 MHz) CKS1 [2:0] = 1: CCLK1 = DCCLK CKS1[2:0] = 2: CCLK1 = DCCLK / 2 CKS1[2:0] = 3: CCLK1 = DCCLK / 4 CKS 1[2:0] = 4: CCLK1 = A2 CKS1 [2:0] = 5: CCLK1 = A2 / 2 CKS1[2:0] = 6: CCLK1 = CLK / 2 CKS1 [2:0] = 7: CCLK1 = CLK / 4

Reset value = 0x 0001 X000

Notes:
1. When CKS1 value is changed a special logic insures no glitch occurs on the CCLK1 pin and actual configuration changes can be delayed by half a period to two periods of CCLK1.
2. CCLK1 must be stopped with CKSTOP1 bit before switching from CKS1 = (0, 1, 2, 3, 6, 7) to CKS1 = (4, 5) or vice versa.

Table 20. SC1_CFG3 (Config Byte 3 for SC1)

7	6	5	4	3	2	1	0
X	X	X	ICCADJA	X	X	X	X

Bit Number	Bit Mnemonic	Description
7-5	X	

Bit Number	Bit Mnemonic	Description
4	ICCADJA	CI_{CC} overflow adjust This bit controls the DC/DCA sensitivity to any overflow current. Set this bit to decrease the DC/DCA sensitivity (CI_{CC_ovf} is increased by about 20%). Clear this bit to have a normal configuration. The reset value is 0.
3	X	
2	X	
1	X	
0	X	

Reset value = 0x XXX0 XXXX

Table 21. SC1_CFG4 (Config Byte 4 for SC1)

7	6	5	4	3	2	1	0
X	DEMBOOSTA1	DEMBOOSTA0	STEPREGA	INT_PULLUP	X	X	CRST_SEL1

Bit Number	Bit Mnemonic	Description
7	X	

Bit Number	Bit Mnemonic	Description
6-5	DEMBOOSTA[1-0]	DC/DC A Maximum Startup Current drawn from power supply 00: Normal: 80 mA average 01: Normal + 18% 10: Normal + 18% (and boost on oscillator) 11: Normal + 40%
4	STEPREGA	Step Regulator mode Clear this bit to enable the automatic step-up converter (CVCC is stable even if VCC is not higher than CVCC). Set this bit to permanently disable the step-up converter (CVCC is stable only if VCC is sufficiently higher than CVCC). This bit must always be set if no external self is used
3	INT_PULLUP	Internal pull-up Set this bit to activate the internal pull-up (connected internally to VCC) on $\overline{INT}$ pin. Clear this bit to deactivate the internal pull-up.
2	X	
1	X	
0	CRST_SEL1	Card Reset Selection Set this bit to have the CRST1 pin driven by hardware through the A1/RST pin. Clear this bit to have the CRST1 pin driven by software through the CARDRST bit. The reset value is 0.

Reset value = 0x X000 0000

Table 22. SC1_INTERFACE (Interface Byte for SC1)

7	6	5	4	3	2	1	0
0	**IODIS1**	**CKSTOP1**	**CARDRST1**	**CARDC81**	**CARDC41**	**CARDCK1**	**CARDIO1**

Bit Number	Bit Mnemonic	Description
7	0	This bit should not be set.
6	IODIS1	Card I/O isolation Set this bit to drive the CIO1, CC41, CC81 pins according to CARDIO1, CARDC41, CARDC81 respectively. Clear this bit to drive the CIO1, CC41 and CC81 pins connected to inputs according to IOSEL[3/0] bits.
5	CKSTOP1	CARD Clock Stop Set this bit to stop CCLK1 according to CARDCK1. This can be used to set asynchronous cards in power-down mode (GSM) or to drive CCLK1 by software. Clear this bit to have CCLK1 running according to CKS1. This can be used to activate asynchronous cards. Note: When this bit is changed a special logic ensures that no glitch occurs on the CCLK1 pin and actual configuration changes can be delayed by half a period to two periods of CCLK1.
4	CARDRST1	Card Reset Set this bit to enter a reset sequence according to ART1 bit value. Clear this bit to drive a low level on the CRST1 pin.
3	CARDC81	Card C8 Set this bit to drive the CC81 pin High with the on-chip pull-up (according to IODIS1 bit value). The pin can then be an input (read in SC1_STATUS register). Clear this bit to drive a low level on the CC81 pin (according to IODIS1 bit value).
2	CARDC41	Card C4 Set this bit to drive the CC41 pin High with the on-chip pull-up (according to IODIS1 bit value). The pin can then be an input (read in SC1_STATUS register). Clear this bit to drive a low level on the CC41 pin (according to IODIS1 bit value).
1	CARDCK1	Card Clock Set this bit to set a high level on the CCLK1 pin (according to CKSTOP1 bit value). Clear this bit to drive a low level on the CCLK1 pin.
0	CARDIO1	Card I/O Set this bit to drive the CIO1 pin High with the on-chip pull-up (according to IODIS1 bit value). The pin can then be an input (read in SC1_STATUS register). Clear this bit to drive a low level on the CIO1 pin (according to IODIS1 bit value).

Reset value = 0x 0110 0000

Table 23. SC1_STATUS (Status Byte for SC1)

7	6	5	4	3	2	1	0
CC81	CC41	CARDIN1	VCARD_OK1	X	VCARD_INT1	CRST1	CIO1

Bit Number	Bit Mnemonic	Description
7	CC81	Card CC8 This bit provides the actual level on the CC8 pin when read.

Bit Number	Bit Mnemonic	Description
6	CC41	Card CC4 This bit provides the actual level on the CC4 pin when read.
5	CARDIN1	Card Presence Status This bit is set when a card is detected. It is cleared otherwise.
4	VCARD_OK1	SC1 Voltage Status This bit is set by the DCDCA when the output voltage remains within the voltage range specified by VCARD1[1:0] bits. It is cleared otherwise.
3	X	
2	VCARD_INT1	SC1 Smart Card voltage interrupt This bit is set when VCARD_OK1 bit is set. This bit is cleared when read by the micro controller.
1	CRST1	Card RST This bit provides the actual level on the CRST pin when read.
0	CIO1	Card I/O This bit provides the actual level on the CIO pin when read.

Reset value = reset value depends on hardware configuration

Table 24. SC2_CFG0 ()

7	6	5	4	3	2	1	0
VCARD_INT2	**VCARD_OK2**	**ATRERR2**	**INSERT2**	**X**	**VCARDERR2**	**VCARD21**	**VCARD20**

Bit Number	Bit Mnemonic	Description
7	VCARD_INT2	SC2 voltage interrupt This bit is set when VCARD_OK2 bit is set. This bit is cleared when read by the micro controller.
6	VCARD_OK2	SC2 Voltage Status This bit is set by the LD02 when the output voltage remains within the voltage range specified by VCARD2[1:0] bits. It is cleared otherwise.
5	ATRERR2	Answer to Reset Interrupt for SC2 This bit is set when the card clock counter overflows (no falling edge on CIO2 is received before the overflow of the card clock counter). This bit is cleared by hardware when this register is read. It can be set by software for test purpose.
4	INSERT2	Card Insertion Interrupt This bit is set when a card is inserted or extracted in SC2 connector: a change in CARDIN2 value filtered according to CDS2[2-0]. It can be set by software for test purpose. This bit is cleared by hardware when this register is read. It cannot be cleared by software.
3	X	
2	VCARDERR2	Interface 2 Card Out of Range Voltage Interrupt This bit is set when the output voltage on $CVCC_N$ goes out of the voltage range specified by VCRDN field. It can be set by software for test purpose and deactivate the card. This bit is cleared by hardware when this register is read. It cannot be cleared by software. The reset value is 0.
1-0	VCARD2[1:0]	Interface 2 Card Voltage Selection VCRD2[1:0] = 00: 0V VCRD2[1:0] = 01: 1.8V class C VCRD2[1:0] = 10: 3V class B VCRD2[1:0] = 11: 5V class A No card deactivation is performed when the voltage is changed. The micro controller should deactivate the card before changing the voltage and activating the card again. The reset value is 00.

Reset value = 0x 0000 X000

Table 25. SC2_CFG1 ()

7	6	5	4	3	2	1	0
X	X	SC2_FULL	CARDDET2	PULLUP2	CDS22	CDS21	CDS20

Bit Number	Bit Mnemonic	Description
7-6	X	
5	SC2_FULL	Set this bit to activate full IO interface on Smart card 2: • CIO3/CC42 is CC42 and CRST3/CC82 is CC82. • Interface 3 LDO is disabled. • CARDCK3 is reset and CKSTOP3 to stop CCLK on SC3. • ITDIS3 is set to disable interrupts from SC3. CVCC2 and CVCC3 shall be connected externally and SC2_FULL must be set before activating the LDO. Clear this bit only to use only CIO on interface 2: • CIO3/CC42 is CIO3 and CRST3/CC82 is CRST3. • Interface 3 can then be used independently to connect a SIM/SAM card. The reset value is 1.
4	CARDDET2	Card Presence Detection Polarity - Interface 2 Set this bit to indicate the card presence detector is closed when no card is inserted (CPRES2 is low). Clear this bit to indicate the card presence detector is open when no card is inserted (CPRES2 is high). The reset value is 0.
3	PULLUP2	Pull-up Enable Set this bit to enable the internal pull-up on the CPRES2 pin. This allows to minimize the number of external components. Clear this bit to disable the internal pull-up and minimize the power consumption when the card detection contact is on. Then an external pull-up must be connected to V_{CC} (typically a 1 MΩ resistor). The reset value is 1.
2-0	CDS2[2:0]	Card Detection filtering - Interface 2 CPRES2 is sampled by the master clock provided on CLK input. A change on CPRES2 is detected after: CDS2[2-0] = 0: no sample(1) CDS2[2-0] = 1: 4 identical samples CDS2 [2-0] = 2: 8 identical samples (reset value) CDS2[2-0] = 3: 16 identical samples CDS2[2-0] = 4: 32 identical samples CDS2[2-0] = 5: 64 identical samples CDS2[2-0] = 6: 128 identical samples CDS2[2-0] = 7: 256 identical samples Note: 1. When CDS2[2-0] = 0 and ITDIS2 = 0, a card insertion (even if CLK is stopped) puts a low level on $\overline{INT}$ pin. This can be used to wake up the external micro controller and restart CLK when a card is inserted in the AT83C24.

Reset value = 0x XX10 1010

Table 26. SC2_CFG2 ()

7	6	5	4	3	2	1	0
ART2	**CRST_SEL2**	**CARDRST2**	**CARDCK2**	**CKSTOP2**	**CKS22**	**CKS21**	**CKS20**

Bit Number	Bit Mnemonic	Description
7	ART2	Automatic Reset Transition Set this bit to have the CRST2 pin changed according to activation sequence. Clear this bit to have the CRST2 pin immediately following the value programmed in CARDRST2.
6	CRST_SEL2	Card Reset Selection Set this bit to have the CRST2 pin driven by hardware through the A1/RST pin. Clear this bit to have the CRST pin driven by software through the CARDRST bit. The reset value is 0.
5	CARDRST2	Card Reset Set this bit to enter a reset sequence according to ART2 bit value. Clear this bit to drive a low level on the CRST2 pin.
4	CARDCK2	Card Clock Set this bit to set a high level on the CCLK2 pin (according to CKSTOP2 bit value). Clear this bit to drive a low level on the CCLK2 pin.
3	CKSTOP2	CARD Clock Stop Set this bit to stop CCLK2 according to CARDCK2. This can be used to set asynchronous cards in power-down mode (GSM) or to drive CCLK2 by software. Clear this bit to have CCLK2 running according to CKS2. This can be used to activate asynchronous cards. Note: When this bit is changed a special logic ensures that no glitch occurs on the CCLK2 pin and actual configuration changes can be delayed by half a period to two periods of CCLK2.
2-0	CKS2[2:0]	Interface 2 Card Clock Selection CKS2 [2:0] = 0: CCLK2 = CLK (then the maximum frequency is 24 MHz) CKS2 [3:0] = 1: CCLK2 = DCCLK CKS2 [3:0] = 2: CCLK2 = DCCLK / 2 CKS2 [3:0] = 3: CCLK2 = DCCLK / 4 CKS2 [3:0] = 4: CCLK2 = A2 CKS2 [3:0] = 5: CCLK2 = A2 / 2 CKS2 [3:0] = 6: CCLK2 = CLK / 2 CKS2 [3:0] = 7: CCLK2 = CLK / 4

Reset value = 0x00001000

Notes:
1. When CKS2 value is changed a special logic insures no glitch occurs on the CCLK2 pin and actual configuration changes can be delayed by half a period to two periods of CCLK2.
2. CCLK2 must be stopped with CKSTOP2 bit before switching from CKS2 = (0, 1, 2, 3, 6, 7) to CKS2 = (4, 5) or vice versa.

Table 27. SC3_CFG0()

7	6	5	4	3	2	1	0
VCARD_INT3	**VCARD_OK3**	**ATRERR3**	**X**	**X**	**VCARDERR3**	**VCARD31**	**VCARD30**

Bit Number	Bit Mnemonic	Description
7	VCARD_INT3	SC3 voltage interrupt This bit is set when VCARD_OK3 bit is set. This bit is cleared when read by the micro controller.
6	VCARD_OK3	SC3 Voltage Status This bit is set by the LDO3 when the output voltage remains within the voltage range specified by VCARD3[1:0] bits. It is cleared otherwise.
5	ATRERR3	Answer to Reset Interrupt for SC3 This bit is set when the card clock counter overflows (no falling edge on CIO3 is received before the overflow of the card clock counter). This bit is cleared by hardware when this register is read. It can be set by software for test purpose.
4	X	
3	X	
2	VCARDERR3	Interface 3 Card Out of Range Voltage Interrupt This bit is set when the output voltage on $CVCC_N$ goes out of the voltage range specified by VCRDN field. It can be set by software for test purpose and deactivate the card. This bit is cleared by hardware when this register is read. It cannot be cleared by software. The reset value is 0.
1-0	VCARD3[1:0]	Interface 3 Card Voltage Selection VCRD3[1:0] = 00: 0V VCRD3[1:0] = 01: 1.8V class C VCRD3[1:0] = 10: 3V class B VCRD3[1:0] = 11: 5V class A No card deactivation is performed when the voltage is changed. The micro controller should deactivate the card before changing the voltage and activating the card again. The reset value is 00.

Reset value = 0x 000X 0000

Table 28. SC3_CFG2 ()

7	6	5	4	3	2	1	0
ART3	**X**	**CARDRST3**	**CARDCK3**	**CKSTOP3**	**CK32**	**CKS31**	**CKS30**

Bit Number	Bit Mnemonic	Description
7	ART3	Automatic Reset Transition Set this bit to have the CRST3 pin changed according to activation sequence. Clear this bit to have the CRST3 pin immediately following the value programmed in CARDRST3.
6	X	
5	CARDRST3	Card Reset Set this bit to enter a reset sequence according to ART3 bit value. Clear this bit to drive a low level on the CRST3 pin. This bit must be cleared to use AUX2 pin for CRST3 source.
4	CARDCK3	Card Clock Set this bit to set a high level on the CCLK3 pin (according to CKSTOP3 bit value). Clear this bit to drive a low level on the CCLK3 pin.
3	CKSTOP3	CARD Clock Stop Set this bit to stop CCLK3 according to CARDCK3. This can be used to set asynchronous cards in power-down mode (GSM) or to drive CCLK3 by software. Clear this bit to have CCLK3 running according to CKS3. This can be used to activate asynchronous cards. Note: When this bit is changed a special logic ensures that no glitch occurs on the CCLK3 pin and actual configuration changes can be delayed by half a period to two periods of CCLK3.
2-0	CKS3[2:0]	Interface 4Card Clock Selection CKS3 [2:0] = 0: CCLK3 = CLK (then the maximum frequency is 24 MHz) CKS3 [3:0] = 1: CCLK3 = DCCLK CKS3 [3:0] = 2: CCLK3 = DCCLK / 2 CKS3 [3:0] = 3: CCLK3 = DCCLK / 4 CKS3 [3:0] = 4: CCLK3 = A2 CKS3 [3:0] = 5: CCLK3 = A2 / 2 CKS3 [3:0] = 6: CCLK3 = CLK / 2 CKS3 [3:0] = 7: CCLK3 = CLK / 4 The reset value is 0.

Reset value = 0x 0X00 1000

Notes:
1. When CKS3 value is changed a special logic insures no glitch occurs on the CCLK3 pin and actual configuration changes can be delayed by half a period to two periods of CCLK3.
2. CCLK3 must be stopped with CKSTOP3 bit before switching from CKS3 = (0, 1, 2, 3, 6, 7) to CKS3 = (4, 5) or vice versa.

Table 29. SC4_CFG0()

7	6	5	4	3	2	1	0
VCARD_INT4	**VCARD_OK4**	**ATRERR4**	**X**	**X**	**VCARDERR4**	**VCARD41**	**VCARD40**

Bit Number	Bit Mnemonic	Description
7	VCARD_INT4	SC4 voltage interrupt This bit is set when VCARD_OK4 bit is set. This bit is cleared when read by the micro controller.
6	VCARD_OK4	SC4 Voltage Status This bit is set by the LD04 when the output voltage remains within the voltage range specified by VCARD4[1:0] bits. It is cleared otherwise.
5	ATRERR4	Answer to Reset Interrupt for SC4 This bit is set when the card clock counter overflows (no falling edge on CIO4 is received before the overflow of the card clock counter). This bit is cleared by hardware when this register is read. It can be set by software for test purpose.
4	X	
3	X	
2	VCARDERR4	**Interface 4 Card Out of Range Voltage Interrupt** This bit is set when the output voltage on $CVCC_N$ goes out of the voltage range specified by VCRDN field. It can be set by software for test purpose and deactivate the card. This bit is cleared by hardware when this register is read. It cannot be cleared by software. The reset value is 0.
1-0	VCARD4[1:0]	**Interface 4 Card Voltage Selection** VCRD4[1:0] = 00: 0V VCRD4[1:0] = 01: 1.8V class C VCRD4[1:0] = 10: 3V class B VCRD4[1:0] = 11: 5V class A No card deactivation is performed when the voltage is changed. The micro controller should deactivate the card before changing the voltage and activating the card again. The reset value is 00.

Reset value = 0x 000X X000

Table 30. SC4_CFG2 ()

7	6	5	4	3	2	1	0
ART4	**X**	**CARDRST4**	**CARDCK4**	**CKSTOP4**	**CKS42**	**CKS41**	**CKS40**

Bit Number	Bit Mnemonic	Description
7	ART4	Automatic Reset Transition Set this bit to have the CRST4 pin changed according to activation sequence. Clear this bit to have the CRST4 pin immediately following the value programmed in CARDRST4.
6	X	
5	CARDRST4	Card Reset Set this bit to enter a reset sequence according to ART4 bit value. Clear this bit to drive a low level on the CRST4 pin.
4	CARDCK4	Card Clock Set this bit to set a high level on the CCLK4 pin (according to CKSTOP4 bit value). Clear this bit to drive a low level on the CCLK4 pin.
3	CKSTOP4	CARD Clock Stop Set this bit to stop CCLK4 according to CARDCK4. This can be used to set asynchronous cards in power-down mode (GSM) or to drive CCLK4 by software. Clear this bit to have CCLK4 running according to CKS4. This can be used to activate asynchronous cards. Note: When this bit is changed a special logic ensures that no glitch occurs on the CCLK4 pin and actual configuration changes can be delayed by half a period to two periods of CCLK4.
2-0	CKS4[2:0]	Interface 4Card Clock Selection CKS4 [2:0] = 0: CCLK4 = CLK (then the maximum frequency is 24 MHz) CKS4 [3:0] = 1: CCLK4 = DCCLK CKS4 [3:0] = 2: CCLK4 = DCCLK / 2 CKS4 [3:0] = 3: CCLK4 = DCCLK / 4 CKS4 [3:0] = 4: CCLK4 = A2 CKS4 [3:0] = 5: CCLK4 = A2 / 2 CKS4 [3:0] = 6: CCLK4 = CLK / 2 CKS4 [3:0] = 7: CCLK4 = CLK / 4 The reset value is 0.

Reset value = 0x 0X00 1000

Notes:
1. When CKS4 value is changed a special logic insures no glitch occurs on the CCLK4 pin and actual configuration changes can be delayed by half a period to two periods of CCLK4.
2. CCLK4 must be stopped with CKSTOP4 bit before switching from CKS4 = (0, 1, 2, 3, 6, 7) to CKS4 = (4, 5) or vice versa.

Table 31. SC5_CFG0()

7	6	5	4	3	2	1	0
VCARD_INT5	VCARD_OK5	ATRERR5	X	X	VCARDERR5	VCARD51	VCARD50

Bit Number	Bit Mnemonic	Description
7	VCARD_INT5	SC5 voltage interrupt This bit is set when VCARD_OK5 bit is set. This bit is cleared when read by the micro controller.
6	VCARD_OK5	SC5 Voltage Status This bit is set by the LDO5 when the output voltage remains within the voltage range specified by VCARD5[1:0] bits. It is cleared otherwise.
5	ATRERR5	Answer to Reset Interrupt for SC5 This bit is set when the card clock counter overflows (no falling edge on CIO5 is received before the overflow of the card clock counter). This bit is cleared by hardware when this register is read. It can be set by software for test purpose.
4	X	
3	X	
2	VCARDERR5	Interface 5 Card Out of Range Voltage Interrupt This bit is set when the output voltage on $CVCC_N$ goes out of the voltage range specified by VCRDN field. It can be set by software for test purpose and deactivate the card. This bit is cleared by hardware when this register is read. It cannot be cleared by software. The reset value is 0.
1-0	VCARD5[1:0]	Interface 5 Card Voltage Selection VCRD5[1:0] = 00: 0V VCRD5[1:0] = 01: 1.8V class C VCRD5[1:0] = 10: 3V class B VCRD5[1:0] = 11: 5V class A No card deactivation is performed when the voltage is changed. The micro controller should deactivate the card before changing the voltage and activating the card again. The reset value is 00.

Reset value = 0x 000X X000

Table 32. SC5_CFG2 ()

7	6	5	4	3	2	1	0
ART5	**X**	**CARDRST5**	**CARDCK5**	**CKSTOP5**	**CKS52**	**CKS51**	**CKS50**

Bit Number	Bit Mnemonic	Description
7	ART5	Automatic Reset Transition Set this bit to have the CRST5 pin changed according to activation sequence. Clear this bit to have the CRST5 pin immediately following the value programmed in CARDRST5.
6	X	
5	CARDRST5	Card Reset Set this bit to enter a reset sequence according to ART5 bit value. Clear this bit to drive a low level on the CRST5 pin.
4	CARDCK5	Card Clock Set this bit to set a high level on the CCLK5 pin (according to CKSTOP5 bit value). Clear this bit to drive a low level on the CCLK5 pin.
3	CKSTOP5	CARD Clock Stop Set this bit to stop CCLK5 according to CARDCK5. This can be used to set asynchronous cards in power-down mode (GSM) or to drive CCLK5 by software. Clear this bit to have CCLK5 running according to CKS5. This can be used to activate asynchronous cards. Note: When this bit is changed a special logic ensures that no glitch occurs on the CCLK5 pin and actual configuration changes can be delayed by half a period to two periods of CCLK5.
2-0	CKS5[2:0]	Interface 5Card Clock Selection CKS5 [2:0] = 0: CCLK5 = CLK (then the maximum frequency is 24 MHz) CKS5 [3:0] = 1: CCLK5 = DCCLK CKS5 [3:0] = 2: CCLK5 = DCCLK / 2 CKS5 [3:0] = 3: CCLK5 = DCCLK / 4 CKS5 [3:0] = 4: CCLK5= A2 CKS5 [3:0] = 5: CCLK5 = A2 / 2 CKS5 [3:0] = 6: CCLK5 = CLK / 2 CKS5 [3:0] = 7: CCLK5 = CLK / 4 The reset value is 0.

Reset value = 0x 0X00 1000

Notes:
1. When CKS5 value is changed a special logic insures no glitch occurs on the CCLK5 pin and actual configuration changes can be delayed by half a period to two periods of CCLK5.
2. CCLK5 must be stopped with CKSTOP5 bit before switching from CKS5 = (0, 1, 2, 3, 6, 7) to CKS5 = (4, 5) or vice versa.

Table 33. TIMER_MSB (Timer MSB for SC1, SC2, SC3, SC4, SC5)

7	6	5	4	3	2	1	0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Bit Number	Bit Mnemonic	Description
7 - 0	Bits 15 - 8	Timer MSB (bits 15 to 8)

Reset value = 0x 0000 0001

Table 34. TIMER_LSB (Timer LSB for SC1, SC2, SC3, SC4, SC5)

7	6	5	4	3	2	1	0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Number	Bit Mnemonic	Description
7 - 0	bits 7 - 0	Timer LSB (bits 7to 0)

Reset value = 0x 1001 0000

Table 35. CAPTURE_MSB (Capture MSB for SC1, SC2, SC3, SC4, SC5)

7	6	5	4	3	2	1	0
bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8

Bit Number	Bit Mnemonic	Description
7 - 0	bits 15 - 8	See Section “Software activation for SCn (n=1, 2, 3, 4, 5) interfaces and ARTn bit = 1”, page 25

Reset value = 0x 0000 0000

Table 36. CAPTURE_LSB (Capture LSB for SC1, SC2, SC3, SC4, SC5)

7	6	5	4	3	2	1	0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Bit Number	Bit Mnemonic	Description
7 - 0	bits 7 - 0	See Section “Software activation for SCn (n=1, 2, 3, 4, 5) interfaces and ARTn bit = 1”, page 25

Reset value = 0x 0000 0000

Table 37. IO_SELECT (Selection byte for IO)

7	6	5	4	3	2	1	0
X	X	X	X	IOSEL3	IOSEL2	IOSEL1	IOSEL0

Bit Number	Bit Mnemonic	Description
7	X	
6	X	
5	X	
4	X	
3-0	IOSEL[3:0]	IO Selection This field indicates the IO routing between the host and the Smart Card Interfaces when activated, seeTable 38 and IODISn value (n=1, 2, 3, 4, 5). When no host IO is routed to a smart card pin, this pin is driven according to the Interface register. See Section “CIO, CC4, CC8 controller”, page 15.

Reset value = 0x XXXX 1000

Table 38. IO Selection

IOSEL[3:0]	IO1	IO2	AUX1	AUX2
0000	CIO1	- (1)	- (1)	- (1)
0001	CIO2	- (1)	- (1)	- (1)-
0010	CIO3	- (1)	- (1)	- (1)
0011	CIO4	- (1)	- (1)	- (1)
0100	CIO5	- (1)	- (1)	- (1)
0101	CIO1	CIO2	CC41	CIO3/CC42
0110	CIO1	CIO2	CC41	CIO4
0111	CIO1	CIO2	CC41	CIO5
1000	**CIO1**	**CIO2**	**CC41**	**CC81**
1001	CIO1	CIO3	CC41	CC81
1010	CIO1	CIO4	CC41	CC81
1011	CIO1	CIO5	CC41	CC81
1100	CIO1	CIO5	CIO3/CC42	CIO4
1101	CIO2	CIO5	CIO3/CC42	CIO4
1110	CIO2	CIO4	CIO3/CC42	CRST3/CC82
1111	CIO2	CIO5	CIO3/CC42	CRST3/CC82

Reset value for IOSEL[3:0]= 0x1000

Note: 1. If no input (IO1, IO2, AUX1, AUX2) is selected for a SCIB pin (CIOn, CC4n CC8n), and if the smart card interface is started, the electrical level on the SCIB pin corresponds to the CARDIOn, CARDC4n or CARDC8n bit value.

2. For IOSEL[3:0] = 0xOE and IOSEL[3:0] = 0x0F, the CARDRST3 bit must be set to connect AUX2 to CRST3/CC82 pin.

Table 39. INTERFACEB ()

7	6	5	4	3	2	1	0
X	CARDC82	CARDIO5	CARDIO4	CARDIO3/CARDC42	CARDIO2	DEMBOOSTB1	DEMBOOSTB0

Bit Number	Bit Mnemonic	Description
7	X	
6	CARDC82	Set this bit to drive the CRST3/CC82 pin High with the on-chip pull-up (according to IODIS2 bit value). The pin can then be an input (read in STATUSB register). Clear this bit to drive a low level on the CC82 pin (according to IODIS2 bit value).
5	CARDIO5	Set this bit to drive the CIO5 pin High with the on-chip pull-up when isolated from the host (See “ITDIS ()” on page 59.). The pin can then be an input (read in STATUSB register). Clear this bit to drive a low level on the CIO5 pin when isolated from the host.
4	CARDIO4	Set this bit to drive the CIO4 pin High with the on-chip pull-up when isolated from the host (See “ITDIS ()” on page 59.). The pin can then be an input (read in STATUSB register). Clear this bit to drive a low level on the CIO4/C45 pin when isolated from the host.
3	CARDIO3/ CARDC42	Set this bit to drive the CIO3/CC42 pin High with the on-chip pull-up when isolated from the host (See “ITDIS ()” on page 59.). The pin can then be an input (read in STATUSB register). Clear this bit to drive a low level on the CIO3/CC42 pin when isolated from the host. This bit is CIO3 when AUX=0 or when AUX=1 and IFN=2, otherwise it is CC42.
2	CARDIO2	Set this bit to drive the CIO2 pin High with the on-chip pull-up when isolated from the host (See “ITDIS ()” on page 59.). The pin can then be an input (read in STATUSB register). Clear this bit to drive a low level on the CIO2 pin when isolated from the host.
1-0	DEMBOOSTB[1-0]	Configuration for DC/DCB startup current. 00: Normal: 80 mA average 01: Normal + 18% 10: Normal + 18% (and boost on oscillator) 11: Normal + 40%

Reset value = 0x X000 0000

Table 40. STATUSB () - Read Only

7	6	5	4	3	2	1	0
X	**CARDIN2**	**CIO5**	**CIO4**	**CRST3/ CC82**	**CIO3/ CC42**	**CRST2**	**CIO2**

Bit Number	Bit Mnemonic	Description
7	X	
6	CARDIN2	Card Presence Status 2 This bit is set when a card is detected. It is cleared otherwise.
5	CIO5	Card CIO5 This bit provides the actual level on the CIO5 pin when read.
4	CIO4	Card CIO4 This bit provides the actual level on the CIO4 pin when read.
3	CRST3/CC82	Card CRST3 This bit provides the actual level on the CRST3 pin when read.
2	CIO3/CC42	Card CIO3 This bit provides the actual level on the CIO3 pin when read.
1	CRST2	Card CRST2 This bit provides the actual level on the CRST2 pin when read.
0	CIO2	Card CIO2 This bit provides the actual level on the CIO2 pin when read.

Reset value = reset value depends on hardware configuration

Table 41. ITDIS ()

7	6	5	4	3	2	1	0
IODIS5	**IODIS4**	**IODIS3**	**IODIS2**	**ITDIS5**	**ITDIS4**	**ITDIS3**	**ITDIS2**

Bit Number	Bit Mnemonic	Description
7	IODIS5	Card I/O isolation Set this bit to drive CIO5 pin according to CARDIO5. Clear this bit to drive the CIO5 pin connected to inputs according to IO_SELECT registers. If IOSEL config doesn't link an input to CIO5, CIO5 outputs CARDIO5 value.
6	IODIS4	Card I/O isolation Set this bit to drive CIO4 pin according to CARDIO4. Clear this bit to drive the CIO4 pin connected to inputs according to IO_SELECT registers. If IOSEL config doesn't link an input to CIO4, CIO4 outputs CARDIO4 value.
5	IODIS3	Card I/O isolation Set this bit to drive CIO3 pin according to CARDIO3. Clear this bit to drive the CIO3 pin connected to inputs according to IO_SELECT registers. If IOSEL config doesn't link an input to CIO3, CIO3 outputs CARDIO3 value.
4	IODIS2	Card I/O isolation Set this bit to drive the CIO2, CC42, CC82 pins according to CARDIO2, CARDC42, CARDC82 respectively. Clear this bit to drive the CIO2, CC42 and CC82 pins connected to inputs according to IO_SELECT register. If IOSEL config doesn't link an input to CIO2, CIO2 outputs CARDIO2 value.
3	ITDIS5	Interrupt Disable of Smart Card Interface 5 Set this bit to disable interrupts from the interface 5 (the flags are set but $\overline{INT}$ pin is not driven). Clear this bit to allow interrupts.
2	ITDIS4	Interrupt Disable of Smart Card Interface 4 Set this bit to disable interrupts from the interface 4(the flags are set but $\overline{INT}$ pin is not driven). Clear this bit to allow interrupts.
1	ITDIS3	Interrupt Disable of Smart Card Interface 3 Set this bit to disable interrupts from the interface 3 (the flags are set but $\overline{INT}$ pin is not driven). Clear this bit to allow interrupts.
0	ITDIS2	Interrupt Disable of Smart Card Interface 2 Set this bit to disable interrupts from the interface 2(the flags are set but $\overline{INT}$ pin is not driven). Clear this bit to allow interrupts.

Reset value = 0x 1111 0010

Table 42. DCDCB (Config Interface B Byte 2)

7	6	5	4	3	2	1	0
SHUTDOWNB	VDCB_INT	VDCB_OK	0	ICCADJB	STEPREGB	VDCB1	VDCB0

Bit Number	Bit Mnemonic	Description
7	SHUTDOWNB	Shutdown DCDCB Set this bit to reduce the power consumption. An automatic de-activation sequence will be done. Clear this bit to enable VDCB. The reset value is 0.
6	VDCB_INT	DC/DC B voltage interrupt This bit is set when VCARD_OKB bit is set. This bit is cleared when read by the micro controller. The reset value is 0.
5	VDCB_OK	DC/DC B Voltage Status This bit is set by the DCDC when the output voltage remains within the voltage range specified by VDCB[1:0] bits. It is recommended to wait for this bit to be set before activating a card at the corresponding voltage. It is cleared otherwise. The reset value is 0.
4	0	This bit must be always at 0.
3	ICCADJB	CI_{CC} overflow adjust This bit controls the DC/DCB sensitivity to any overflow current. Set this bit to decrease the DC/DCB sensitivity (CI_{CC_ovf} is increased by about 20%). Clear this bit to have a normal configuration. The reset value is 0.
2	STEPREGB	DC/DC B Step-up Regulator Mode Set this bit to permanently disable the step-up converter (CVCC is stable only if VCC is sufficiently higher than CVCC). This bit must always be set if no external self is used. Clear this bit to enable the automatic step-up converter (CVCC is stable even if VCC is not higher than CVCC). The reset value is 0.
1-0	VDCB[1:0]	DC/DC B Voltage Selection VDCB[1:0] = 00: 0V VDCB[1:0] = 01: 2.2V (for Class C) VDCB[1:0] = 10: 3.2V (for Class B and C) VDCB[1:0] = 11: 5.2V (for Class A, B and C) No card deactivation is performed when the voltage is changed. The voltage must be set higher than the voltage of all the active cards. If a Class A card is deactivated and the remaining cards are in Class B or C, VDCB can be reduced to 3.2V to reduce power consumption. If a Class B card is deactivated and the remaining cards are in Class C, VDCB can be reduced to 2.2V to reduce power consumption.It is not reset when cards are deactivated. It must be cleared by the micro controller to stop DC/DC B (e.g. to reduce power consumption). The reset value is 00.

Reset value = 0x 0000 0000

Table 43. LDO

7	6	5	4	3	2	1	0
IPLUS5	**IPLUS4**	**IPLUS3**	**IPLUS2**	**1**	**1**	**1**	**1**

Bit Number	Bit Mnemonic	Description
7	IPLUS5	If set, this bit increases the startup and overflow current of LDO5 (+60%)
6	IPLUS4	If set, this bit increases the startup and overflow current of LDO4 (+60%)
5	IPLUS3	If set, this bit increases the startup and overflow current of LDO3 (+60%)
4	IPLUS2	If set, this bit increases the startup and overflow current of LDO2 (+60%)
3	1	Do not clear this bit.
2	1	Do not clear this bit.
1	1	Do not clear this bit.
0	1	Do not clear this bit.

Reset value = 0x 0000 1111

Table 44. SLEW_CTRL_1(Slew control for SC1 and SC2)

7	6	5	4	3	2	1	0
CCLK2_SLEW_CTRL1	CCLK2_SLEW_CTRL0	CIO2_SLEW_CTRL1	CIO2_SLEW_CTRL0	CCLK1_SLEW_CTRL1	CCLK1_SLEW_CTRL0	CIO1_SLEW_CTRL1	CIO1_SLEW_CTRL0

Bit Number	Bit Mnemonic	Description
7-6	CCLK2_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC2=5V) 0 1: Mode 2 (optimum for CVCC2=3V) 1 0: Mode 3 (optimum for CVCC2=1.8V) 1 1: Automatic mode The reset value is 11.
5-4	CIO2_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC2=5V) 0 1: Mode 2 (optimum for CVCC2=3V) 1 0: Mode 3 (optimum for CVCC2=1.8V) 1 1: Automatic mode The reset value is 11.
3-2	CCLK1_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC1=5V) 0 1: Mode 2 (optimum for CVCC1=3V) 1 0: Mode 3 (optimum for CVCC1=1.8V) 1 1: Automatic mode The reset value is 11.
1-0	CIO1_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC1=5V) 0 1: Mode 2 (optimum for CVCC1=3V) 1 0: Mode 3 (optimum for CVCC1=1.8V) 1 1: Automatic mode The reset value is 11.

Reset value = 0x 1111 1111

Table 45. SLEW_CTRL_2 (Slew control for SC3 and SC4)

7	6	5	4	3	2	1	0
CCLK4_SLEW_CTRL1	CCLK4_SLEW_CTRL0	CIO4_SLEW_CTRL1	CIO4_SLEW_CTRL0	CCLK3_SLEW_CTRL1	CCLK3_SLEW_CTRL0	CIO3_SLEW_CTRL1	CIO3_SLEW_CTRL0

Bit Number	Bit Mnemonic	Description
7-6	CCLK4_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC4=5V) 0 1: Mode 2 (optimum for CVCC4=3V) 1 0: Mode 3 (optimum for CVCC4=1.8V) 1 1: Automatic mode The reset value is 11.
5-4	CIO4_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC4=5V) 0 1: Mode 2 (optimum for CVCC4=3V) 1 0: Mode 3 (optimum for CVCC4=1.8V) 1 1: Automatic mode The reset value is 11.
3-2	CCLK3_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC3=5V) 0 1: Mode 2 (optimum for CVCC3=3V) 1 0: Mode 3 (optimum for CVCC3=1.8V) 1 1: Automatic mode The reset value is 11.
1-0	CIO3_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC3=5V) 0 1: Mode 2 (optimum for CVCC3=3V) 1 0: Mode 3 (optimum for CVCC3=1.8V) 1 1: Automatic mode The reset value is 11.

Reset value = 0x 1111 1111

Table 46. SLEW_CTRL_3 (Slew control for SC5)

7	6	5	4	3	2	1	0
X	X	X	X	CCLK5_SLEW_CTRL1	CCLK5_SLEW_CTRL0	CIO5_SLEW_CTRL1	CIO5_SLEW_CTRL0

Bit Number	Bit Mnemonic	Description
7-4	X	
3-2	CCLK5_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC5=5V) 0 1: Mode 2 (optimum for CVCC5=3V) 1 0: Mode 3 (optimum for CVCC5=1.8V) 1 1: Automatic mode The reset value is 11.
1-0	CIO5_SLEW_CTRL[1-0]	0 0: Mode 1 (optimum for CVCC5=5V) 0 1: Mode 2 (optimum for CVCC5=3V) 1 0: Mode 3 (optimum for CVCC5=1.8V) 1 1: Automatic mode The reset value is 11.

Reset value = 0x XXXX 1111

Electrical Characteristics

Absolute Maximum Ratings *

Ambient Temperature Under Bias:	- 40°C to 85°C
Storage Temperature:	-65°C to +150°C
Voltage on VCC:	V_{SS} -0.5V to +6.0V
Voltage on SCIB pins (***):	CVSS -0.5V to CVCC + 0.5V
Voltage on host interface pins:	VSS -0.5V to EVCC + 0.5V
Voltage on other pins:	VSS -0.5V to VCC + 0.5V
Max Power Dissipation:	350mW
Thermal resistor of QFN package (**)	24°C/W
Thermal resistor of VQFP package	67°C/W

*NOTICE: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
Power Dissipation value is based on the maximum allowable die temperature and the thermal resistance of the package.

(**) Exposed die attached pad must be soldered to ground

Thermal resistor is measured on multi-layer PCB with 0 m/s air flow.

(***) including shortages between any groups of smart card pins.

AC/DC Parameters

EVCC connected to host power supply: from 2.5V to 5.5V.

T_A = -40°C to +85°C; V_{SS} = 0V; V_{CC} = 3V to 5.5V.

CLASS A (5V) for smart card 1, 2, 3, 4, 5 supplied with CVCC (+/- 8%)

CLASS B (3V)for smart card 1, 2, 3, 4, 5 supplied with CVCC (+/- 8%)

CLASS C (1.8V) for smart card 1, 2, 3, 4, 5 supplied with CVCC (+/- 8%)

Table 47. Core (VCC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{PFDP}	Power fail high level threshold	2.46	2.59	2.75	V	
V_{PFDM}	Power fail low level threshold	2.26	2.40	2.56	V	
Hysteresis	Delta between (VPFDP - VPFDM)	100	190	300	mV	
t_{rise}	VCC rise time	1us		10s	µs	
t_{fall}	VCC fall time	100us		10s		
$I_{cc\ operating}$	Operating current		0.25 * CLK +12		mA	DCDCA, DCDCB and LDOs on with load= 0 mA VCC = 5.5V
$I_{cc\ power\ down}$	Power down current		30	75	µA	SHUTDOWNA bit = 1 SHUTDOWNB bit = 1 VCC = 5.5V
CLK	On Chip Oscillator	4		48	MHz	

Table 48. Host Interface (IO1, IO2, AUX1, AUX2, CLK, A2/CK, A1/RST, $\overline{INT}$)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low-voltage			0.8	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output low voltage			0.3	V	I_{OL} = -500µA
V_{OH}	Output High Voltage	VCC - 0.7V			V	I_{OH} = +30µA

Table 49. Host Interface (SCL, SDA, $\overline{RESET}$)

Sym?bol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low-voltage			0.8	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output low voltage			0.3	V	I_{OL} = -3mA

Table 50. Smart Card 1 Class A, 5V (CVCC1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	4.6	5	5.4	V	Load = 60mA VCC = 3V to 5.5V if STEPREG = 0 VCC > 5.3V if STEPREG = 1
$CI_{CC_}ovf$	Card Supply Current Overflow: ICCADJA = 0 (reset value)			90	mA	
	Ripple on CVCC	32	96	240	mV	With low ESR capacitance (0.1 Ohms max)
	Spikes on CVCC		0.5		V	
Vcardok up	Vcardok high level threshold		5		V	
Vcardok down	Vcardok low level threshold	4.64			V	
T_{VHL}	CVCC valid to 0.4V		100	500	µs	C_L =10µF
T_{VLH}	CVCC 0 to valid		1000	4000	µs	C_L = 10µF

Table 51. Smart Card 1 Class B, 3V (CVCC1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	2.76	3	3.24	V	Load = 60mA VCC = 3V to 5.5V if STEPREG = 0 VCC > 3.3V if STEPREG = 1

Table 51. Smart Card 1 Class B, 3V (CVCC1) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJA = 0 (reset value)			85	mA	
	Ripple on CVCC	32	56	176	mV	With low ESR capacitance (0.1 Ohms max)
	Spikes on CVCC		0.4		V	
Vcardok up	Vcardok high level threshold		3		V	
Vcardok down	Vcardok low level threshold	2.816			V	
T_{VHL}	CVCC valid to 0.4V		100	400	µs	C_L =10µF
T_{VLH}	CVCC 0 to valid		300	2000	µs	C_L = 10µF

Table 52. Smart Card 1 Class C, 1.8V (CVCC1)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	1.656	1.8	1.944	V	Load = 35mA
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJA = 0 (reset value)			65	mA	
	Ripple on CVCC	30	38	56	mV	
	Spikes on CVCC		0.05		V	
Vcardok up	Vcardok high level threshold		1.8		V	
Vcardok down	Vcardok low level threshold	1.718			V	
T_{VHL}	CVCC valid to 0.4V	30	80	400	µs	C_L =10µF
T_{VLH}	CVCC 0 to valid		220	2000	µs	C_L = 10µF

Table 53. Smart Card 2 Class A, 5V (CVCC2)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	4.6	5	5.4	V	Load = 60mA
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJB = 0 (reset value)			75	mA	
	Ripple on CVCC	20	90	143	mV	
	Spikes on CVCC				V	
Vcardok up	Vcardok high level threshold		5		V	
Vcardok down	Vcardok low level threshold	4.646			V	
T_{VHL}	CVCC valid to 0.4V		150	500	µs	C_L =2.2µF

Table 53. Smart Card 2 Class A, 5V (CVCC2) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{VLH}	CVCC 0 to valid		200	2000	µs	C_L = 2.2µF

Table 54. Smart Card 2 Class B, 3V (CVCC2)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	2.76	3	3.24	V	Load = 60mA
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJB = 0 (reset value)			60	mA	
	Ripple on CVCC	29	88	164	mV	
	Spikes on CVCC				V	
Vcardok up	Vcardok high level threshold		3		V	
Vcardok down	Vcardok low level threshold	2.825			V	
T_{VHL}	CVCC valid to 0.4V		100	500	µs	C_L =2.2µF
T_{VLH}	CVCC 0 to valid		100	1000	µs	C_L = 2.2µF

Table 55. Smart Card 2 Class C, 1.8V (CVCC2)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	1.656	1.8	1.944	V	Load = 35mA
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJB = 0 (reset value)			75	mA	
	Ripple on CVCC	29	86	158	mV	
	Spikes on CVCC				V	
Vcardok up	Vcardok high level threshold		1.8		V	
Vcardok down	Vcardok low level threshold	1.651			V	
T_{VHL}	CVCC valid to 0.4V		70	500	µs	C_L =2.2µF
T_{VLH}	CVCC 0 to valid		80	1000	µs	C_L = 2.2µF

Table 56. Smart Card 3, 4, 5 Class A, 5V (CVCC3, CVCC4, CVCC5)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	4.6	5	5.4	V	Load = 30mA
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJB = 0 (reset value)			70	mA	

Table 56. Smart Card 3, 4, 5 Class A, 5V (CVCC3, CVCC4, CVCC5) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
	Ripple on CVCC	32	78	134	mV	
	Spikes on CVCC				V	
Vcardok up	Vcardok high level threshold		5		V	
Vcardok down	Vcardok low level threshold	4.514			V	
T_{VHL}	CVCC valid to 0.4V		50	500	µs	C_L =470nF
T_{VLH}	CVCC 0 to valid		200	2000	µs	C_L = 470nF

Table 57. Smart Card 3, 4, 5 Class B, 3V (CVCC3, CVCC4, CVCC5)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	2.76	3	3.24	V	Load = 30mA
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJB = 0 (reset value)			70	mA	
	Ripple on CVCC	32	82	175	mV	
	Spikes on CVCC				V	
Vcardok up	Vcardok high level threshold		3		V	
Vcardok down	Vcardok low level threshold	2.791			V	
T_{VHL}	CVCC valid to 0.4V		40	500	µs	C_L =470nF
T_{VLH}	CVCC 0 to valid		100	2000	µs	C_L = 470nF

Table 58. Smart Card 3, 4, 5 Class C, 1.8V (CVCC3, CVCC4, CVCC5)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCC	Smart card voltage	1.656	1.8	1.944	V	Load = 15mA
CI_{CC}_ovf	Card Supply Current Overflow: ICCADJB = 0 (reset value)			75	mA	
	Ripple on CVCC	32	84	178	mV	
	Spikes on CVCC				V	
Vcardok up	Vcardok high level threshold		1.8		V	
Vcardok down	Vcardok low level threshold	1.65			V	
T_{VHL}	CVCC valid to 0.4V		30	500	µs	C_L =470nF
T_{VLH}	CVCC 0 to valid		100	2000	µs	C_L = 470nF

Table 59. Smart Card 1, 2, 3, 4, 5 Clock (CCLK1, CCLK2, CCLK3, CCLK4, CCLK5)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OL}	Output low voltage			0.3	V	Class A: I_{OL} = -200µA Class B: I_{OL} = -200µA Class C: I_{OL} = -200µA
V_{OH}	Output High Voltage	0.8 CVCC			V	Class A: I_{OH} = 200µA Class B: I_{OH} = 200µA Class C: I_{OH} = 200µA
t_R	Rise time (see Tables 66 to 68)			16	ns	C_L = 30pF Class A C_L = 30pF Class B C_L = 30pF Class C
t_F	Fall time (see Tables 66 to 68)			16	ns	C_L = 30pF Class A C_L = 30pF Class B C_L = 30pF Class C
	Low level voltage stability (taking into account PCB design)	-0.25 -0.25 -0.25		0.6 0.4 0.4	V	Class A Class B Class C
	High level voltage stability (taking into account PCB design)	CVCC-0.5		CVCC+0.25	V	CVCC= Class A, Class B or Class C
CCLK	Smart card clock frequency			24	MHz	

Table 60. Smart Card n I/Os (CIOn, CC4n, CC8n, CRSTn) (n =1, 2, 3, 4, 5)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low-voltage	-0.5		0.15 CVCC	V	
V_{IH}	Input High Voltage	0.7 CVCC		CVCC + 0.5	V	
V_{OL}	Output Low-voltage			0.3	V	I_{OL} = -1mA
V_{OH}	Output High Voltage	0.8 CVCC			V	Class A: I_{OH} = 20µA Class B: I_{OH} = 20µA Class C: I_{OH} = 20µA
I_{IL}	Input Low Current			600	µA	
I_{IH}	Input High Current	-40		+40	µA	
I_{OS}	Output Short Circuit Current	-15		+15	mA	Short to GND or CVCC
	Low level voltage stability (taking into account PCB design)	-0.25 -0.25 -0.25		0.6 0.4 0.4	V	Class A Class B Class C
	High level voltage stability (taking into account PCB design)	CVCC-0.5		CVCC+0.25	V	CVCC= Class A, Class B or Class C
t_R	Rise time (see Tables 63 to 65)			100	ns	C_L = 30pF Class A C_L = 30pF Class B C_L = 30pF Class C

Table 60. Smart Card n I/Os (CIOn, CC4n, CC8n, CRSTn) (n =1, 2, 3, 4, 5) (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_F	Fall time			100	ns	C_L = 30pF Class A C_L = 30pF Class B C_L = 30pF Class C

Table 61. Card Presence (CPRES1, CPRES2)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL1}	CPRES1 weak pull-up output current	3	10	25	µA	Short to VSS PULLUP1 = 1: Internal pull-up active
R_{CPRES2}	CPRES2 weak pull-up output current	3	10	25	µA	Short to VSS PULLUP2 = 1: Internal pull-up active

Table 62. DCDCB

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CVCCB	DCDCB output voltage	4.9 3 2	5.3 3.35 2.4		V	Load = 75mA Load = 40mA Load = 10mA
	Ripple on CVCCB			200	mV	
Vcardok up	Vdcbok high level threshold		5.3 3.35 2.4		V	Class A Class B Class C
Vcardok down	Vdcbok low level threshold		4.9 3.1 2.1		V	Class A Class B Class C
T_{VHL}	VDCB valid to 0		100	500	µs	
T_{VLH}	VDCB 0 to valid		1000	4000	µs	

Table 63. Slew rate on CIOn with CVCCn= 5V (n=1, 2, 3, 4, 5), Mode 1

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{R/F}$	Rise time/ Fall time with CIOn_SLEW_CTRL[1-0] = 00 (5V) or CIOn_SLEW_CTRL[1-0] = 11(mode auto)		40		ns	
t_R	Rise time with CIOn_SLEW_CTRL[1-0] = 01 (3V)		20		ns	
t_R	Rise time with CIOn_SLEW_CTRL[1-0] = 10 (1.8V)		8		ns	

Table 64. Slew rate on CIOn with CVCCn= 3V (n=1, 2, 3, 4, 5), Mode 2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{R/F}$	Rise time/ Fall time with CIOn_SLEW_CTRL[1-0] = 01 (3V) or CIOn_SLEW_CTRL[1-0] = 11(mode auto)		30		ns	
t_R	Rise time with CIOn_SLEW_CTRL[1-0] = 10 (1.8V)		12		ns	

Table 65. Slew rate on CIOn with CVCCn= 1.8V (n=1, 2, 3, 4, 5), Mode 3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{R/F}$	Rise time/ Fall time with CIOn_SLEW_CTRL[1-0] = 10 (1.8V) or CIOn_SLEW_CTRL[1-0] = 11(mode auto)		25		ns	

Table 66. Slew rate on CCLKn with CVCCn= 5V (n=1, 2, 3, 4, 5), Mode 1

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{R/F}$	Rise time/ Fall time with CCLKn_SLEW_CTRL[1-0] = 00 (5V) or CCLKn_SLEW_CTRL[1-0] = 11(mode auto)		12		ns	
$t_{R/F}$	Rise time/ Fall time with CCLKn_SLEW_CTRL[1-0] = 01 (3V)		7		ns	
$t_{R/F}$	Rise time/ Fall time with CCLKn_SLEW_CTRL[1-0] = 10 (1.8V)		2.7		ns	

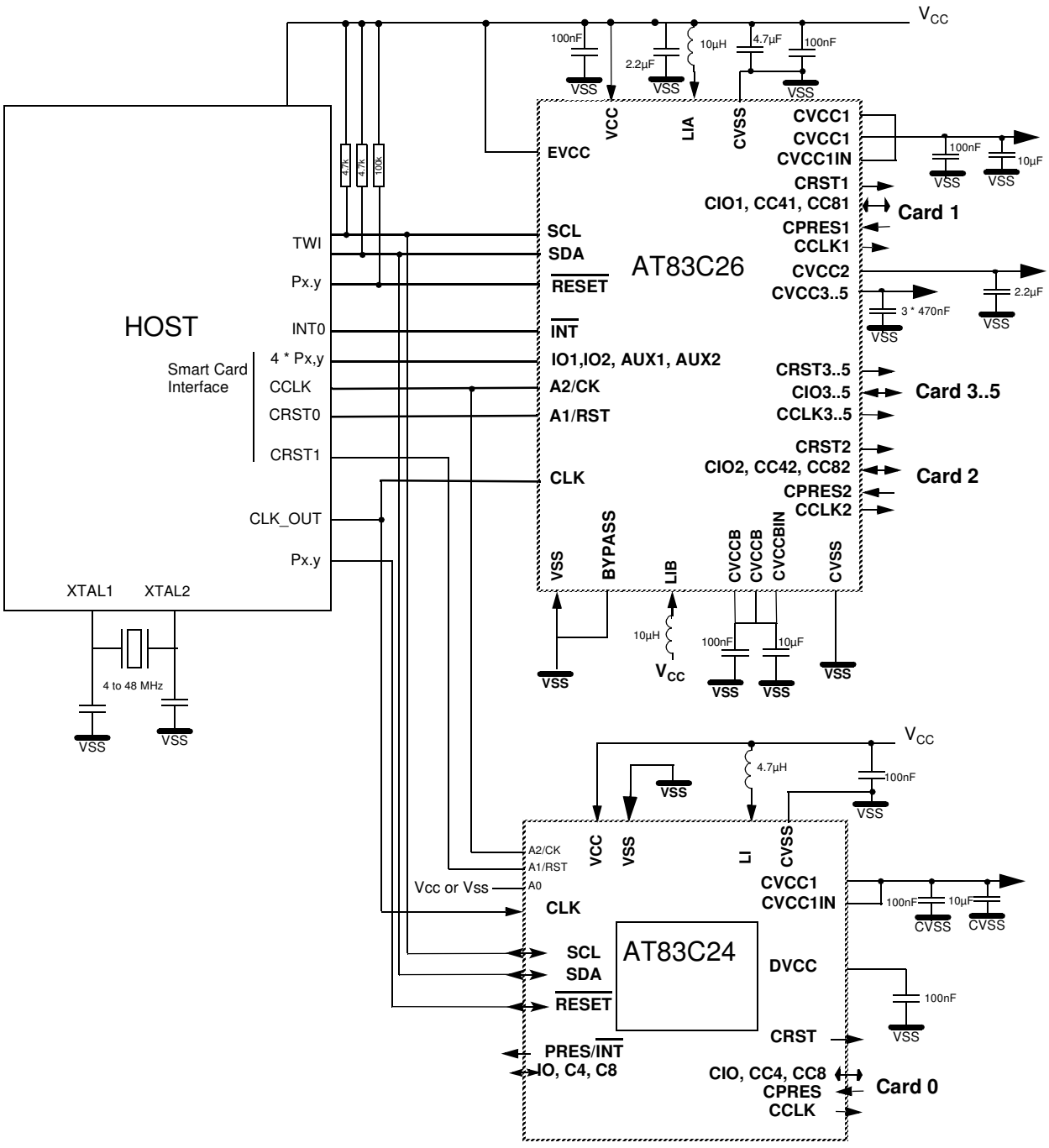
Table 67. Slew rate on CCLKn with CVCCn= 3V (n=1, 2, 3, 4, 5), Mode 2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$t_{R/F}$	Rise time/ Fall time with CCLKn_SLEW_CTRL[1-0] = 01 (3V) or CCLKn_SLEW_CTRL[1-0] = 11(mode auto)		9		ns	
$t_{R/F}$	Rise time/ Fall time with CCLKn_SLEW_CTRL[1-0] = 10 (1.8V)		4		ns	

Table 68. Slew rate on CCLKn with CVCCn= 1.8V (n=1, 2, 3, 4, 5), Mode 3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_R	Rise time/ Fall time with CCLKn_SLEW_CTRL[1-0] = 10 (1.8V) or CCLKn_SLEW_CTRL[1-0] = 11(mode auto)		8.5		ns	

Typical Application



Ordering Information

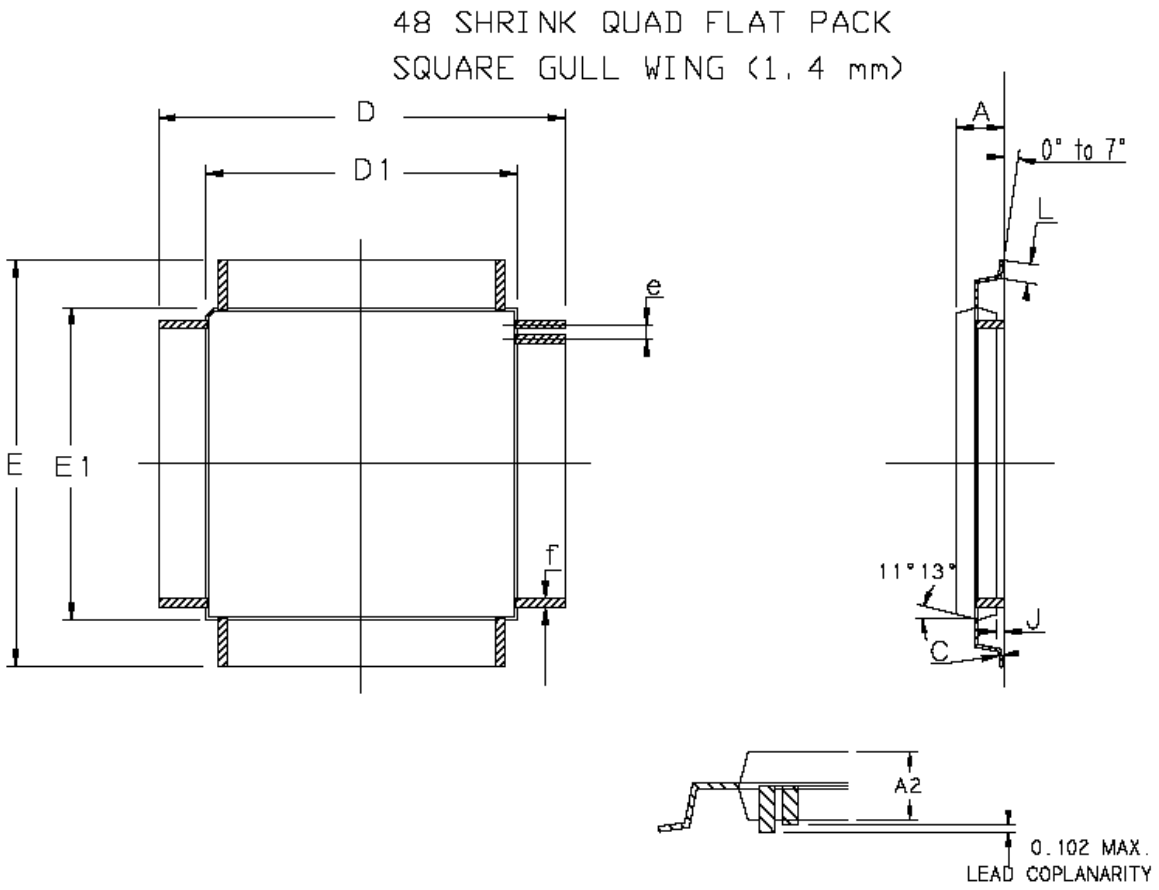
Part Number	Supply Voltage	Temperature Range	Package	Packing
AT83C26-PLTUL	3V to 5.5V	Industrial green	MLF48	Tray
AT83C26-PLRUL	3V to 5.5V	Industrial green	MLF48	Tape&Reel
AT83C26-RKTUL	3V to 5.5V	Industrial green	VQFP48	Tray
AT83C26-RKRUL	3V to 5.5V	Industrial green	VQFP48	Tape&Reel

Samples

Part Number	Supply Voltage	Temperature Range	Package	Packing
AT83C26-PLTEL	3V to 5.5V	25°C	MLF48	Tray
AT83C26-RKTEL	3V to 5.5V	25°C	VQFP48	Tray

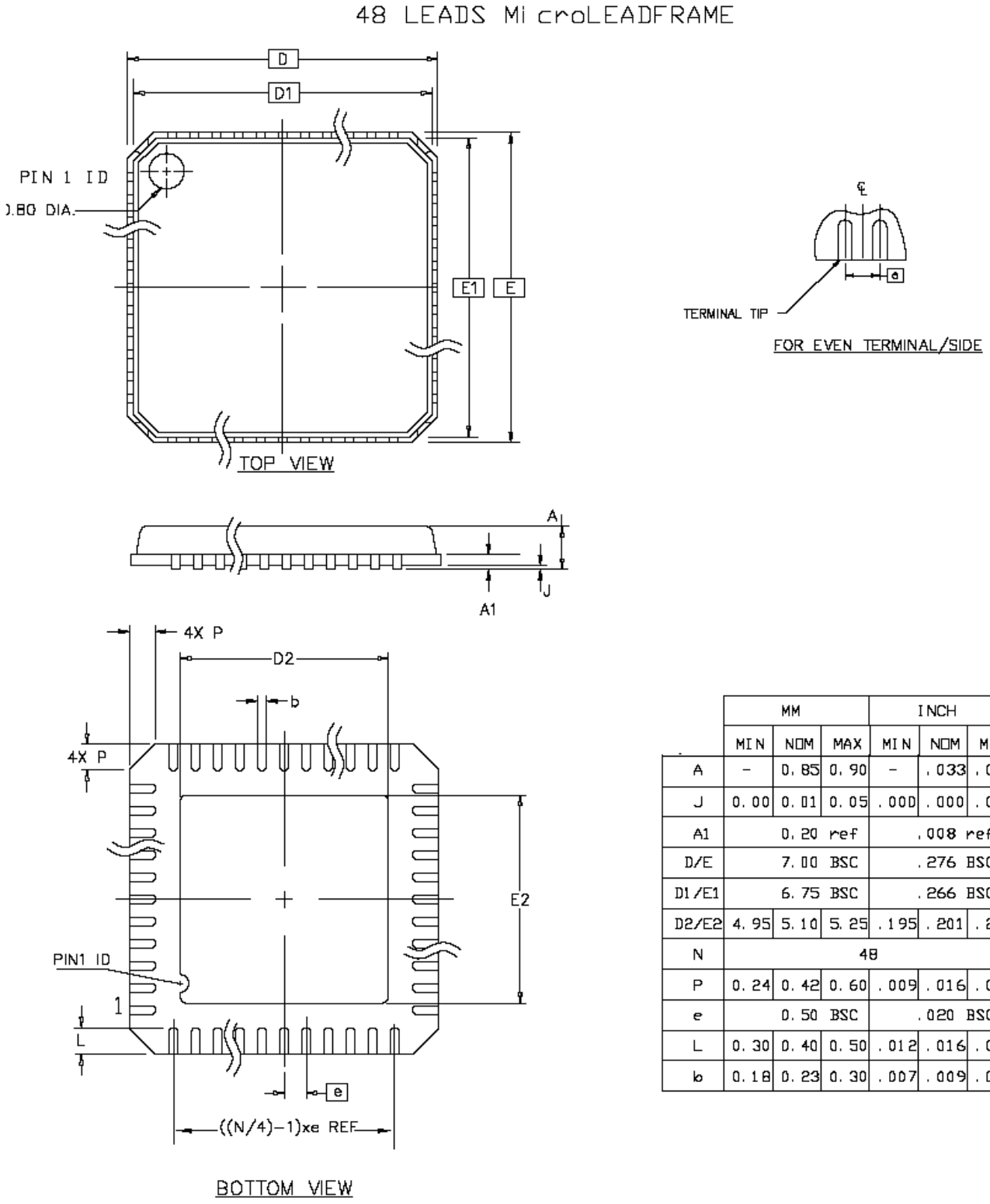
Package Drawings

VQFP48



	MM		INCH	
	Min	Max	Min	Max
A	–	1.60	–	.063
C	0.09	0.16	.004	.006
A2	1.35	1.45	.053	.057
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.17	0.27	.007	.011

QFN48



	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	0.85	0.90	–	.033	.035
J	0.00	0.01	0.05	.000	.000	.002
A1		0.20 ref			.008 ref	
D/E		7.00 BSC			.276 BSC	
D1/E1		6.75 BSC			.266 BSC	
D2/E2	4.95	5.10	5.25	.195	.201	.207
N	48					
P	0.24	0.42	0.60	.009	.016	.024
e		0.50 BSC			.020 BSC	
L	0.30	0.40	0.50	.012	.016	.020
b	0.18	0.23	0.30	.007	.009	.012

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