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We turn engineering into art

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R8051XC

Configurable Microcontroller

Overview

The R8051XC is a fast, configurable, single-chip 8-bit microcontroller core that can implement a variety of fast processor variations executing the MCS® 51 instruction set.

The efficient core design runs an average of 8.1 times faster than the 80C51. A rich set of optional features and peripherals enable designers to closely match the core with their specific application and hardware requirements (FPGA, ASIC, or structured ASIC). These options include memory pointers, interrupts, interfaces for serial communication, I2C and SPI interfaces, a timer system, I/O ports, power management unit, multiplication-division unit, watchdog timer, DMA controller and real-time clock. Integrated on-chip debugging using either the native OCDS or FS2's OCI is also available.

The R8051XC is an extension of our proven 8051 family of processor cores, which have been successfully implemented in a hundred different customer products. Designers can purchase a custom configuration by selecting a set of options that best meets their needs, or choose from these three prepackaged versions of the core:

- R8051XC-F is the fully-configurable version of the core, with all options included.
- R8051XC-A matches our earlier R8051, with a set of peripherals making it compatible with the Intel 80C31 (see details in the Configurations section).
- R8051XC-B matches our earlier R80515 core, with a set of peripherals making it compatible with the Siemens 80C515 and 80C517.

Representative ASIC implementation results for the different configurations range from under 9,000 gates for the R8051XC-A to under 55,000 for all available options (except debug). Speed ranges from 250 to 350 MHz and above, depending on the technology.

Developed for easy reuse in ASIC and FPGA implementations, the core is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset.

Features

- Eight-bit instruction decoder for MCS® 51 instruction set
- Executes instructions with one clock per cycle (versus twelve for standard 80C51) for an average 8.1 times speed increase
- ALU performs 8-bit arithmetic and logical operations and Boolean manipulations; 8-bit multiplication and division can be optionally removed to save silicon
- Flexible external memory interface can address up to 8MB of Program Memory and 8MB of Data Memory Space (when the extended memory option is included)
- Can address up to 256 B of Internal Data Memory
- SFR interface services 40 to 118 external Special Function Registers (depending on configuration)
- Extensive core configurability: choose options as needed, or get fully-configurable version

Optional Features and Peripherals

- External Memory Interface
  - Addresses up to 8 MB of Program Memory (when using memory banking)
  - Addresses up to 8 MB of Data Memory (when using memory banking)
  - One, two, or eight Data Pointers for fast data block transfer
  - Additional Arithmetic Unit supporting Data Pointers auto-increment/-decrement and auto-switch
  - Supports external DMA controller through HOLD interface
  - Program memory write mode
- Multiplication-Division Unit
  - 16 x 16-bit multiplication
  - 32/16- and 16/16-bit division
  - 32-bit normalization and L/R shifting
- Special Function Registers interface
  - Services from 40 to 118 External Special Function Registers (depending on peripheral configuration)
- Interrupt Controller: four priority levels with eighteen interrupt sources, or two priority levels with six sources
- Power Management Unit with power-down modes (IDLE and STOP)
- Interface for on-chip debug: native On-Chip Debug Support (OCDS
- Direct Memory Access (DMA) Controller
  - Up to eight independent channels
  - Read/Write Access to all memory spaces (incl. SFR)
  - Linear addressing (up to 8MB)
  - Address auto-increment/decrement
  - Synchronous/asynchronous Mode
  - Software Trigger/Hardware Trigger
- 16-bit Timers/Counters:
  - 80C51-like Timers 0 and 1
  - 80C515-like Timer 2; it includes a Compare/Capture Unit with four 16-bit Compare registers for Pulse Width Modulation; four external Capture inputs for Pulse Width Measuring; and a 16-bit Reload register for Pulse Generation
- Input/Output ports
  - Up to four 8-bit I/O ports; alternate port functions, such as external interrupts and the serial interface are separated, providing extra port pins when compared with the standard 8051
- Serial 0: a full-duplex serial interface (80C51-like), equipped with additional baud rate generator
- Serial 1: an asynchronous-only version of Serial 0
- 15-bit programmable Watchdog timer
- SPI Master/Slave interface
- One or two I2C™ Master/Slave interfaces

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Implementation Results

R8051XC reference designs have been evaluated in a variety of technologies. The following table presents sample results for the R8051XC-A configuration.

Device		Area	Speed
ASIC	UMC 0.25 um	13k gates	155 MHz
	UMC 0.18 um	13.3k gates	210 MHz

Notes:

R8051XC-A Configuration optimized for speed

Configurability

A spreadsheet-like Design Configurator is available to help in the selection of the core's many options. The configurable options include:

- Size of external data/program memory: 64 KB to 8 MB
- Number of DPTR registers: 1, 2 or 8
- Arithmetic support for DPTRs: yes or no
- Two types of interrupt controller: Type 51 Type 515
  - interrupt sources: 0 … 6 0 … 18
  - external interrupts: 0 … 2 0 … 13
  - priority levels: 2 4
- Number of 8-bit I/O ports: 0 to 4
- Number of 16-bit timers: 0 to 3
- Number or serial ports: 0, 1, or 2
- Watchdog timer: yes or no
- Multiplication-Division unit: yes or no
- DMA Channels: 0 to 8
- I2C master-slave interface: 0, 1, or 2
- SPI master-slave interface: yes or no
- On-chip debug support: OCDS, FS2 OCI, or none
  For OCDS:
  - Number of hardware breakpoints: 2 to 8
  - Program trace: yes or no
  - Data & program trace: yes or no
- Rarely used instructions MUL, DIV, DA: yes or no
- Software Reset: yes or no
- Support for external DMA operations: yes or no
- Real Time Clock: yes or no

The 8051-like prepackaged R051XC-A core includes: 64kB memory interface, two timers, one serial port, four parallel I/O Ports, two-level interrupt controller, and two DPTR registers.

The 80515-like prepackaged R8051XC-B core includes: 64kB memory interface, three timers, two serial ports, four parallel I/O ports, watchdog timer, multiplication-division unit, and two DPTR registers.

Performance

The R8051XC is designed to run at frequencies up 230 MHz on typical 0.18-micron process. It uses from 6K to 70K gates depending on the technology and configuration. The R8051XC is a technology independent design that can be implemented in a variety of process technologies.

The architecture eliminates redundant bus states and implements parallel processing of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most of the 1-byte instructions are performed in a single cycle. The R8051XC uses 1 clock per cycle. This leads, together with other extensions (mutli-DPTR, MDU) to performance improvement at rate of 9.6 (in terms of DMIPS) with respect to the Intel device working with the same clock frequency.

The table below shows the speed advantage of the R8051XC over the standard 8051. A speed advantage of 12 means that the R8051XC performs the same instruction twelve times as fast as the 8051.

Speed advantage	Number of instructions	Number of opcodes
24	1	1
12	31	101
9.6	2	2
8	21	38
6	41	94
4	15	19
Average: 8.1	Sum: 111	Sum: 255

The average of speed advantage is 8.1. However, the real speed improvement seen in any system will depend on the instruction mix.

Performance		
Configuration:	Dhrystones/Mhz	Ratio
Basic	113.9	6.9
Multiple DPTR	142.2	8.6
Multiple DPTR+auto-inc	154.1	9.3
MDU+Multiple DPTR+auto-inc	157.8	**9.6**

The following table shows example implementation results for 0.18 um technology for range of predefined configurations.

Configuration	Speed[1]	Area [2]
R8051XC CPU.	230 MHz	6.2k gates
R8051XC–A	210 MHz	11.2k gates
R8051XC–B	210 MHz	17k gates
R8051XC–F	200 MHz	55.1k gates

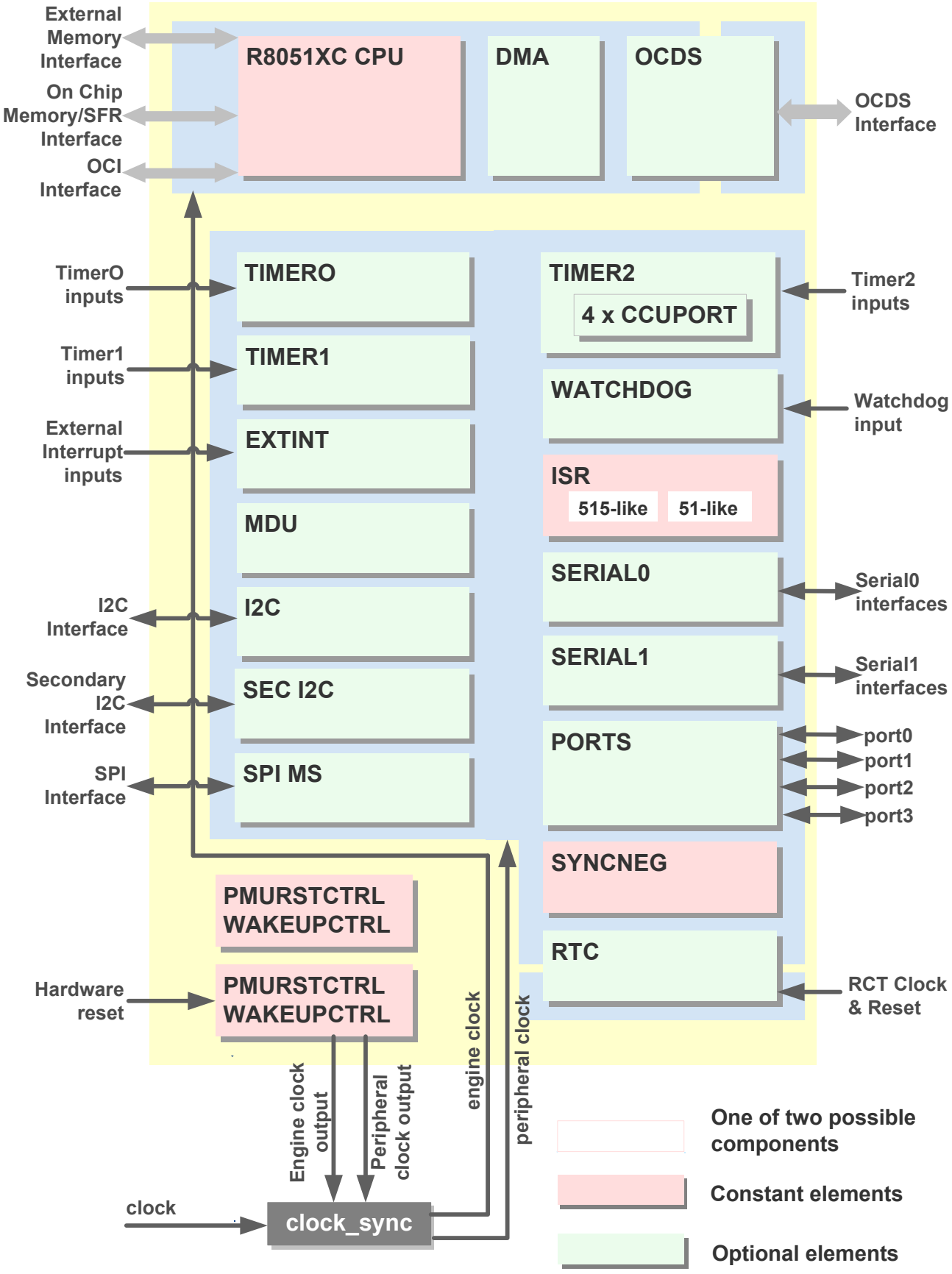
Notes:

[1] Implemented with optimization set for speed

[2] Implemented with constraints set for minimal area

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Block Diagram



Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

Central Processing Unit

The CPU fetches instructions from program memory and uses RAM or SFRs as operands. Provides the ALU for 8-bit arithmetic, logic, multiplication and division operations, and Boolean manipulations. The RAM and SFR interface can address up to 256 bytes of Read/Write Data Memory Space and built-in and off-core Special Function Registers. The memory interface can address from 64KB to 8MB of Program Memory, and from 64KB up to 8MB of External Data Memory. It uses a HOLD interface to support any external DMA controller, and it eases the connection to memories using a de-multiplexed address/data bus. The variable-length code fetch and MOVC to access fast or slow program memory, and similarly a variable-length MOVX to access fast or slow RAM or peripherals are provided.

DMA Controller

The Direct Memory Access (DMA) Controller contains up to eight individual Channels, each capable of transferring data from or to any addressable location (program memory, internal or external data memory, or SFR). Each channel can work in synchronous mode (when just one byte is transferred at each trigger) or asynchronous mode (when all the data is transferred at each trigger). Transfers can be triggered by software or by specified interrupt source.

Ports

The parallel I/O port controller serves up to four parallel 8-bit I/O ports to be used with off-core buffers. It is compatible with the classic 80C51, but lacks the multiplexed memory bus feature and alternate functions. (These could be combined off-core if required).

Timers 0 and 1

Timers 0 and 1 are nearly identical, and they each have these three modes: 13-bit timer/counter, 16-bit timer/counter, and 8-bit timer/counter with auto reload. Timer 0 has an additional mode: two 8-bit timers. Each timer can also count external pulses (1 to 0 transition) on the corresponding t0 or t1 pin. Another option is to gate the timer/counter using an external control signal, which allows it to measure the pulse width of external signals.

Timer 2

Operates as a timer, event counter, or gated timer.

In timer mode, the Timer 2 can be incremented every 12 or 24 clock cycles, depending on the prescaler setting. In event counter mode, Timer 2 is incremented when an external signal changes from 1 to 0 (sampled every machine cycle). Timer 2 is incremented in the cycle following the one in which that transition was detected. In gated timer mode, Timer 2's incrementing is gated by an external signal.

A Timer 2 reload can be executed in two modes. In Mode 0, the reload signal is generated by a Timer 2 overflow (auto reload), while in Mode 1 it is generated by a negative transition at the corresponding input pin t2ex.

Pin Description

Name	Type	Polarity/ Bus size	Description
General signals			
clkcpu	I	Rise	**Engine clock** Pulse for internal circuits, which are stopped in IDLE or STOP mode
clkcpuen	O	High	**Engine clock enable output** External control for the "clkcpu" clock, when set to 1 the "clkcpu" input should be running, otherwise the "clkcpu" should be stopped
clkper	I	Rise	**Peripheral clock** Pulse for internal circuits, which are stopped in STOP mode
clkperen	O	High	**Peripheral clock enable output** External control for the "clkper" clock, when set to 1 the "clkper" input should be running, otherwise the "clkper" should be stopped
reset	I	High	**Hardware reset input** High level on this pin for two clock cycles while the oscillator is running resets the device
ro	O	High	**Reset output** Set active when either the Hardware Reset, Watchdog Timer, Software Reset or OCDS generates reset signal to the core
swd	I	High	**Start Watchdog Timer input** High level on this pin during reset starts the watchdog timer immediately after reset is released
Real Time Clock signals			
rtcx	I	Rise/Fall	RTC 32,768kHz clock input
rtcreset	I	High	RTC reset input
Port 0			
port0i port0o	I O	8 8	8-bit bi-directional I/O port with separated inputs and outputs
Port 1			
port1i port1o	I O	8 8	8-bit bi-directional I/O port with separated inputs and outputs
Port 2			
port2i port2o	I O	8 8	8-bit bi-directional I/O port with separated inputs and outputs
Port 3			
port3i port3o	I O	8 8	8-bit bi-directional I/O port with separated inputs and outputs

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Compare-Capture Unit

The CCU within Timer2 performs Compare and Capture functions. For the Compare function, values stored in four 16-bit compare/capture registers are compared with the contents of the Timer 2 register. The results are signaled on the "ccubus" outputs and interrupts are generated.

For the Capture function actual timer/counter contents can be saved into one of four 16-bit registers upon an external event (Mode 0) or software write operation (Mode 1).

Multiplication Division Unit

This on-chip arithmetic unit performs these unsigned integer operations:

- 16 x 16 bit multiplication
- 32 / 16 bit division and 16 / 16 bit division
- 32 bit normalization and L/R shifting

The MDU allows operations to occur concurrently to and independent of the engine activity.

Serial 0 and 1

The core includes two fully independent serial ports for simultaneous communication over two channels. They can operate in identical or different modes and at different communication speeds. Serial Port 0 is capable of both synchronous and asynchronous transmission while Serial 1 provides asynchronous mode only.

In synchronous mode, the microcontroller generates a clock and operates in half-duplex mode. In asynchronous mode, full duplex operation is available. Received data is buffered in a holding register, which allows the serial ports to receive an incoming word before the software has read the previous value.

Serial Port 0 offers the following communication protocols:

- Synchronous mode, fixed baud rate
- 8-bit UART mode, variable baud rate
- 9-bit UART mode, variable or fixed baud rate

Serial Port 1 has two operating modes:

- 8-and 9-bit UART mode, variable baud rate

Both include an additional Baud Rate Generator.

Power Management Unit & Reset Control

Generates clock enable signals for the main CPU and for peripherals; serves Power Down Modes IDLE and STOP; and generates an internal synchronous reset signal (upon external reset, watchdog timer overflow or software reset condition).

The IDLE mode leaves the clock of the internal peripherals running. Power consumption drops because the CPU is not active. Any interrupt or reset will wake the CPU.

The STOP mode turns off all internal clocks. The CPU will exit this state with an external interrupt or reset. Internally generated interrupts (timer, serial port, watchdog, ...) are disabled since they require clock activity.

Wake-up Control

The Wake-up From Power-Down Mode Control Unit services two external interrupts during power-down modes. They can combinationally force the clock enable outputs back to active state so the clock generation can be resumed.

Pin Description - Continued

Name	Type	Polarity/ Bus size	Description
External interrupt inputs			
int0	I	Low/Fall	External interrupt 0
int1	I	Low/Fall	External interrupt 1
int2	I	Fall/Rise	External interrupt 2
int3	I	Fall/Rise	External interrupt 3
int4	I	Rise	External interrupt 4
int5	I	Rise	External interrupt 5
int6	I	Rise	External interrupt 6
int7	I	Rise	External interrupt 7
int8	I	Rise	External interrupt 8
int9	I	Rise	External interrupt 9
int10	I	Rise	External interrupt 10
int11	I	Rise	External interrupt 11
int12	I	Rise	External interrupt 12
Serial 0 interface			
rxd0i	I	-	Serial 0 receive data
rxd0o	O	-	Serial 0 transmit data
txd0	O	-	Serial 0 transmit data or receive clock in mode 0
Serial 1 interface			
rxd1	I	-	Serial 1 receive data
txd1	O	-	Serial 1 transmit data
Timers inputs			
t0	I	Fall	Timer 0 external input
t1	I	Fall	Timer 1 external input
t2	I	Fall	Timer 2 external input
t2ex	I	Fall	Timer 2 capture trigger
Compare – Capture Unit			
cc(0)	I	Rise/Fall	Compare/Capture 0 input
cc(3:1)	I	Rise	Compare/Capture 1-3 inputs
ccubus	O	4	Compare/Capture outputs
External memory interface			
mempsack	I	High	Program memory read acknowledge
memack	I	High	Data memory acknowledge
memdatai	I	8	Memory data input
memdatao	O	8	Memory data output
memaddr	O	16..23	Memory address
mempswr	O	High	Program store write enable
mempsrd	O	High	Program store read enable
memwr	O	High	Data Memory write enable
memrd	O	High	Data Memory read enable
Internal Data Memory interface			
ramdatai	I	8	Data bus input
ramdatao	O	8	Data bus output
ramaddr	O	8	Data file address
ramwe	O	High	Data file write enable
ramoe	O	High	Data file output enable

Real Time Clock

The RTC provides a real-time count with a resolution of 1/256th second and range of 179 years. It can set and read seconds, minutes, hours, day of the week, and the date, represented by a 16-bit number interpreted by software. An alarm function can generate interrupts periodically or at a specific time, and these may be used to wake up from IDLE/STOP mode.

SFR Mux

The SFR Multiplexer provides a common bus multiplexer for all the internal and external Special Function Registers.

OCDS

The OCDS unit serves interface for On-Chip Debug Support through an IEEE1149.1 (JTAG) port. The OCDS unit provides the following functions:

- Run, Stop, Single-step
- Software breakpoint
- Debugger program execution
- Hardware breakpoints
- Read/Write Access to Program Memory, External/Internal Data Memory and SFRs
- Program Trace and Data Trace (optional)

Watchdog Timer

A 15-bit counter that is incremented every 24 or 384 clock cycles. After an external reset, it is disabled and all registers are set to zeros. It can be started by applying an active input during reset (hardware automatic start) or by setting the enable bit by software. Once started, it cannot be stopped unless the external reset signal becomes active.

When the Watchdog enters the state of 7CFFh, it activates a dedicated flag and forces internal reset. It can be avoided by refreshing the Watchdog with software before it reaches 7CFFh.

Interrupt Service Routine Unit

The R8051XC provides two types of interrupt controllers: an 8051-compatible with up to six interrupt sources and two priority levels, or an 80515-compatible with up to eighteen interrupt sources and four priority levels. Each source has its own request flag(s) located in a dedicated SFR. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

Primary and Secondary I2C™ Interfaces

The primary (I2C) and secondary (SEC_I2C) I2C Bus Controllers each provide a serial interface that meets the Philips I2C bus specification v1.0 and support all master/slave receiver/transmitter modes. Each is a true multi-master bus controller, including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer. They perform 8-bit oriented, bi-directional data transfers up to 100 kbit/s in the standard mode, or up to 400 kbit/s in the fast mode

Serial Peripheral Interface (SPI) Interface

Provides full-duplex, synchronous communication between the core and other peripheral devices, including other MCUs. It can operate either as Master or Slave, with programmable clock rate, phase, and polarity. The maximum data rate is ¼ of the system clock for a Slave, and ½ of the system clock for a Master. Write collision and overrun detection protect data, and Master mode fault detection for multi-master systems prevents bus conflict.

Pin Description - Continued

Name	Type	Polarity/ Bus size	Description
External Special Function Registers interface			
sfrdatai	I	8	SFR data bus input
sfrdatao	O	8	SFR data bus output
sfraddr	O	7	SFR address
sfrwe	O	High	SFR write enable
sfroe	O	High	SFR output enable
External memory interface for rising-edge triggered synchronous memories			
memdatao_comb	O	8	Memory data output
memaddr_comb	O	16..23	Memory address
mempswr_comb	O	High	Program store write enable
mempsrd_comb	O	High	Program store read enable
memwr_comb	O	High	Data Memory write enable
memrd_comb	O	High	Data Memory read enable
Internal Data Memory interface for rising-edge triggered synchronous memories			
ramdatao_comb	O	8	Data bus output
ramaddr_comb	O	8	Data file address
ramwe_comb	O	High	Data file write enable
ramoe_comb	O	High	Data file output enable
External Special Function Registers interface for rising-edge triggered synchronous devices			
sfrdatao	O	8	SFR data bus output
sfraddr	O	7	SFR address
sfrwe	O	High	SFR write enable
sfroe	O	High	SFR output enable
On-Chip Instrumentation interface (OCI)*			
debugreq	I	High	Debug mode request
debugstep	I	High	Debug mode single-step
debugprog	I	High	Debugger program select
debugack	O	High	Debugger acknowledge signal
flush	O	High	First fetch after branch indicator
fetch	O	High	Fetch from program memory, when flush inactive
waitstaten	O	Low	Waitstate indicator
acc	O	8	Accumulator register output
On-Chip Debug Support interface (OCDS)*			
trst	I	Low	Debug logic reset input (IEEE1149.1 Test Logic Reset)
tck	I	High	Debug clock (IEEE1149.1 Test Clock)
tms	I	High	Test Mode Select (IEEE1149.1 Test Mode Select)
tdi	I	High	Debug Data Input (IEEE1149.1 Test Data Input)
tdo	O	High	Debug Data Output (IEEE1149.1 Test Data Output)
tdoenable	O	High	Debug Data Output Enable

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Verification Methods

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models.

The core satisfies the requirements of the Reuse Methodology Manual and the VSIA Quality IP Metric.

Quality IP Assessment	Score
IP Ease of Reuse	97%
Design & Verification Quality	83%
IP Maturity	100%
Vendor Assessment	82%
Total	**89%**

The R8051XC has been verified through extensive functional simulation and it has achieved high Code Coverage simulation results.

Code Coverage	Metric
Statement	100 %
Branch	96.7 %
Condition	80.5 %
Triggering	-
Path	62.9 %
Toggle	93.1 %

The trial ATPG coverage figures met the requirements and reached level of 99%. Additionally the value of IDDQ reached level of 99%.

Related Products

SPI-MS - Serial Peripheral Interface supporting slave as well as master capability with own rate generator and programmable polarity of serial clock. A dedicated set of slave selection signals facilitates integration in multi slave system;

I2C – controller which meets the original Philips I2C bus interface controller specification requirements. It may operate in one of the following transmission modes: Master Transmitter, Master Receiver, Slave Transmitter and Slave Receiver with transmission rates up to 400 kHz;

I2CS – controller compatible with the Philips I2C bus interface slave controller. It may operate in one of the following transmission modes: Slave Transmitter and Slave Receiver with transmission rates up to 400 kHz.

Third Party Reference

The R8051XC core may be delivered with debug instrumentation implemented and ready to work with Keil uVision debug environment. For more details about On Chip Debug Support visit Evatronix web site http://www.evatronix.pl.

Following is a link to the R8051XC on the list of devices that are supported by the Keil development tools http://www.keil.com/dd/chip/4122.htm.

Pin Description – Continued

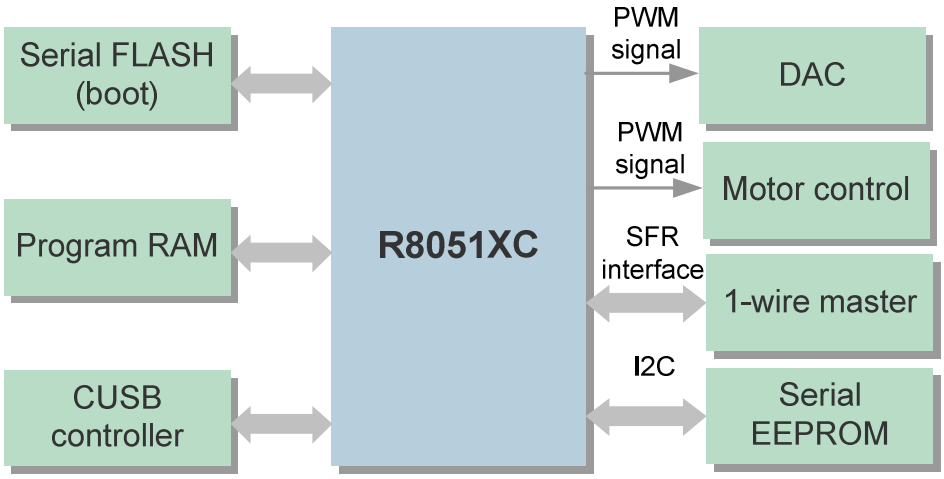
Name	Type	Polarity/ Bus size	Description
Trace RAM signals (OCDS)*			
addr_buf0	O	4	Trace buffer 0 address bus
addr_buf1	O	4	Trace buffer 1 address bus
datao_buf0	O	45	Trace buffer 0 data output
datao_buf1	O	45	Trace buffer 1 data output
datai_buf0	I	45	Trace buffer 0 data input
datai_buf1	I	45	Trace buffer 1 data input
wr_buf0	O	High	Trace buffer 0 write enable
wr_buf1	O	High	Trace buffer 1 write enable
rd_buf0	O	High	Trace buffer 0 read enable
rd_buf1	O	High	Trace buffer 1 read enable
Hold interface			
hold	I	High	Hold mode request
holda	O	High	Hold mode acknowledge signal
intoccur	O	High	Interrupt occured in Hold mode
I2C™ interface			
scli	I	High	I2C serial clock input
sclo	O	High	I2C serial clock output
sdai	I	-	I2C data input
sdao	O	-	I2C data output
Secondary I2C™ interface			
scl2i	I	High	I2C serial clock input
scl2o	O	High	I2C serial clock output
sda2i	I	-	I2C data input
sda2o	O	-	I2C data output
SPI interface			
ssn	I	Low	SPI Slave Select input
misoi	I	-	SPI Master Input / Slave Output bidirectional port – input part
misoo	O	-	SPI Master Input / Slave Output bidirectional port – output part
misotri	O	High	SPI Master Input / Slave Output bidirectional port – output enable
mosii	I	-	SPI Master Output / Slave Input bidirectional port – input part
mosio	O	-	SPI Master Output / Slave Input bidirectional port – output part
mositri	O	High	SPI Master Output / Slave Input bidirectional port – output enable
scki	I	Rise/Fall	SPI Serial Clock bidirectional port – input part
scko	O	Rise/Fall	SPI Serial Clock bidirectional port – output part
scktri	O	High	SPI Serial Clock bidirectional port – output enable
spssn	O	8	8-bit output port to control external slave devices

*The OCI and OCDS are mutually exclusive

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Example Application

The following figure presents an example application of the R8051XC core.



Standard Deliverables

- HDL source code for the R8051XC
- Synthesis support (Synopsys)
  - A complete set of synthesis scripts
- Simulation support (MTI, Cadence)
  - A set of scripts and macros
- Extensive VHDL or Verilog 2001 Test Bench that instantiates:
  - The R8051XC Microcontroller
  - The R8051XC CPU behavioral model
  - Clock and reset generator
  - External RAM model
  - Program Memory model including random code generation mode
  - Memory access comparators
  - Verification components that drive and compare pins dedicated to several peripherals of the R8051XC
  - A collection of 8051 assembler programs which are executed directly by the Test Bench
  - A set of expected results
- Documentation
  - Design Specification
  - Verification Specification
  - Test Plan
  - Integration Manual
  - Application Notes
- Configuration tool for easy use with the R8051XC-F
- Reference design for propriety development board
  This design uses the R8051XC and illustrates how to build and connect memories and port modules

Options

Typically the core is delivered as either VHDL or Verilog source code for ASIC implementations. The following options may be ordered according to user's requirements.

- Pre-configured R8051XC-A or R8051XC-B versions
- Fully configurable R8051XC-F version
- EDIF netlist for FPGA and low volume production
- Complete debug solution including software plug-in for Keil environment and USB Pod
- Annual maintenance
- On-site support and training

Product Versions

The core can be delivered as either pre-configured version (A or B) or fully configurable source code.

R8051XC-A – predefined configuration with peripheral set compatible to Intel 80C31 including: 2 Timers, Serial port, 4 Parallel Ports, 2 Level Interrupt Controller

R8051XC-B – predefined configuration with peripherals compatible to Siemens 80C515 and 80C517, including: 3 Timers, 2 Serial ports, 4 Parallel ports, Watchdog, Multiplication-Division Unit, Dual DPTR

R8051XC-F – fully configurable version extending R8051XC-B with: I2C serial port, SPI port, memory banking, arithmetic support for DPTRs, 8 DPTRs, possibility of instruction set reduction.

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