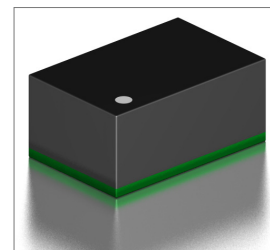


Features

- ± 20 ppb (Frequency Stability) Available
- CMOS
- (VC)OCXO
- Small Package

Applications

- Military Communication Equipment
- Base Stations
- Test Equipment
- Synthesizers
- Digital Switching



Part Numbering Guide

SOC 14 C 03 K 15 V H - 10.000M

SUNTSU OCXO

14.4mm x 9.4mm

CMOS

SUPPLY VOLTAGE
03 : 3.3V $\pm 5\%$

FREQUENCY STABILITY
K : ± 50 ppb
L : ± 30 ppb
M : ± 20 ppb
N : ± 10 ppb

OPERATING TEMPERATURE RANGE
05 : 0°C - +50°C
15 : -10°C - +55°C
27 : -20°C - +70°C
38 : -30°C - +85°C
48 : -40°C - +85°C
49 : -40°C - +95°C

OCXO/VCOCXO
BLANK : OCXO
V : VCOCXO

FREQUENCY
MHz

PULLABILITY
BLANK : OCXO
H : ± 3.0 ppm



Cage Code: 4GUT4

To customize your parameters contact a Suntsu representative.

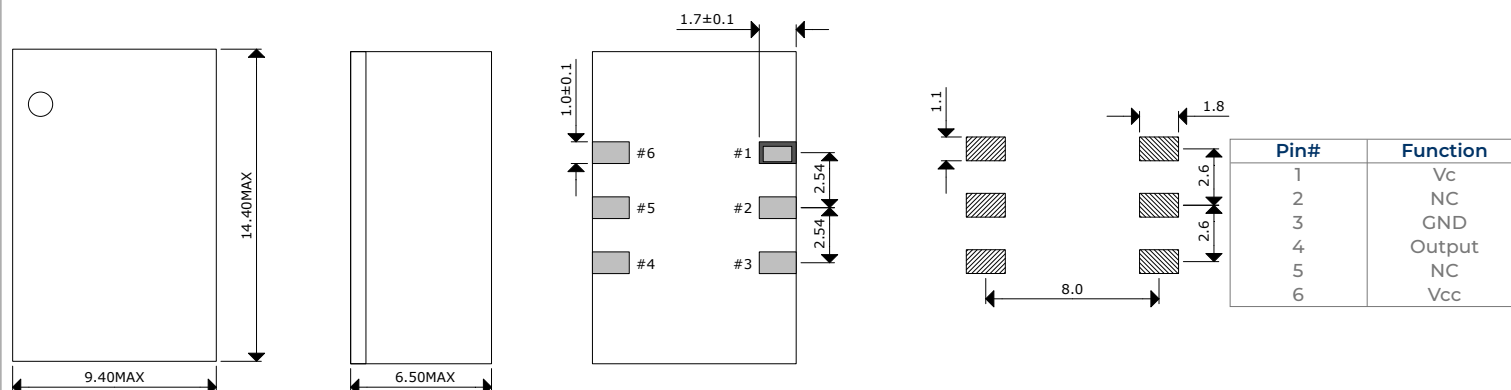
* For frequency stability option N contact a Suntsu Sales representative.

** For operating temperatures of -40 - +95°C Contact a Suntsu representative.

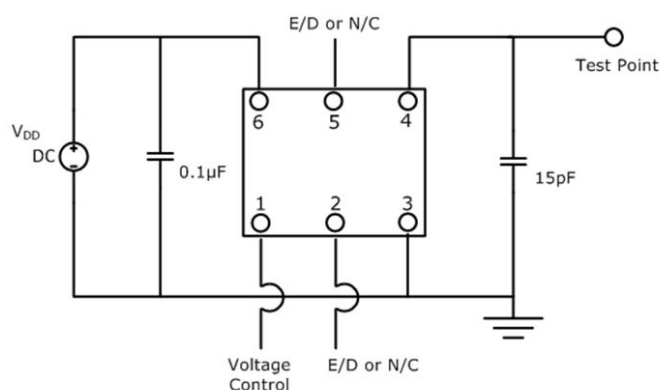
Electrical Parameters	Units	Minimum	Typical	Maximum	Remarks
Frequency Range	MHz	10		40	
Frequency Tolerance at +25°C	ppm	-0.5		+0.5	
Freq. Stability vs. Op Temp.	ppb	-10		+10	See part numbering guide for options.
Freq. Stability vs. Supply Voltage	ppb	-10		+10	V _{DD} $\pm 5\%$ Change
Freq. Stability vs. Load	ppb	-10		+10	$\pm 5\%$ Change
Freq. Stability vs. Aging/Year	ppm	-1		+1	
Operating Temperature	°C	-40		+95	See part numbering guide for options.
Storage Temperature	°C	-55		+125	
Supply Voltage (V _{DD})	V	3.135	3.3	3.465	
Power Consumption At Turn On	W			2.0	
Power Consumption At 25°C	W			0.5	
Control Voltage (V _c)	V	0		3.3	
Control Middle Voltage	V		1.65		
Pullability	ppm		± 3.0		
Linearity	%			10	
V _c Input Impedance	K Ω	50			
Deviation Slope			Positive		
Output Logic (CMOS)	pF			15	
Output Logic Level - High (V _{OH})	V	0.9*V _{DD}			
Output Logic Level - Low (V _{OL})	V			0.1*V _{DD}	
Rise Time (T _R) And Fall Time (T _F)	ns			5	
Symmetry (Duty Cycle)	%	45	50	55	
Start-Up Time	ms			3	
Warm-Up Time	Mins		3		
Phase Noise (Typical) 1Hz Offset	dBc/Hz		-60		
Phase Noise (Typical) 100Hz Offset	dBc/Hz		-120		
Phase Noise (Typical) 1kHz Offset	dBc/Hz		-150		

Outline Drawing & Land Pattern

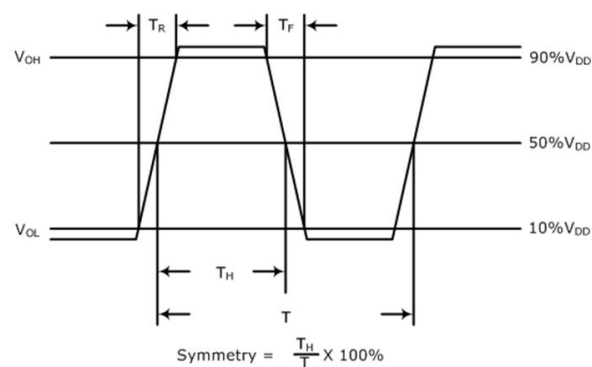
All dimensions are in millimeters (mm) unless otherwise noted. Drawings are not to scale.



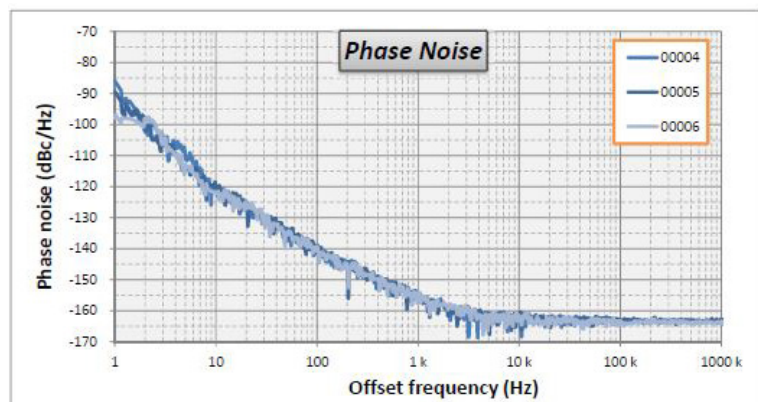
Test Circuit (CMOS)



Waveform (CMOS)

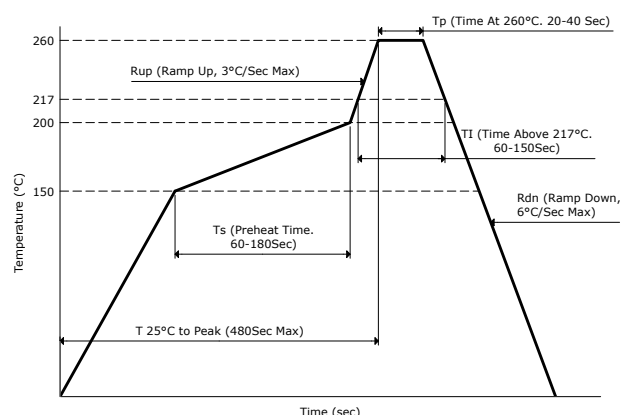


Typical Phase Noise

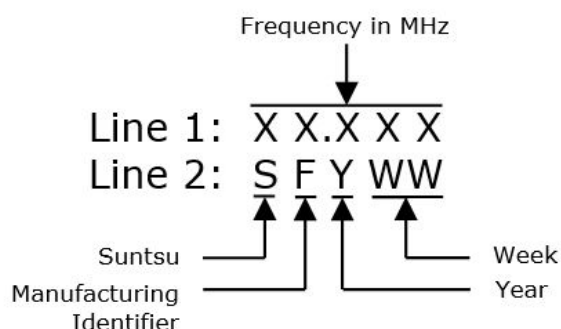


DUT #	Phase noise at offset frequency (dBc/Hz)						
	1Hz	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz
Typ. Spec.	-70.0	-102.0	-131.0	-148.5	-153.0	-155.0	-155.0
00004	-85.9	-121.3	-140.3	-156.4	-163.8	-163.4	-162.9
00005	-89.4	-120.3	-138.9	-155.2	-162.8	-162.8	-163.4
00006	-98.0	-122.0	-139.3	-156.7	-162.1	-163.3	-163.8

Reflow Profile



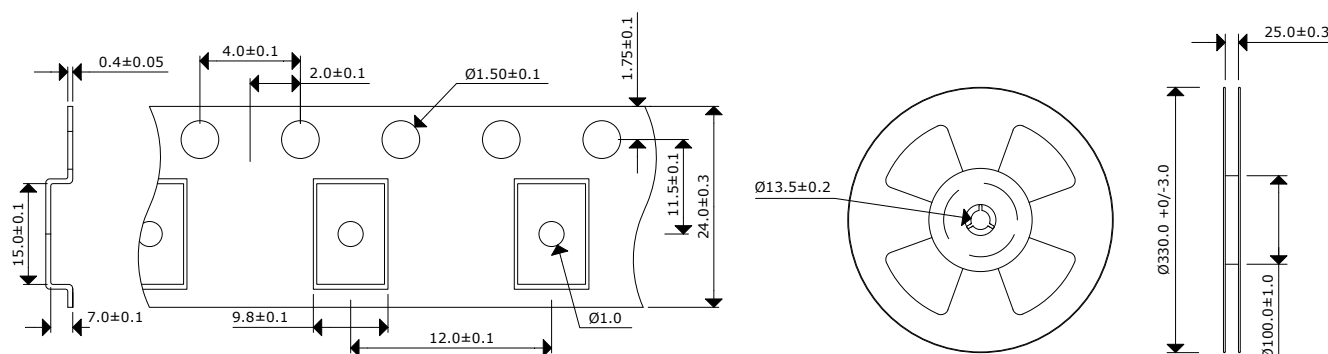
Part Marking



Tape And Reel Dimensions

800pcs/Reel

All dimensions are in millimeters (mm) unless otherwise noted. Drawings are not to scale.



Environmental Specifications

Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Lead Integrity	MIL-STD-883, Method 1014, Condition A
Gross Leak Test	MIL-STD-883, Method 1014, Condition C
Solderability	MIL-STD-883, Method 2003

Mechanical Specifications

Mechanical Shock	MIL-STD-202, Method 213, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition A
Resistance to Solvents	MIL-STD-202, Method 215