

# Accutek Microcircuit Corporation

## AK48256S / AK48256G 262,144 X 8 Bit MOS Dynamic Random Access Memory

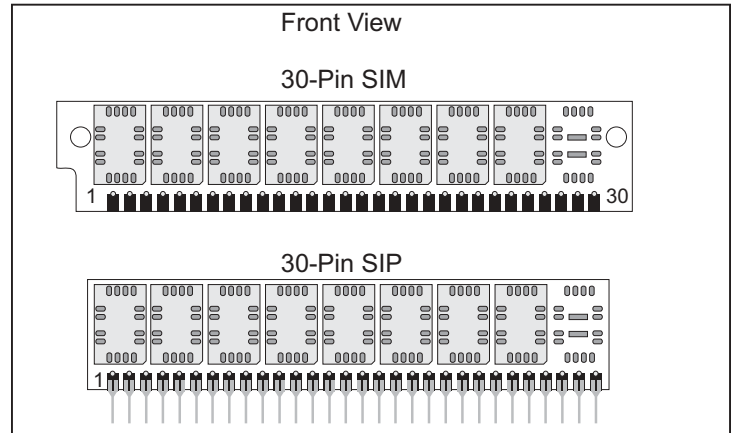
### DESCRIPTION

The Accutek AK48256 high density memory modules is a random access memory organized in 256K x 8 bit words. The assembly consists of eight standard 256K x 1 DRAMs in plastic leaded chip carriers (PLCC) mounted on the front side of a printed circuit board. The module can be configured as a leadless 30 pad SIM or a leaded 30 pin SIP. This packaging approach provides a 6 to 1 density increase over standard DIP packaging.

The operation of the AK48256 is identical to eight 256K x 1 DRAMs. The data input is tied to the data output and brought out separately for each device, with common RAS, CAS and WE control. This common I/O feature dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable (WE) signal must always go low before CAS in a write cycle, Read-Write and Read-Modify-Write operation is not possible.

### FEATURES

- 262,144 by 8 bit organization
- Optional 30 Pad leadless SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- JEDEC standard pinout
- Each device has common D and Q lines with common RAS, CAS and WE control
- 2.8 Watt active and 180 mW standby (max)
- Operating free air temperature 0°C to 70°C
- Upward compatible with AK481024, AK581024, AK584096 and AK5816384
- Functionally and Pin compatible with AK58256A



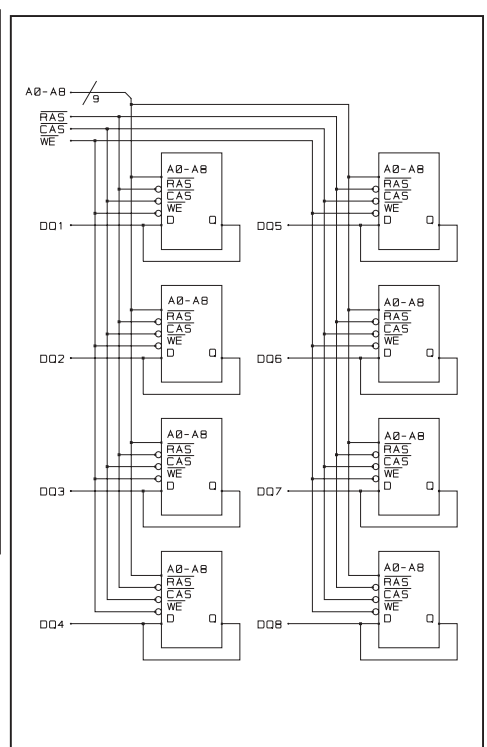
### PIN NOMENCLATURE

A <sub>0</sub> - A <sub>8</sub>	Address Inputs
DQ <sub>1</sub> - DQ <sub>8</sub>	Data In / Data Out
CAS	Column Address Strobe
RAS	Row Address Strobe
WE	Write Enable
Vcc	5v Supply
Vss	Ground
NC	No Connect

### PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL
1	Vcc	16	DQ5
2	CAS	17	A8
3	DQ1	18	NC
4	A0	19	NC
5	A1	20	DQ6
6	DQ2	21	WE
7	A2	22	Vss
8	A3	23	DQ7
9	Vss	24	NC
10	DQ3	25	DQ8
11	A4	26	NC
12	A5	27	RAS
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	Vcc

### FUNCTIONAL DIAGRAM



### MODULE OPTIONS

Leadless SIM: AK48256S
Leaded SIP: AK48256G

## ORDERING INFORMATION

### PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8										
<b>1 Product</b>	<b>AK = Accuthek Memory</b>																	
<b>2 Type</b>	4 = Dynamic RAM 5 = CMOS Dynamic RAM 6 = Static RAM																	
<b>3 Organization/Word Width</b>	1 = by 1    16 = by 16 4 = by 4    32 = by 32 8 = by 8    36 = by 36 9 = by 9																	
<b>4 Size/Bits Depth</b>	64 = 64K    4096 = 4 MEG 256 = 256K    8192 = 8 MEG 1024 = 1 MEG    16384 = 16 MEG																	
<b>5 Package Type</b>	G = Single In-Line Package (SIP) S = Single In-Line Module (SIM) D = Dual In-Line Package (DIP) W = .050 inch Pitch Edge Connect Z = Zig-Zag In-Line Package (ZIP)																	
<b>6 Special Designation</b>	P = Page Mode N = Nibble Mode K = Static Column Mode W = Write Per Bit Mode V = Video Ram																	
<b>7 Separator</b>	- = Commercial 0°C to +70°C M = Military Equivalent Screened (-55°C to +125°C) I = Industrial Temperature Tested (-45°C to +85°C) X = Burned In																	
<b>8 Speed (first two significant digits)</b>	<table border="0"> <tr> <td>DRAMS</td> <td>SRAMS</td> </tr> <tr> <td>50 = 50 nS</td> <td>8 = 8 nS</td> </tr> <tr> <td>60 = 60 nS</td> <td>10 = 10 nS</td> </tr> <tr> <td>70 = 70 nS</td> <td>12 = 12 nS</td> </tr> <tr> <td>80 = 80 nS</td> <td>15 = 15 nS</td> </tr> </table>								DRAMS	SRAMS	50 = 50 nS	8 = 8 nS	60 = 60 nS	10 = 10 nS	70 = 70 nS	12 = 12 nS	80 = 80 nS	15 = 15 nS
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The numbers and coding on this page do not include all variations available but are show as examples of the most widely used variations. Contact Accuthek if other information is required.

### EXAMPLES:

#### AK48256SP-10

256K x 8, 100 nSEC DRAM 30 pin SIM Configuration, Page Mode

#### AK48256GK-80

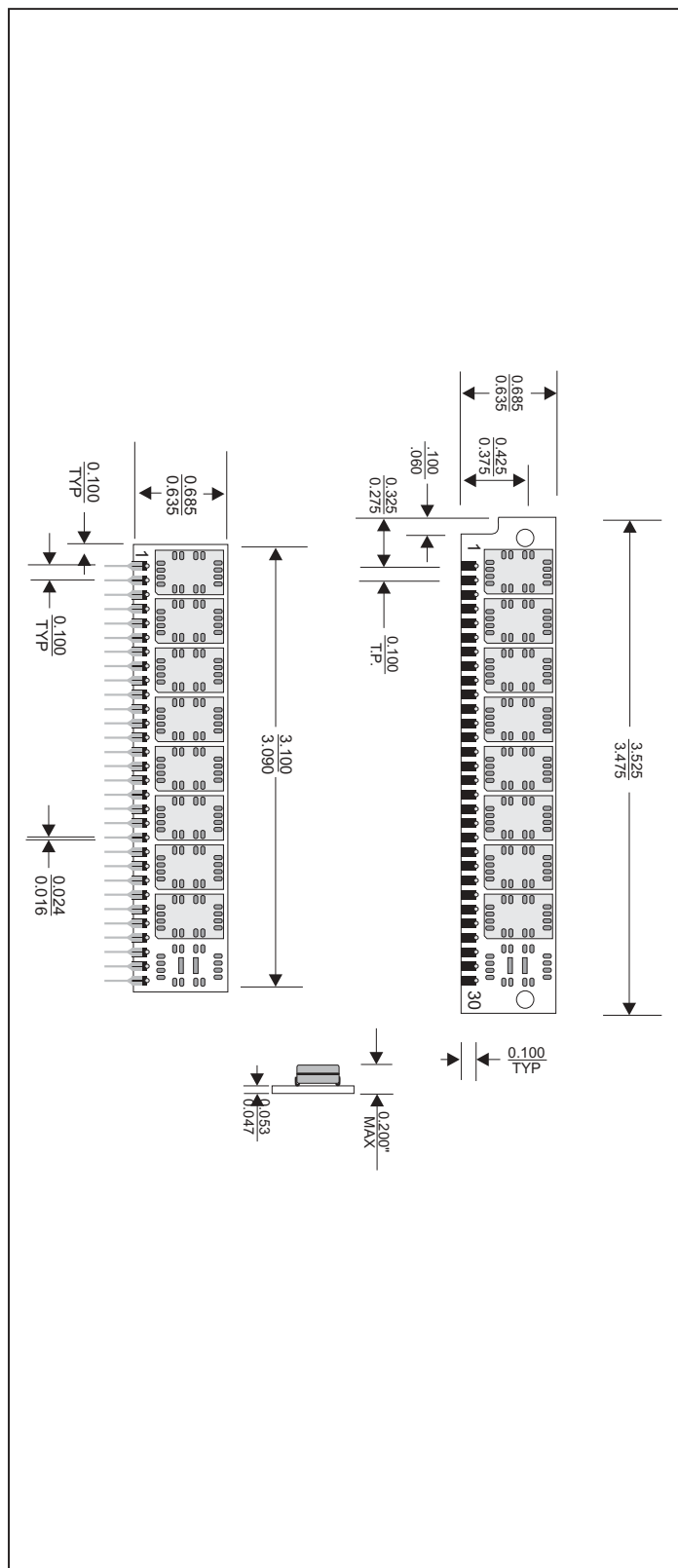
256K x 8, 80 nSEC DRAM 30 pin SIP Configuration, Static Column Mode



**ACCUTEK MICROCIRCUIT CORPORATION**  
 BUSINESS CENTER at NEWBURYPORT  
 2 NEW PASTURE ROAD, SUITE 1  
 NEWBURYPORT, MA 01950-4054  
 VOICE: 978-465-6200 FAX: 978-462-3396  
 Email: sales@accutekmicro.com  
 Internet: www.accutekmicro.com

## MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.