8051 Microcontroller Family Compatible

256K X88257 32,768 x 8 Bit

E^2 Micro-Peripheral

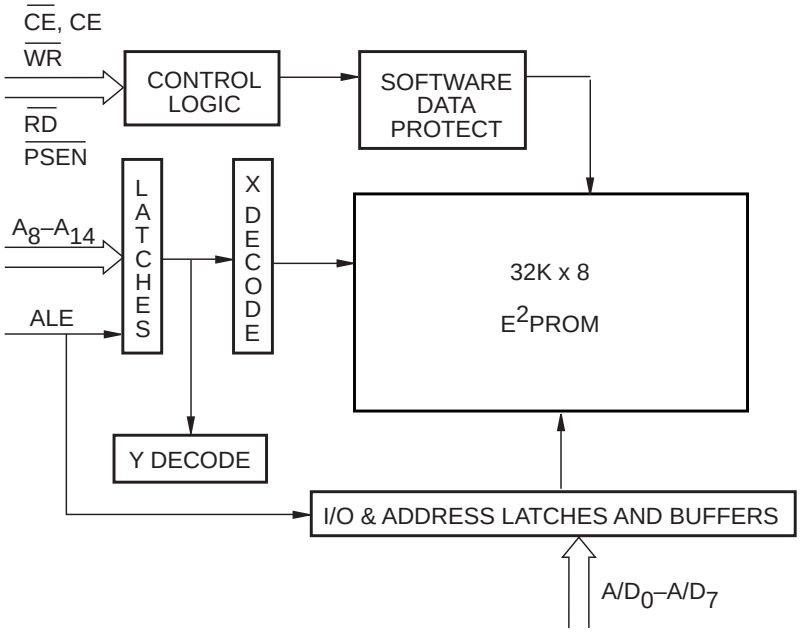
FEATURES

- **Multiplexed Address/Data Bus**
  - **—Direct Interface to Popular 8051 Family**
- **High Performance CMOS**
  - **—Fast Access Time, 120ns**
  - **—Low Power**
    - **—60mA Active Maximum**
    - **—500μA Standby Maximum**
- **Software Data Protection**
- **Toggle Bit Polling**
  - **—Early End of Write Detection**
- **Page Mode Write**
  - **—Allows up to 128 Bytes to be Written in One Write Cycle**
- **High Reliability**
  - **—Endurance: 10,000 Write Cycle**
  - **—Data Retention: 100 Years**
- **28-Lead PDIP Package**
- **28-Lead SOIC Package**
- **32-Lead PLCC Package**

DESCRIPTION

The X88257 is an 32K x 8 E^2PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X88257 features a multiplexed address and data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

FUNCTIONAL DIAGRAM



6509 ILL F02.1

PIN DESCRIPTIONS

Address/Data (A/D_0–A/D_7)

Multiplexed low-order addresses and data. The addresses flow into the device while ALE is HIGH. After ALE transitions from a HIGH to LOW the addresses are latched. Once the addresses are latched these pins input data or output data depending on $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, and $\overline{CE}$.

Addresses (A_8–A_{14})

High order addresses flow into the device when ALE = V_{IH} and are latched when ALE goes LOW.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, ALE is LOW, and CE is LOW, the X88257 is placed in the low power standby mode. If $\overline{CE}$ is used to select the device, the CE must be tied LOW.

Chip Enable (CE)

Chip enable is active HIGH. When CE is used to select the device, the $\overline{CE}$ must be tied HIGH.

Program Store Enable ($\overline{PSEN}$)

When the X88257 is to be used in a 8051-based system, $\overline{PSEN}$ is tied directly to the microcontroller's $\overline{PSEN}$ output.

Read ($\overline{RD}$)

When the X88257 is to be used in a 8051-based system, $\overline{RD}$ is tied directly to the microcontroller's $\overline{RD}$ output.

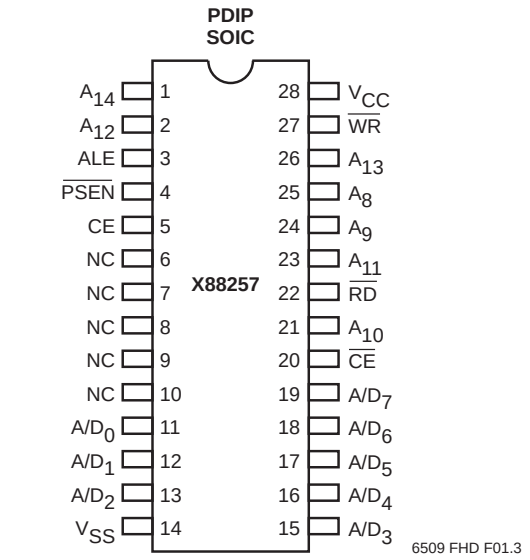
Write ($\overline{WR}$)

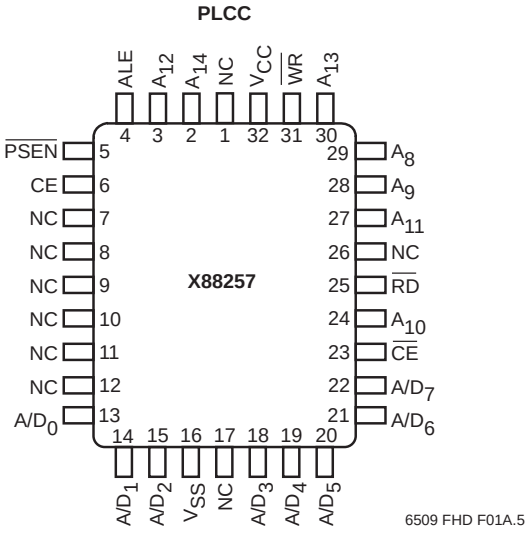
When the X88257 is to be used in a 8051-based system, $\overline{WR}$ is tied directly to the microcontroller's $\overline{WR}$ output.

Address Latch Enable (ALE)

Addresses flow through the latches to address decoders when ALE is HIGH and are latched when ALE transitions from a HIGH to LOW.

PIN CONFIGURATION





PIN NAMES

Symbol	Description
ALE	Address Latch Enable
A/D_0–A/D_7	Address Inputs/Data I/O
A_8–A_{14}	Address Inputs
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
$\overline{PSEN}$	Program Store Enable Input
$\overline{CE}$, CE	Chip Enable
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

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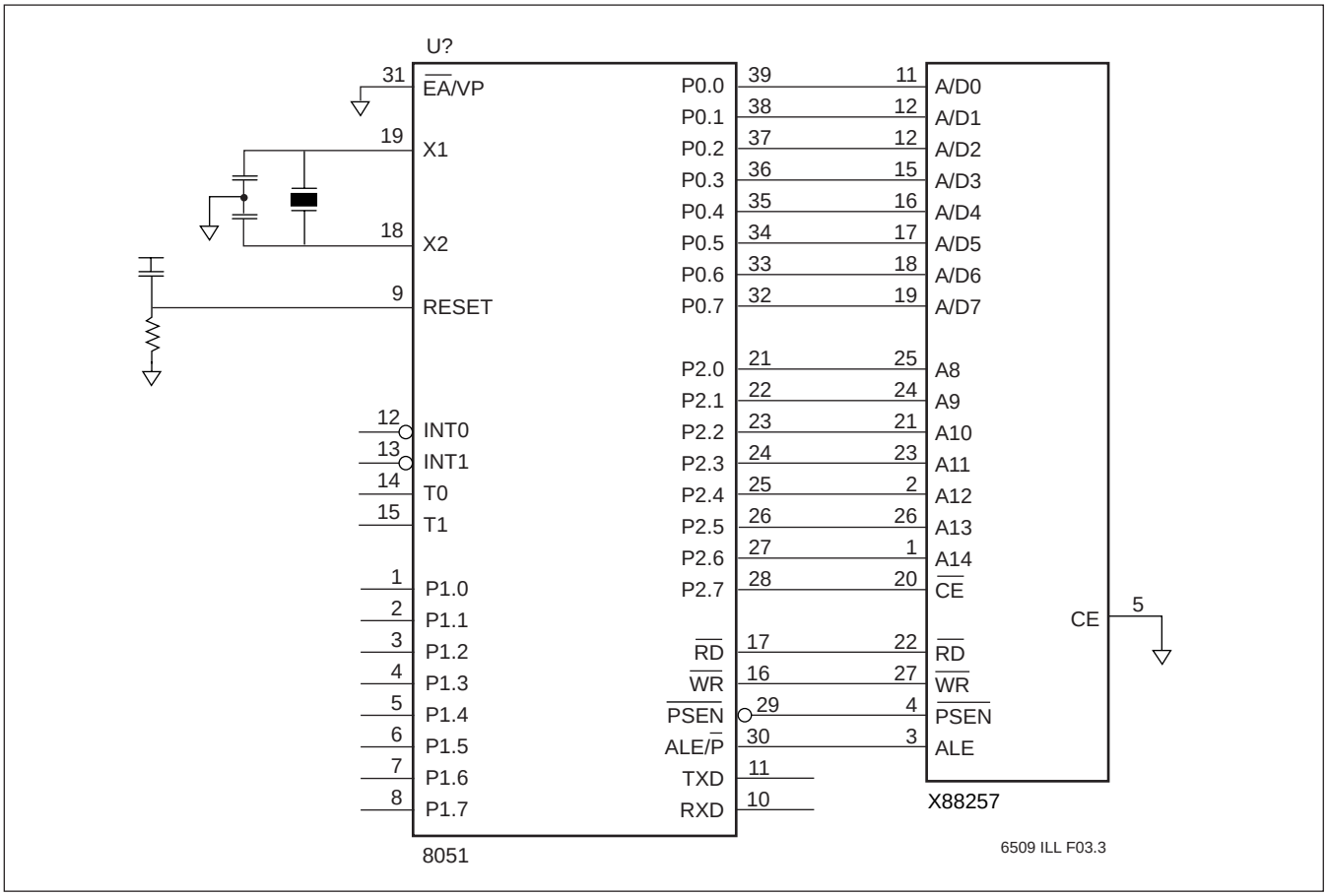
TYPICAL APPLICATION



PRINCIPLES OF OPERATION

The X88257 is a highly integrated peripheral device for a wide variety of single-chip microcontrollers. The X88257 provides 32K-bytes of 5V E²PROM which can be used either for program storage, data storage or a combination of both, in systems based upon Harvard (80XX) architectures. The X88257 incorporates the interface circuitry normally needed to decode the control signals and demultiplex the address/data bus to provide a "seamless" interface.

The interface inputs on the X88257 are configured such that it is possible to directly connect them to the proper interface signals of the appropriate single-chip microcontroller. In the Harvard type system, the reading of data from the chip is controlled either by the $\overline{PSEN}$ or the $\overline{RD}$ signal, which essentially maps the X88257 into both the Program and the Data Memory address map.

The X88257 also features the industry standard 5V E²PROM characteristics such as byte or page mode write and Toggle Bit Polling.

DEVICE OPERATION

Modes—Mixed Program/Data Memory

By properly assigning the address spaces, a single X88257 can be used as both the program and data memory. This would be accomplished by connecting all the 8051 control outputs to the corresponding inputs of the X88257.

Program Memory Mode

This mode of operation is read-only. The $\overline{PSEN}$ and $\overline{ALE}$ inputs of the X88257 are tied directly to the $\overline{PSEN}$ and ALE outputs of the microcontroller. The $\overline{RD}$ and $\overline{WR}$ inputs are tied HIGH.

When ALE is HIGH, the A/D_0–A/D_7 and A_8–A_{14} addresses flow into the device. The addresses, both low- and high-order, are latched when ALE transitions LOW (V_{IL}). $\overline{PSEN}$ will then go LOW and after t_{PLDV}; Valid data is presented on the A/D_0–A/D_7 pins. $\overline{CE}$ must be LOW during the entire operation.

DATA MEMORY MODE

This mode of operation allows both read and write functions. The $\overline{PSEN}$ input is tied to V_{IH} or to V_{CC} through a pull-up resistor. The ALE, $\overline{RD}$, and $\overline{WR}$ inputs are tied directly to the microcontroller ALE, $\overline{RD}$, and $\overline{WR}$ outputs.

Read

This operation is quite similar to the program memory read. A HIGH to LOW transition on ALE latches the addresses and the data will be output on the AD pins after $\overline{RD}$ goes LOW (t_{RLDV}).

Write

A write is performed by latching the addresses on the falling edge of ALE. Then $\overline{WR}$ is strobed LOW followed by valid data being presented at the A/D_0–A/D_7 pins. The data will be latched into the X88257 on the rising edge of $\overline{WR}$. To write to the X88257, a three-byte command sequence must precede the byte(s) being written. (See Software Data Protection.)

MODE SELECTION

$\overline{CE}$	$\overline{PSEN}$	$\overline{RD}$	$\overline{WR}$	Mode	I/O	Power
V_{CC}	X	X	X	Standby	High Z	Standby (CMOS)
HIGH	X	X	X	Standby	High Z	Standby (TTL)
LOW	LOW	HIGH	HIGH	Read	D_{OUT}	Active
LOW	HIGH	LOW	HIGH	Read	D_{OUT}	Active
LOW	HIGH	HIGH	⌐	Write	D_{IN}	Active

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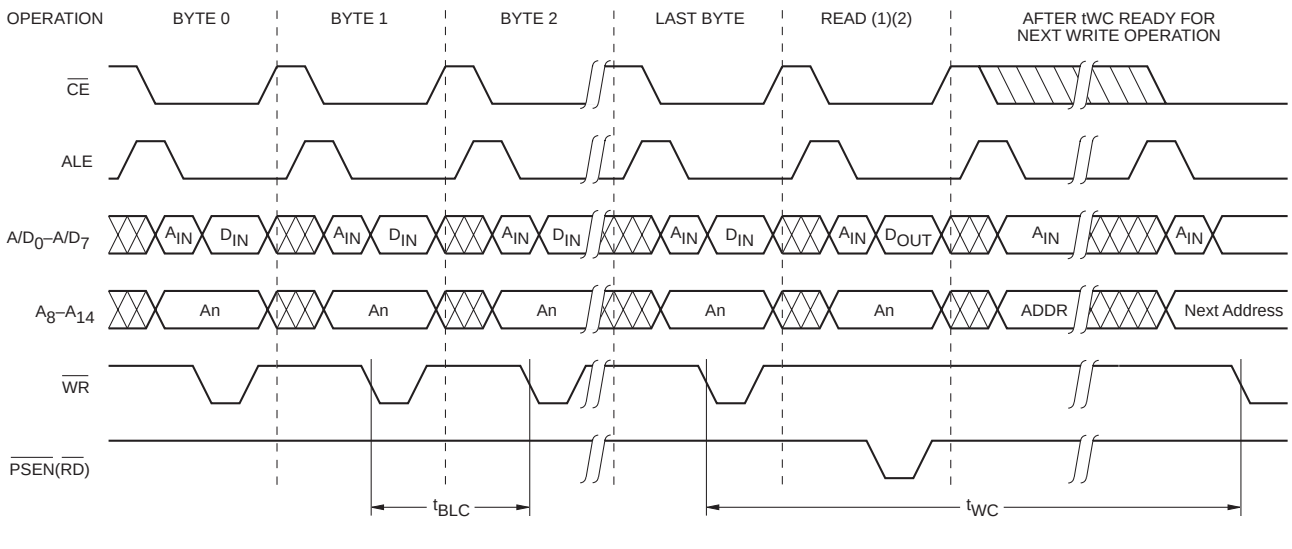
PAGE WRITE OPERATION

Regardless of the microcontroller employed, the X88257 supports page mode write operations. This allows the microcontroller to write from 1 to 128 bytes of data to the X88257. Each individual write within a page write operation must conform to the byte write timing requirements.

The falling edge of $\overline{WR}$ starts a timer delaying the internal programming cycle 100µs. Therefore, each successive write operation must begin within 100µs of the last byte written. The following waveforms illustrate the sequence and timing requirements.

Page Write Timing Sequence for $\overline{WR}$ Controlled Operation

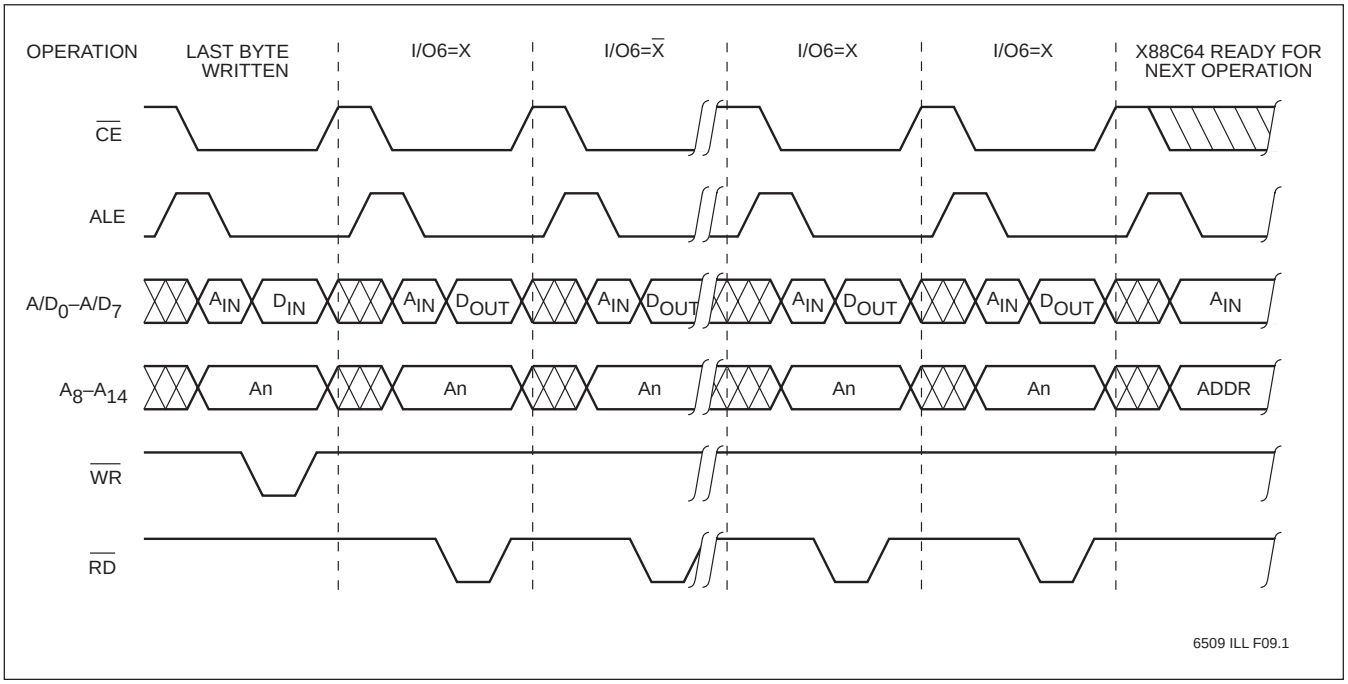


Notes: (1) For each successive write within a page write cycle A_7–A_{14} must be the same.

TOGGLE BIT POLLING

Because the typical write timing is less than the specified 5ms, Toggle Bit Polling has been provided to determine the early end of write. During the internal programming cycle I/O_6 will toggle from “1” to “0” and “0” to “1” on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

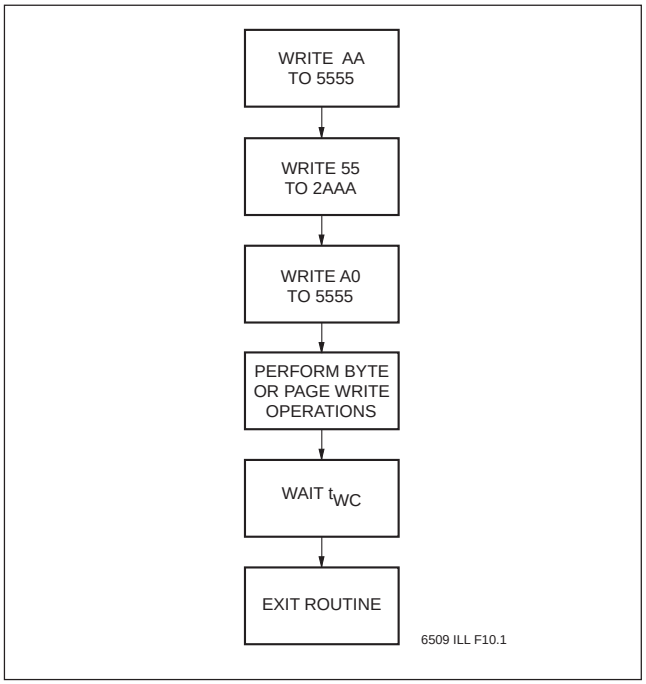
Toggle Bit Polling $\overline{RD}/\overline{WR}$ Control



SOFTWARE DATA PROTECTION

Software Data Protection (SDP) is employed to protect the entire array against inadvertent writes. To write to the X88257, a three-byte command sequence must precede the byte(s) being written. All write operations, both the command sequence and any data write operations must conform to the page write timing requirements.

Writing with SDP



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X88257	5V ±10%

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D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		60	mA	$\overline{CE}$ = $\overline{RD}$ = V_{IL}, All I/O's = Open,Other Inputs = V_{CC}
$I_{SB1(CMOS)}$	V_{CC} Current (Standby)		500	µA	$\overline{CE}$ = V_{CC} – 0.3V, All I/O's = Open,Other Inputs = V_{CC} – 0.3V, ALE = V_{IL}
$I_{SB2(TTL)}$	V_{CC} Current (Standby)		6	mA	$\overline{CE}$ = V_{IH}, All I/O's = Open, Other Inputs = V_{IH}, ALE = V_{IL}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{RD}$ = V_{IH} = $\overline{PSEN}$
V_{IL}(3)	Input LOW Voltage	–1	0.8	V	
V_{IH}(3)	Input HIGH Voltage	2	V_{CC} + 0.5	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance	6	pF	V_{IN} = 0V

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POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(4)	Power-Up to Read	1	ms
t_{PUW}(4)	Power-Up to Write	5	ms

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Notes: (3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

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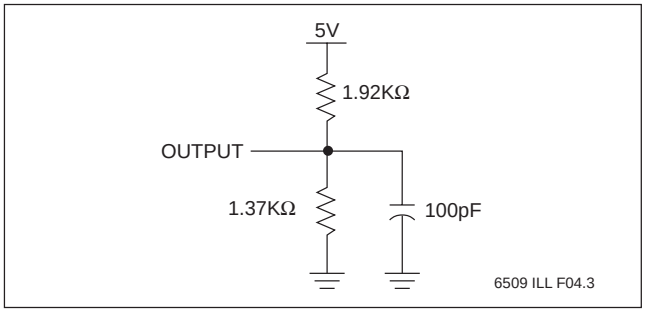
EQUIVALENT A.C. TEST CIRCUIT



A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

$\overline{PSEN}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{PLDV}	$\overline{PSEN}$ Read Access Time		120	ns
t_{PHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{PL}	$\overline{PSEN}$ Pulse Width	150		ns
t_{PS}	$\overline{PSEN}$ Setup Time	30		ns
t_{PH}	$\overline{PSEN}$ Hold Time	20		ns
t_{PHDZ} (5)	$\overline{PSEN}$ Disable to Output in High Z		50	ns
t_{PLDX} (5)	$\overline{PSEN}$ to Output in Low Z	10		ns

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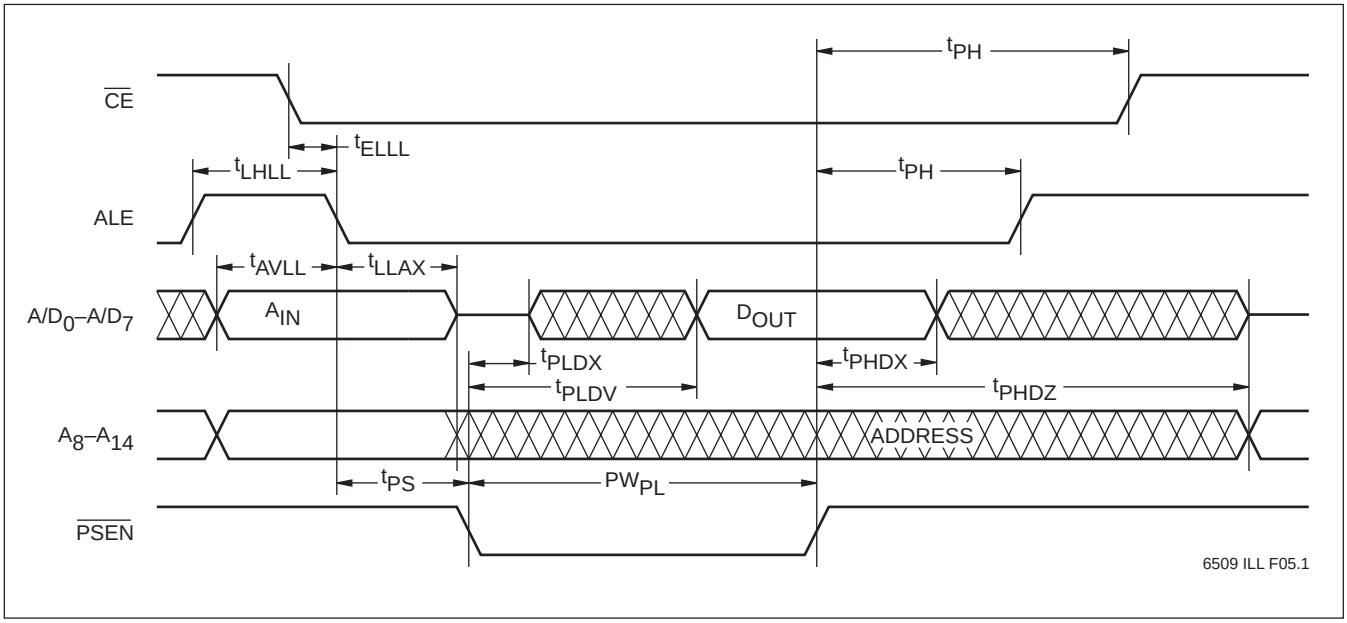
$\overline{PSEN}$ Controlled Read Timing Diagram



Note: (5) This parameter is periodically sampled and not 100% tested.

$\overline{RD}$ Controlled Read Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{RLDV}	$\overline{RD}$ Read Access Time		120	ns
t_{RHDX}	Data Hold Time	0		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
PW_{RL}	$\overline{RD}$ Pulse Width	150		ns
t_{RDS}	$\overline{RD}$ Setup Time	30		ns
t_{RDH}	$\overline{RD}$ Hold Time	20		ns
t_{RHDZ} (6)	$\overline{RD}$ Disable to Output in High Z		50	ns
t_{RLDX} (6)	$\overline{RD}$ to Output in Low Z	0		ns

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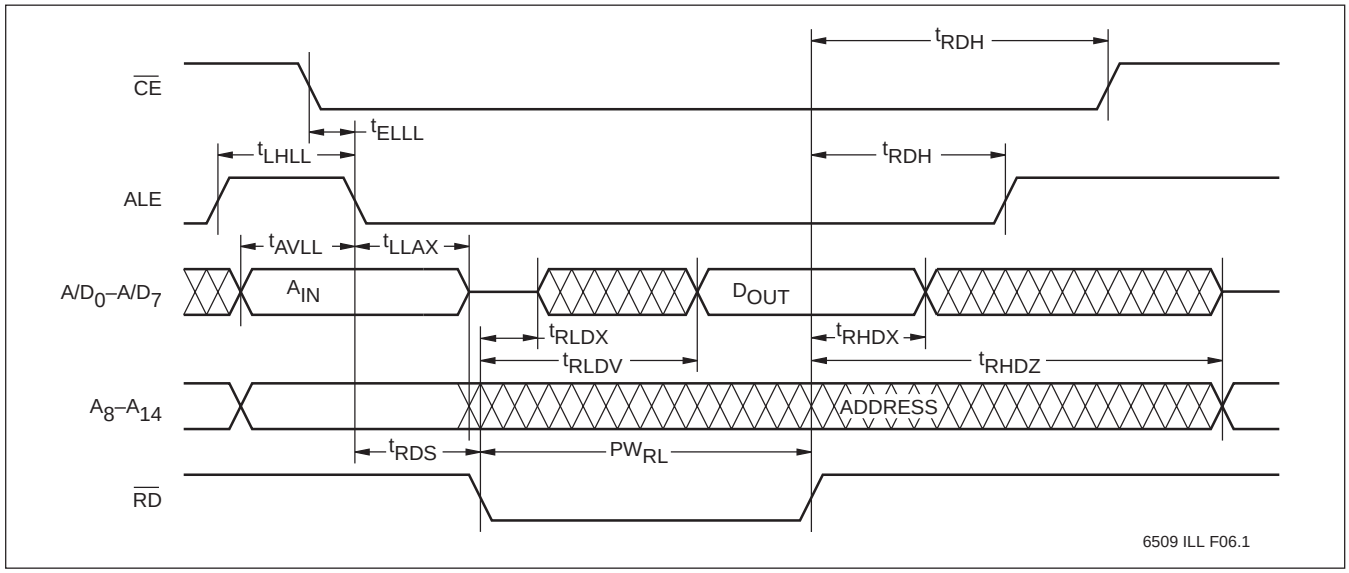
$\overline{RD}$ Controlled Read Timing Diagram



Note: (6) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

$\overline{WR}$ Controlled Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{LHLL}	ALE Pulse Width	80		ns
t_{AVLL}	Address Setup Time	20		ns
t_{LLAX}	Address Hold Time	30		ns
t_{DVWH}	Data Setup Time	50		ns
t_{WHDX}	Data Hold Time	30		ns
t_{ELLL}	Chip Enable Setup Time	7		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	120		ns
t_{WRS}	$\overline{WR}$ Setup Time	30		ns
t_{WRH}	$\overline{WR}$ Hold Time	20		ns
t_{BLC}	Byte Load Time (Page Write)	0.5	100	µs
t_{WC} (7)	Write Cycle Time		5	ms

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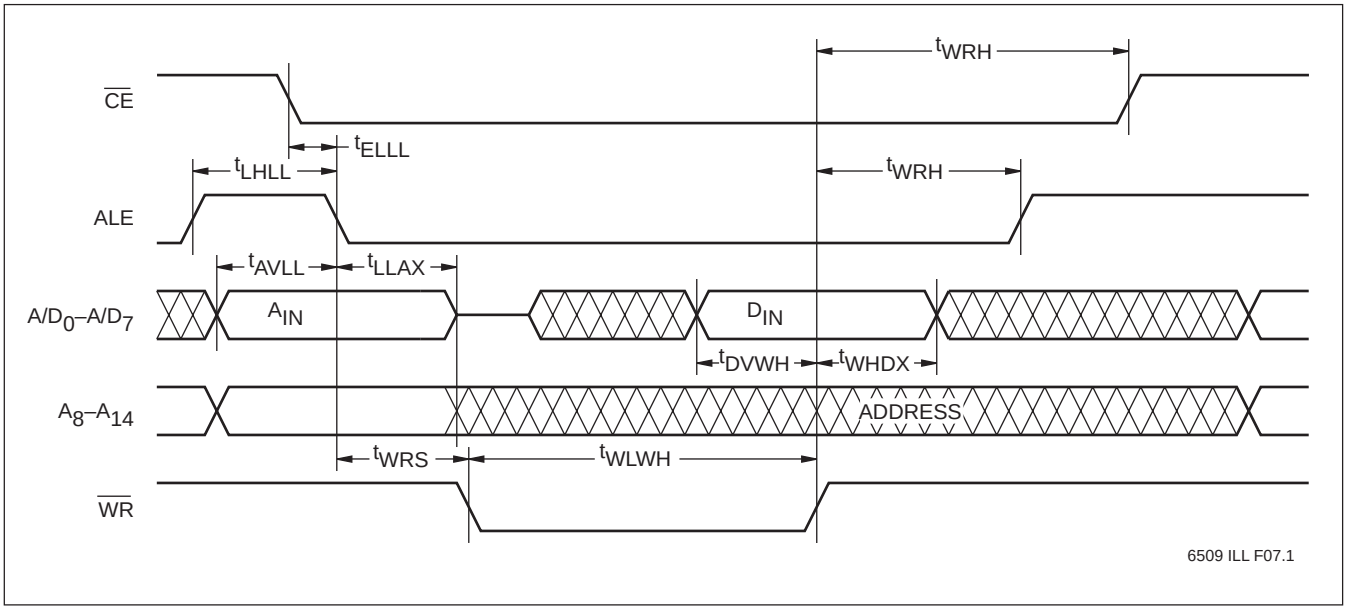
$\overline{WR}$ Controlled Write Timing Diagram



Note: (7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

NOTES

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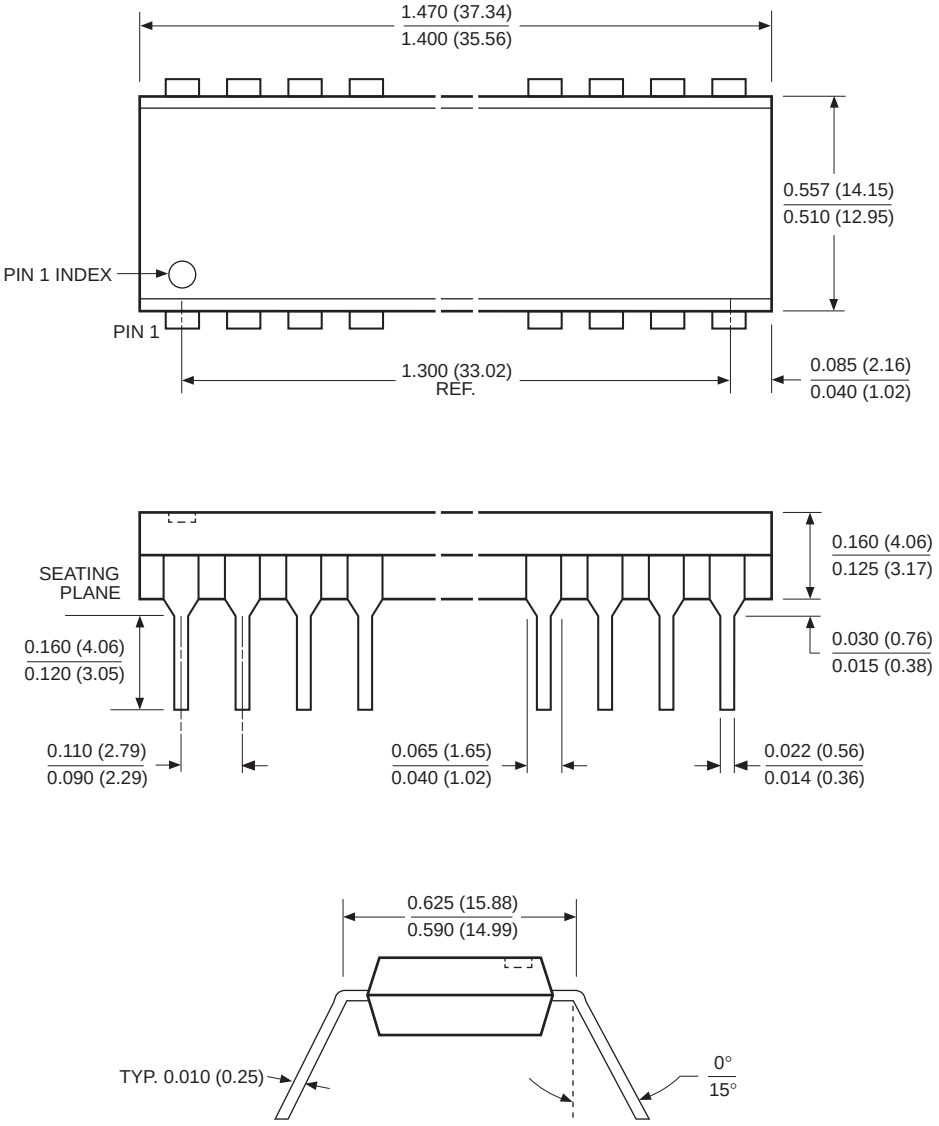
PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



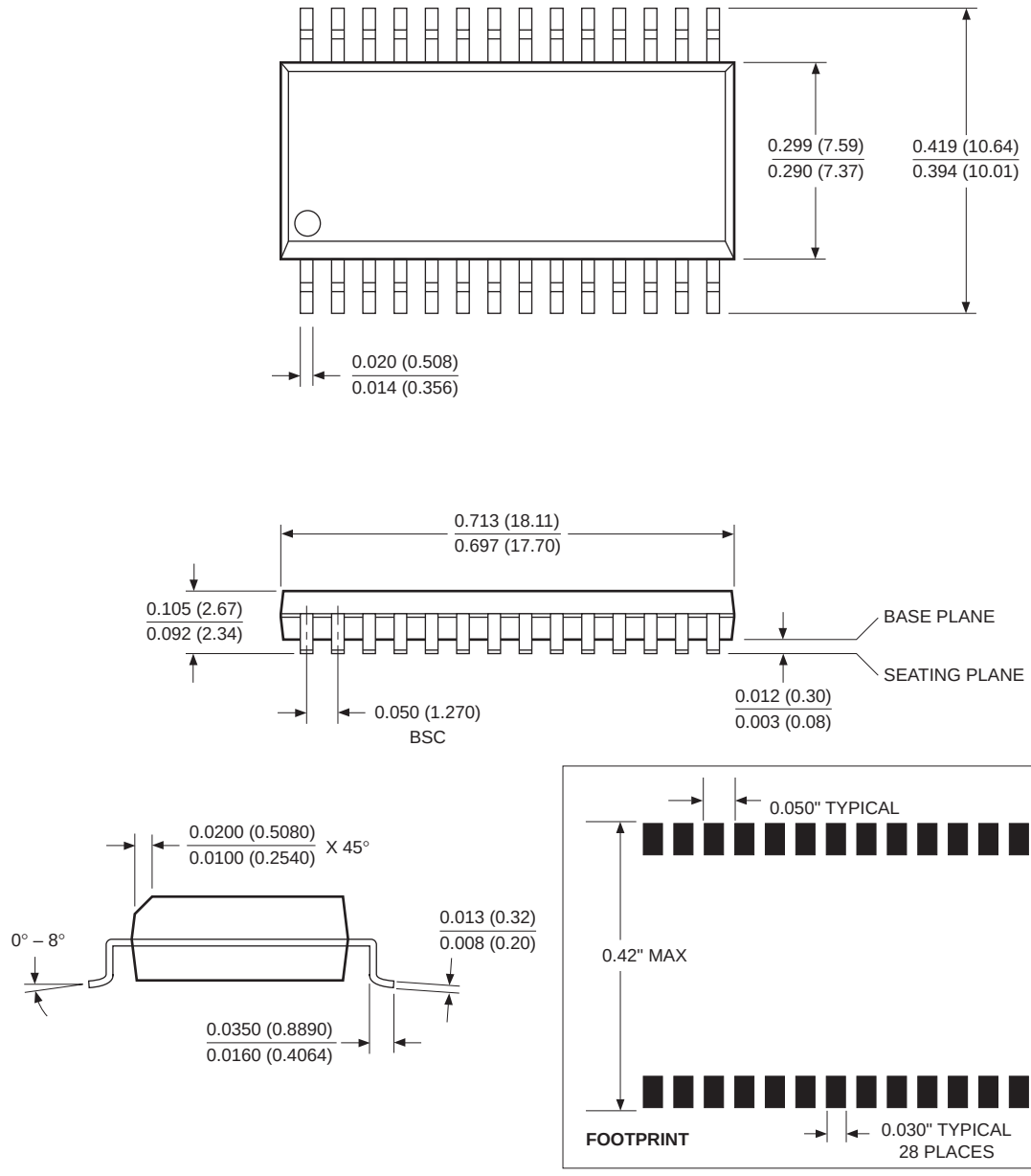
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F04

PACKAGING INFORMATION

28-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTES:

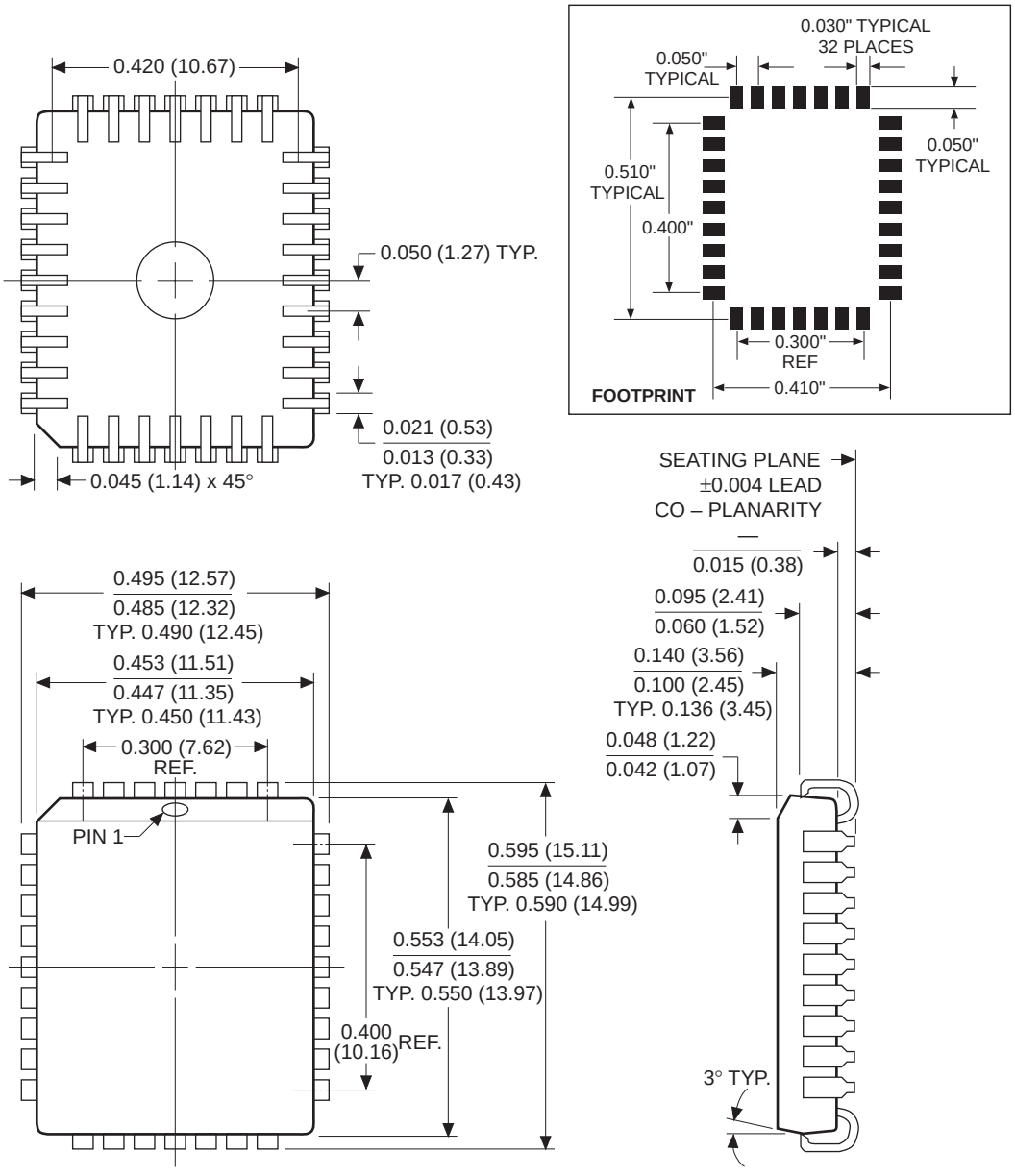
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

3926 FHD F17

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



NOTES:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

3926 FHD F13

ORDERING INFORMATION