

NP100N04NUJ

MOS FIELD EFFECT TRANSISTOR

R07DS0364EJ0100

Rev.1.00

Jun 13, 2011

Description

The NP100N04NUJ is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
— $R_{DS(on)} = 3.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$)
- Low C_{iss} : $C_{iss} = 5600 \text{ pF TYP.}$ ($V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$)
- High current rating: $I_{D(DC)} = \pm 100 \text{ A}$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing	Package
NP100N04NUJ-S18-AY *1	Pure Sn (Tin)	Tube 50 p/tube	TO-262 (MP-25SK) TYP. 1.8g

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	40	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 100	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 400	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	220	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.8	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +175$	$^\circ\text{C}$
Repetitive Avalanche Current *2	I_{AR}	60	A
Repetitive Avalanche Energy *2	E_{AR}	360	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	0.68	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

Notes: *1. $T_C = 25^\circ\text{C}$, $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

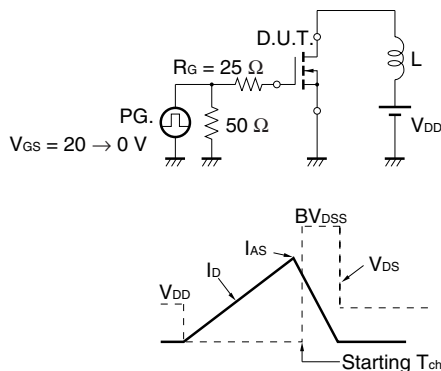
*2. $T_{ch(peak)} \leq 150^\circ\text{C}$, $R_G = 25 \Omega$

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

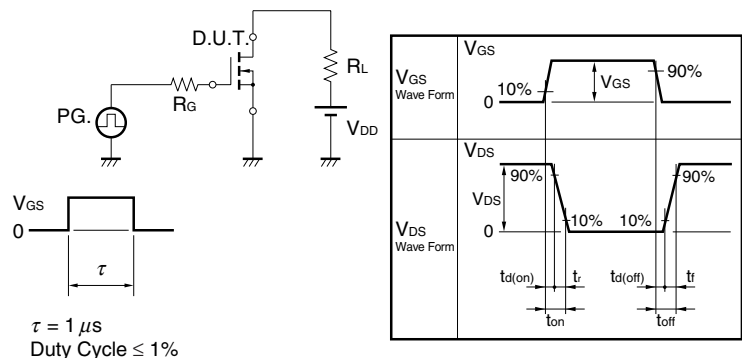
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1.0	μA	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$
Gate Leakage Current	I_{GSS}			± 100	nA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$
Forward Transfer Admittance ^{*1}	$ y_{fs} $	45	87		S	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$
Drain to Source On-state Resistance ^{*1}	$R_{DS(on)}$		2.5	3.0	m Ω	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$
Input Capacitance	C_{iss}		5600	8400	pF	$V_{DS} = 25\text{ V},$ $V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		920	1380	pF	
Reverse Transfer Capacitance	C_{rss}		340	620	pF	
Turn-on Delay Time	$t_{d(on)}$		25	60	ns	$V_{DD} = 20\text{ V}, I_D = 50\text{ A},$ $V_{GS} = 10\text{ V},$ $R_G = 0\text{ }\Omega$
Rise Time	t_r		15	40	ns	
Turn-off Delay Time	$t_{d(off)}$		93	190	ns	
Fall Time	t_f		13	40	ns	$V_{DD} = 32\text{ V},$ $V_{GS} = 10\text{ V},$ $I_D = 100\text{ A}$
Total Gate Charge	Q_G		110	170	nC	
Gate to Source Charge	Q_{GS}		22		nC	
Gate to Drain Charge	Q_{GD}		32		nC	$I_F = 100\text{ A}, V_{GS} = 0\text{ V}$
Body Diode Forward Voltage ^{*1}	$V_{F(S-D)}$		0.9	1.5	V	
Reverse Recovery Time	t_{rr}		55		ns	
Reverse Recovery Charge	Q_{rr}		77		nC	$di/dt = 100\text{ A}/\mu\text{s}$

Note: *1. Pulsed test

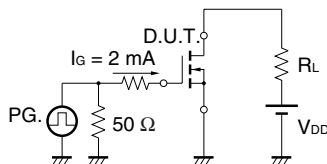
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

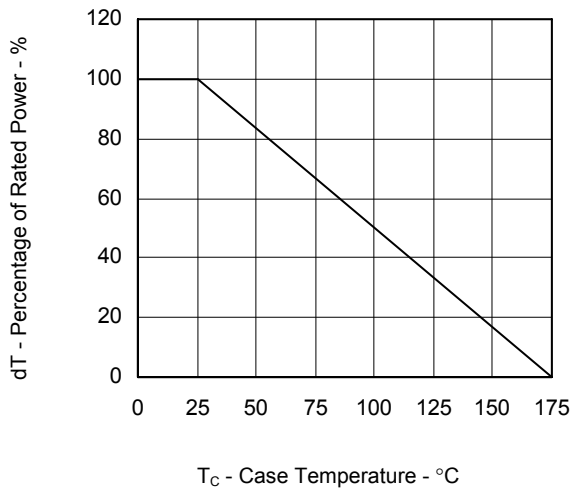


TEST CIRCUIT 3 GATE CHARGE

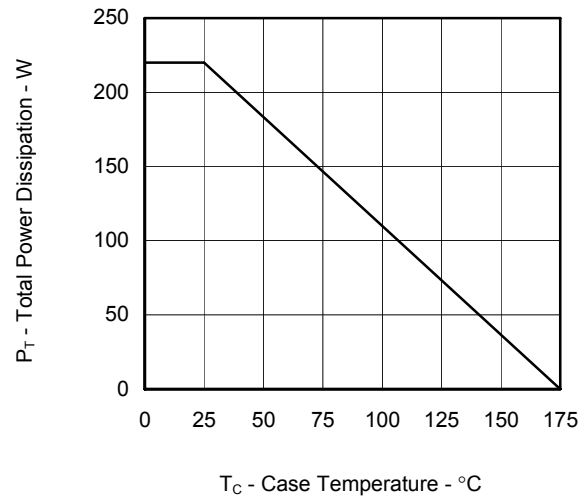


Typical Characteristics ($T_A = 25^\circ\text{C}$)

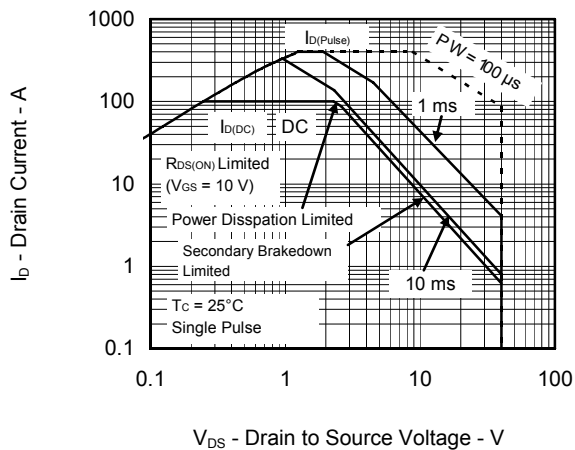
DERATING FACTOR OF FORWARD BIAS SAFE
OPERATING AREA



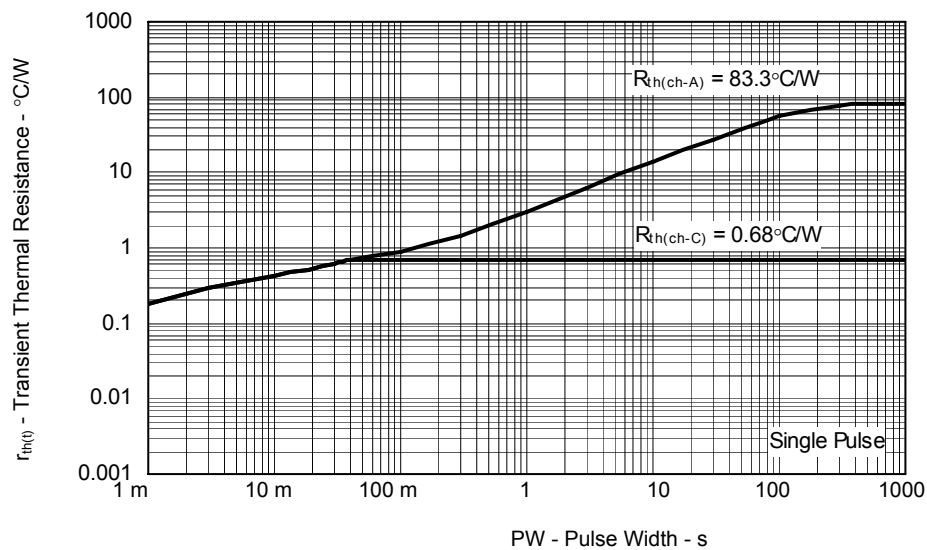
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE

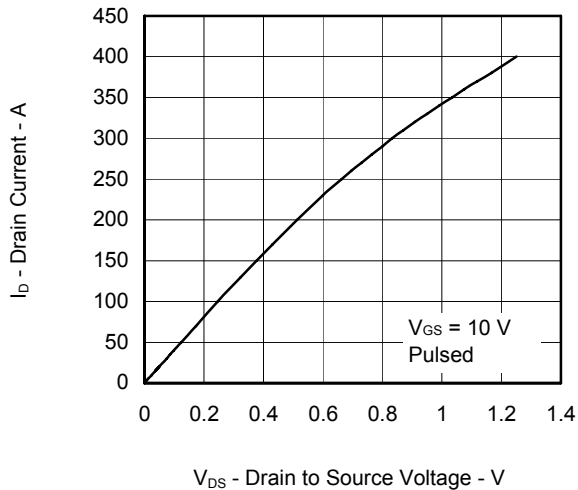


FORWARD BIAS SAFE OPERATING AREA

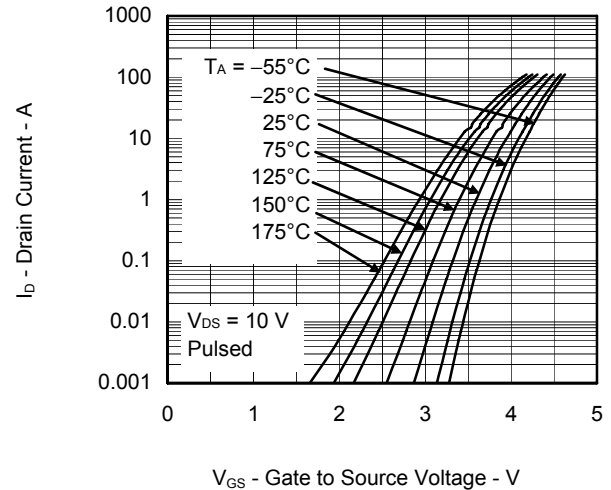
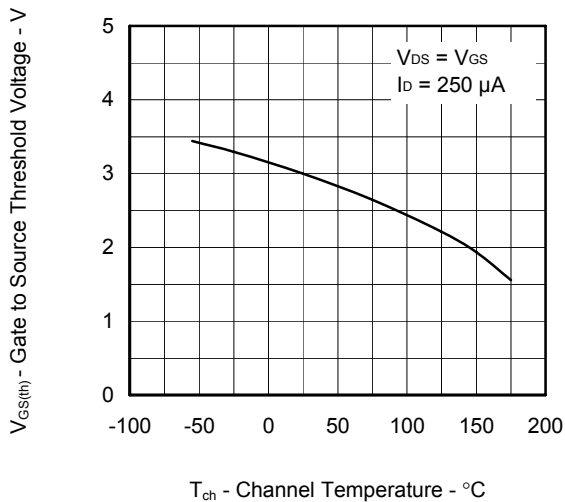
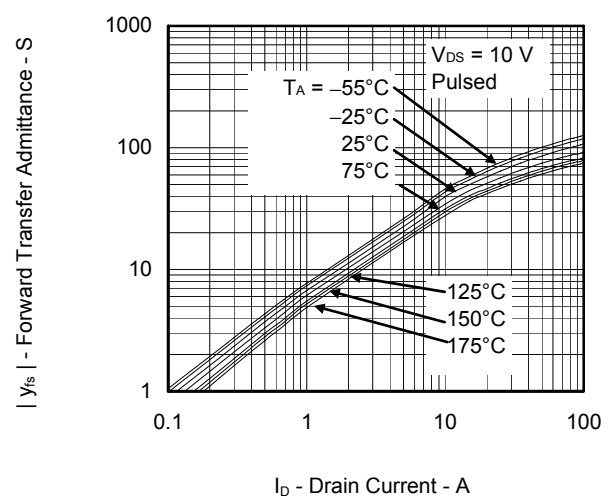
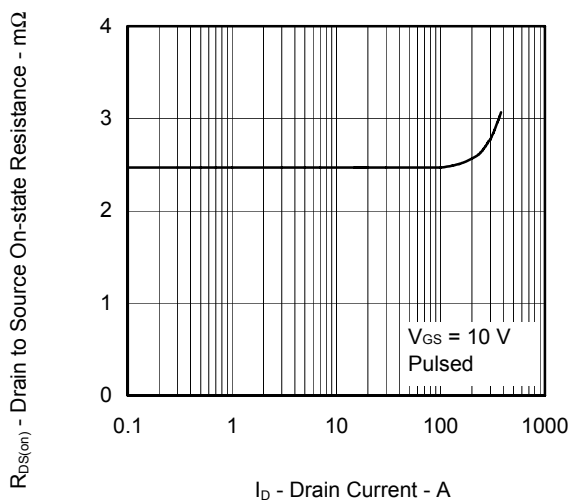
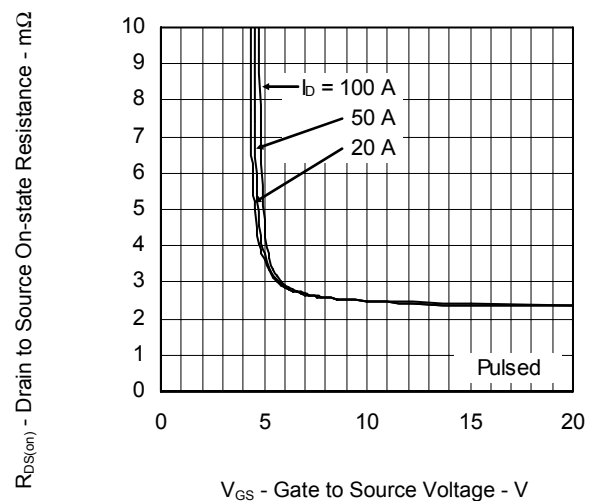


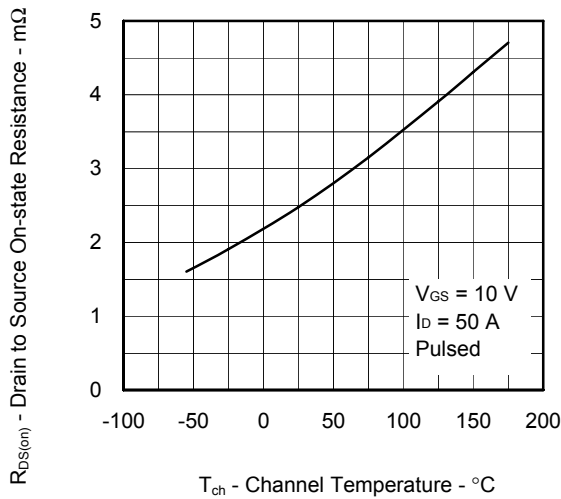
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



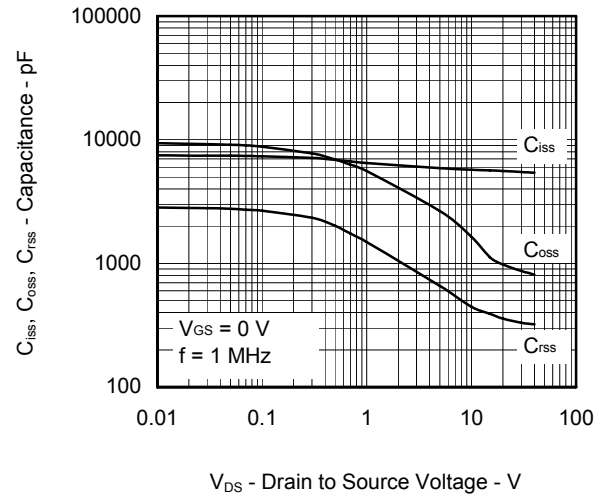
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

FORWARD TRANSFER CHARACTERISTICS

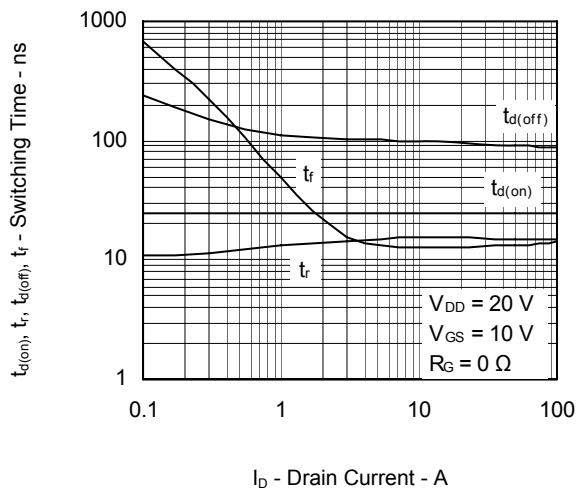
GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATUREFORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE

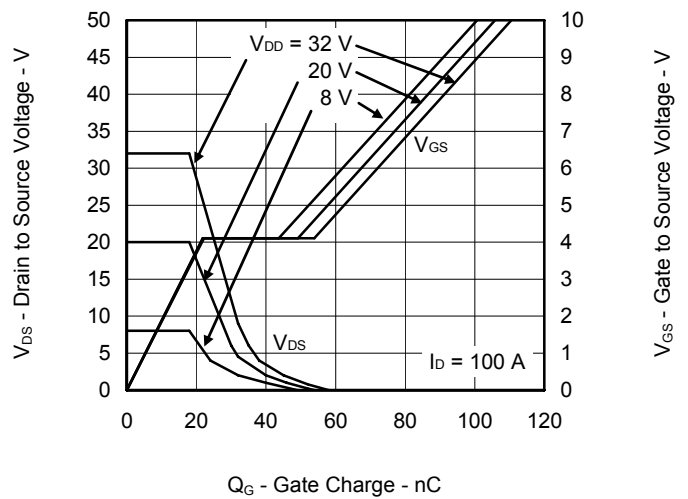
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



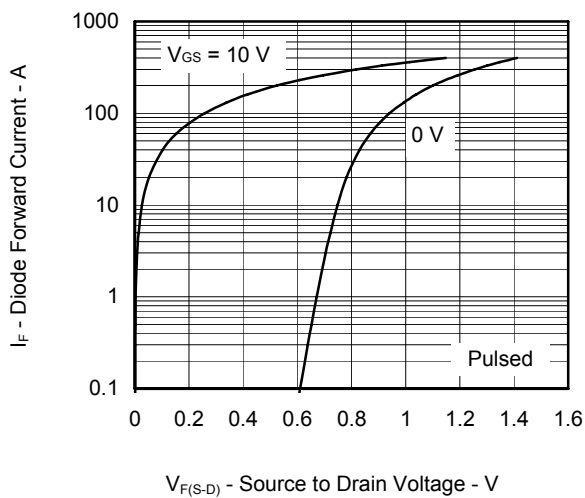
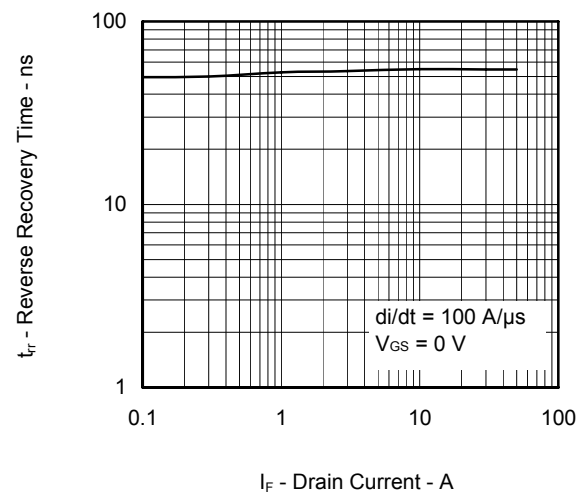
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

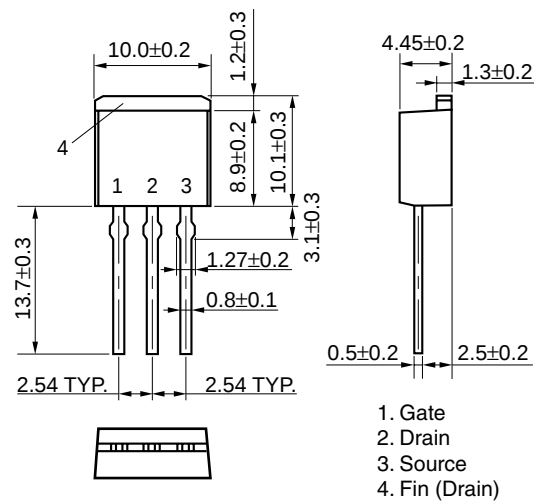


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

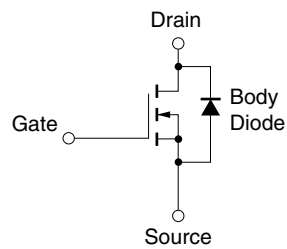
REVERSE RECOVERY TIME vs.
DRAIN CURRENT

Package Drawings (Unit: mm)

TO-262 (MP-25SK)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	NP100N04NUJ Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jun 13, 2011	–	First Edition Issued

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