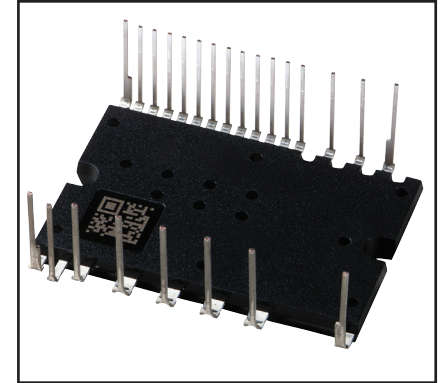
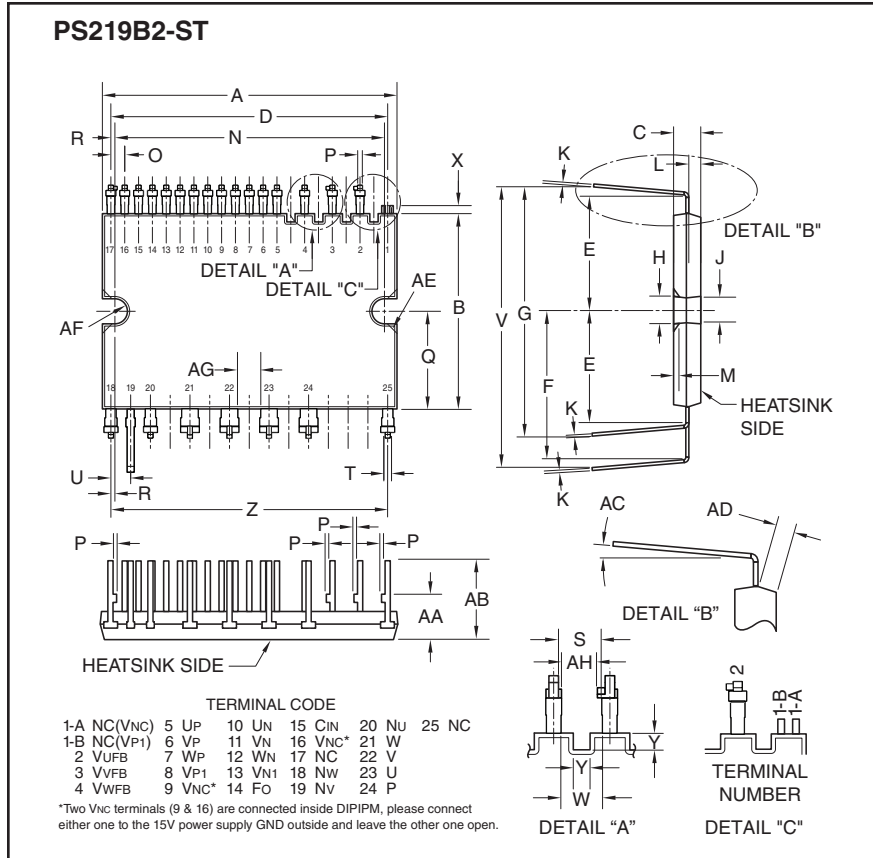


### Intellimod™ Module Dual-In-Line Intelligent Power Module 5 Amperes/600 Volts



#### Description:

DIP-IPMs are intelligent power modules that integrate power devices, drivers, and protection circuitry in an ultra compact dual-in-line transfer-mold package for use in driving small three phase motors. Use of 6th generation CSTBT IGBTs, DIP packaging, and application specific HVICs allow the designer to reduce inverter size and overall design time.

#### Features:

- Compact Packages
- Single Power Supply
- Integrated HVICs
- Direct Connection to CPU
- Over-temperature Protection

#### Applications:

- Small Servo Motors
- Small Motor Control

#### Ordering Information:

PS219B2-ST is a 600V, 5 Ampere short pin DIP Intelligent Power Module.

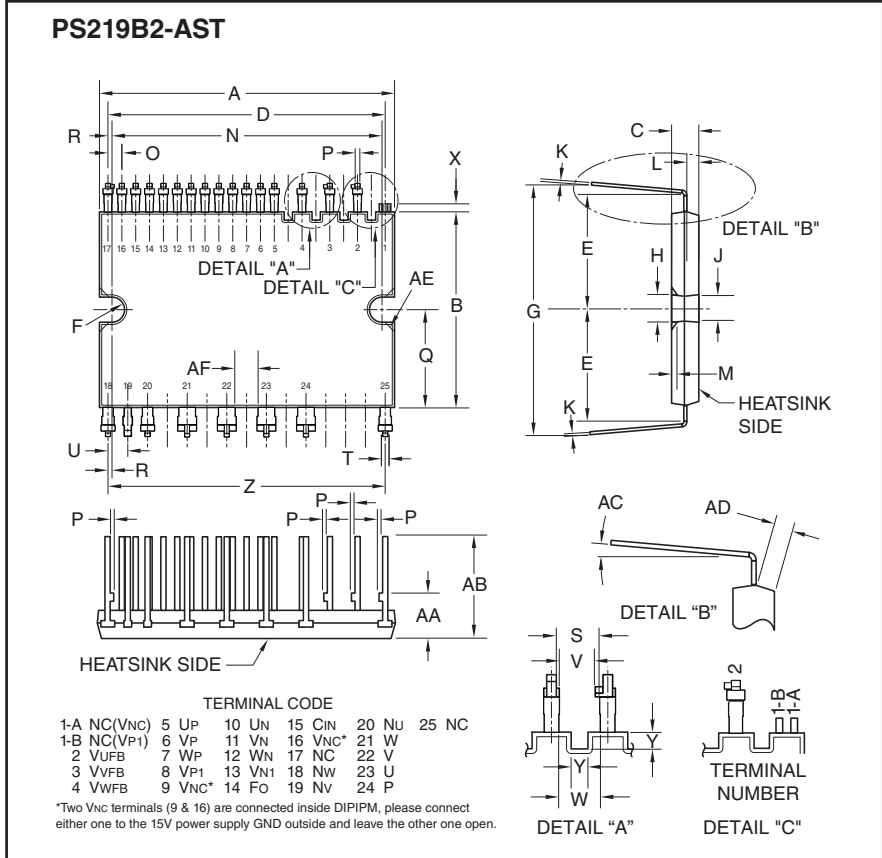
PS219B2-AST – long pin type  
PS219B2-CST – zigzag pin type

#### Outline Drawing and Circuit Diagram

Dim.	Inches	Millimeters
A	1.50±0.02	38.0±0.5
B	0.94±0.02	24.0±0.5
C	0.14	3.5
D	1.40	35.56
E	0.57±0.02	14.4±0.5
F	0.74±0.02	18.9±0.5
G	1.15±0.02	29.2±0.5
H	0.14	3.5
J	0.13	3.3
K	0.016	0.4
L	0.06±0.02	1.5±0.05
M	0.031	0.8
N	1.38±0.019	35.0±0.3
O	0.07±0.008	1.778±0.2
P	0.02	0.5
Q	0.47	12.0
R	0.011	0.28

Dim.	Inches	Millimeters
S	0.1046	2.656
T	0.024	0.6
U	0.1±0.008	2.54±0.2
V	1.33±0.02	33.7±0.5
W	0.1085	2.756
X	0.04	1.0
Y	0.05	1.2
Z	1.40	35.56
AA	0.22±0.02	5.5±0.5
AB	0.37±0.02	9.5±0.5
AC	0 ~ 5°	0 ~ 5°
AD	0.06 Min.	1.5 Min.
AE	0.05	1.2
AF	0.063 Rad.	1.6 Rad.
AG	0.118 Min.	3.0 Min.
AH	0.098 Min.	2.5 Min.

**PS219B2-ST, PS219B2-AST, PS219B2-CST**  
**Intellimod™ Module**  
**Dual-In-Line Intelligent Power Module**  
 5 Amperes/600 Volts

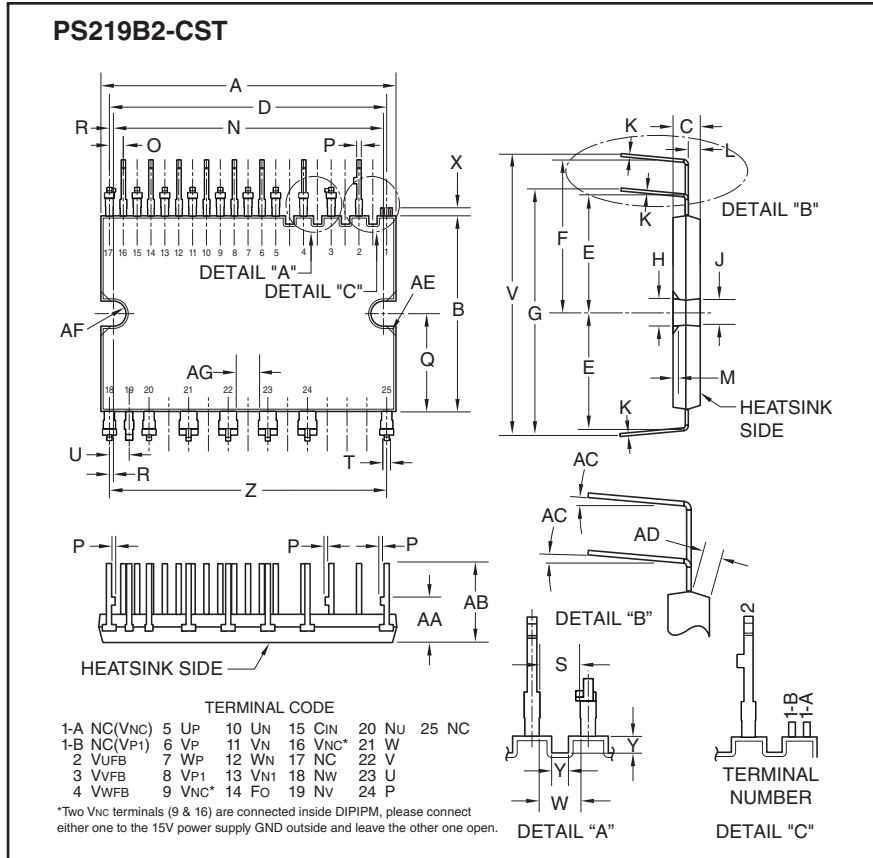


**Outline Drawing and Circuit Diagram**

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G	1.16±0.02	29.4±0.5
H	0.14	3.5
J	0.13	3.3
K	0.016	0.4
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AB	0.55±0.02	14.0±0.5
AC	0 ~ 5°	0 ~ 5°
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AE	0.05	1.2
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**PS219B2-ST, PS219B2-AST, PS219B2-CST**  
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 5 Amperes/600 Volts



**Outline Drawing and Circuit Diagram**

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**PS219B2-ST, PS219B2-AST, PS219B2-CST**  
**Intellimod™ Module**  
**Dual-In-Line Intelligent Power Module**  
 5 Amperes/600 Volts

## Absolute Maximum Ratings, $T_j = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	PS219B2-ST, PS219B2-AST, PS219B2-CST	Units
<b>Inverter Part</b>			
Supply Voltage (Applied between P-NU, NV, NW)	$V_{CC}$	450	Volts
Supply Voltage, Surge (Applied between P-NU, NV, NW)	$V_{CC(\text{surge})}$	500	Volts
Collector-Emitter Voltage	$V_{CES}$	600	Volts
Each IGBT Collector Current ( $T_C = 25^\circ\text{C}$ )	$\pm I_C$	5	Amperes
Each Peak Collector Current ( $T_C = 25^\circ\text{C}$ , Less than 1ms)	$\pm I_{CP}$	10	Amperes
Collector Dissipation ( $T_C = 25^\circ\text{C}$ , per 1 Chip)	$P_C$	21.3	Watts
Power Device Junction Temperature*1	$T_j$	-20 ~ +150	$^\circ\text{C}$

## Control (Protection) Part

Control Supply Voltage (Applied between $V_{P1-V_{NC}}$ , $V_{N1-V_{NC}}$ )	$V_D$	20	Volts
Control Supply Voltage (Applied between $V_{UFB-U}$ , $V_{VFB-V}$ , $V_{WFB-W}$ )	$V_{DB}$	20	Volts
Input Voltage (Applied between $U_P$ , $V_P$ , $W_P-V_{NC}$ , $U_N$ , $V_N$ , $W_N-V_{NC}$ )	$V_{IN}$	-0.5 ~ $V_D+0.5$	Volts
Fault Output Supply Voltage (Applied between $F_O-V_{NC}$ )	$V_{FO}$	-0.5 ~ $V_D+0.5$	Volts
Fault Output Current (Sink Current at $F_O$ Terminal)	$I_{FO}$	1	mA
Current Sensing Input Voltage (Applied between $C_{IN-V_{NC}}$ )	$V_{SC}$	-0.5 ~ $V_D+0.5$	Volts

## Total System

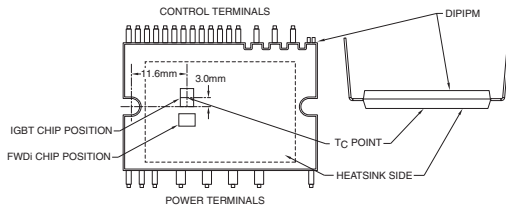
Self-protection Supply Voltage Limit, Short Circuit Protection Capability ( $V_D = 13.5 \sim 16.5\text{V}$ , Inverter Part, $T_j = 125^\circ\text{C}$ , Non-repetitive less than $2\mu\text{s}$ )	$V_{CC(\text{prot.})}$	400	Volts
Module Case Operating Temperature*2	$T_C$	-20 ~ +100	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-40 ~ +125	$^\circ\text{C}$
Isolation Voltage, 60Hz, Sinusoidal 1 Minute, All Connected Pins to Heatsink Plate	$V_{ISO}$	1500	$V_{rms}$

## Thermal Resistance

Junction to Case*3	$R_{th(j-c)Q}$	Inverter IGBT Part (Per 1/6 Module)	—	—	4.7	$^\circ\text{C/Watt}$
	$R_{th(j-c)D}$	Inverter FWDi Part (Per 1/6 Module)	—	—	5.4	$^\circ\text{C/Watt}$

\*1 The maximum junction temperature rating of the power chips integrated within the DIPIPM is  $150^\circ\text{C}$  ( $@T_C \leq 100^\circ\text{C}$ ). However, to ensure safe operation of the DIPIPM, the average junction temperature should be limited to  $T_{j(\text{avg})} \leq 25^\circ\text{C}$  ( $@T_C \leq 100^\circ\text{C}$ ).

\*2 TC measurement point



\*3 Good thermal grease with long-term quality should be applied evenly with  $+100\mu\text{m} \sim +200\mu\text{m}$  on the contacting surface of the DIPIPM and heatsink. The contacting thermal resistance between DIPIPM case and heatsink ( $R_{th(c-f)}$ ) is determined by the thickness and the thermal conductivity of the applied grease. For reference,  $R_{th(c-f)}$  (per 1/6 module) is about  $0.3^\circ\text{C/W}$  when the grease thickness is  $20\mu\text{m}$  and the thermal conductivity is  $1.0\text{W/mK}$ .

**PS219B2-ST, PS219B2-AST, PS219B2-CST**  
**Intellimod™ Module**  
**Dual-In-Line Intelligent Power Module**  
**5 Amperes/600 Volts**

**Electrical and Mechanical Characteristics,  $T_j = 25^\circ\text{C}$  unless otherwise specified**

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units	
<b>Inverter Part</b>							
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$V_D = V_{DB} = 15\text{V}, I_C = 5\text{A}, V_{IN} = 5\text{V}, T_j = 25^\circ\text{C}$	—	1.50	2.00	Volts	
		$V_D = V_{DB} = 15\text{V}, I_C = 5\text{A}, V_{IN} = 5\text{V}, T_j = 125^\circ\text{C}$	—	1.60	2.10	Volts	
Diode Forward Voltage	$V_{EC}$	$-I_C = 5\text{A}, V_{IN} = 0\text{V}$	—	1.70	2.20	Volts	
Switching Times	$t_{on}$		0.75	1.35	1.95	$\mu\text{s}$	
	$t_{rr}$	$V_{CC} = 300\text{V}, V_D = V_{DB} = 15\text{V},$	—	0.30	—	$\mu\text{s}$	
	$t_{C(on)}$	$I_C = 5\text{A}, T_j = 125^\circ\text{C},$	—	0.35	0.55	$\mu\text{s}$	
	$t_{off}$	$V_{IN} = 0 \leftrightarrow 5\text{V}, \text{Inductive Load}$	—	1.40	2.00	$\mu\text{s}$	
	$t_{C(off)}$		—	0.30	0.60	$\mu\text{s}$	
Collector-Emitter Cutoff Current	$I_{CES}$	$V_{CE} = V_{CES}, T_j = 25^\circ\text{C}$	—	—	1.0	mA	
		$V_{CE} = V_{CES}, T_j = 125^\circ\text{C}$	—	—	10	mA	
<b>Control (Protection) Part</b>							
Circuit Current	$I_D$	$V_{IN} = 0\text{V}, V_D = 15\text{V}$	Total of $V_{P1}-V_{NC}, V_{N1}-V_{NC}$	—	—	2.80	mA
		$V_{IN} = 5\text{V}, V_D = 15\text{V}$	Total of $V_{P1}-V_{NC}, V_{N1}-V_{NC}$	—	—	2.80	mA
	$I_{DB}$	$V_{IN} = 0\text{V}, V_D = V_{DB} = 15\text{V}$	Each Part of $V_{UFB-U}, V_{VFB-V}, V_{WFB-W}$	—	—	0.10	mA
		$V_{IN} = 5\text{V}, V_D = V_{DB} = 15\text{V}$	Each Part of $V_{UFB-U}, V_{VFB-V}, V_{WFB-W}$	—	—	0.10	mA
Fault Output Voltage	$V_{FOH}$	$V_{SC} = 0\text{V}, F_O$ Terminal Pull-up to 5V by 10k $\Omega$	4.9	—	—	Volts	
	$V_{FOL}$	$V_{SC} = 1\text{V}, I_{FO} = 1\text{mA}$	—	—	0.95	Volts	
Input Current	$I_{IN}$	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA	
Short Circuit Trip Level	$V_{SC(ref)}$	$V_D = 15\text{V}^{*4}$	0.43	0.48	0.53	Volts	
Over-Temperature Protection ( $V_D = 15\text{V}$ , At Temperature of LVIC) <sup>*6</sup>	$OT_t$	Trip Level	100	120	140	$^\circ\text{C}$	
	$OT_{rh}$	Trip/Reset Hysteresis	—	10	—	$^\circ\text{C}$	
Control Supply	$UV_{DBt}$	Trip Level, $T_j \leq 125^\circ\text{C}$	7.0	10.0	12.0	Volts	
Under-voltage Protection	$UV_{DBr}$	Reset Level, $T_j \leq 125^\circ\text{C}$	7.0	10.0	12.0	Volts	
	$UV_{Dt}$	Trip Level, $T_j \leq 125^\circ\text{C}$	10.3	—	12.5	Volts	
	$UV_{Dr}$	Reset Level, $T_j \leq 125^\circ\text{C}$	10.8	—	13.0	Volts	
Fault Output Pulse Width <sup>*5</sup>	$t_{FO}$		20	—	—	$\mu\text{s}$	
ON Threshold Voltage	$V_{th(on)}$	Applied between	—	2.1	2.6	Volts	
OFF Threshold Voltage	$V_{th(off)}$	$U_P, V_P, W_P-V_{NC},$	0.8	1.3	—	Volts	
ON/OFF Threshold Hysteresis Voltage	$V_{th(hys)}$	$U_N, V_N, W_N-V_{NC}$	0.35	0.65	—	Volts	
Bootstrap Diode Forward Voltage <sup>*7</sup>	$V_F$	$I_F = 10\text{mA},$	1.1	1.7	2.3	Volts	
		Including Voltage Drop by Limiting Resistor					
Built-in Limiting Resistance	R	For Bootstrap Circuit	80	100	120	$\Omega$	

\*4 Short Circuit protection is functioning only for N-side IGBTs. Please select the value of the external shunt resistor such that the  $S_C$  trip level is less than 1.7 times the current rating.

\*5 Fault signal,  $F_O$ , outputs when SC or UV protection works.  $F_O$  pulse width is different for each protection mode. At SC failure,  $F_O$  pulse width is a fixed width (=min. 20 $\mu\text{s}$ ), however, at UV failure,  $F_O$  outputs continuously until recovering from UV state. Minimum  $F_O$  pulse width is 20 $\mu\text{s}$ .

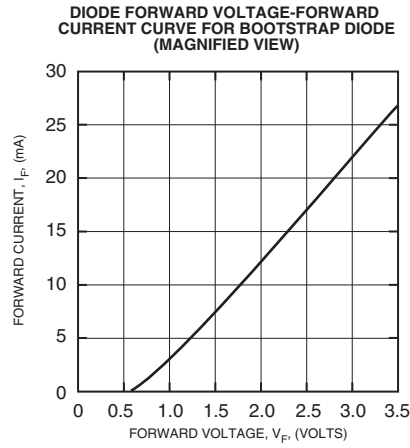
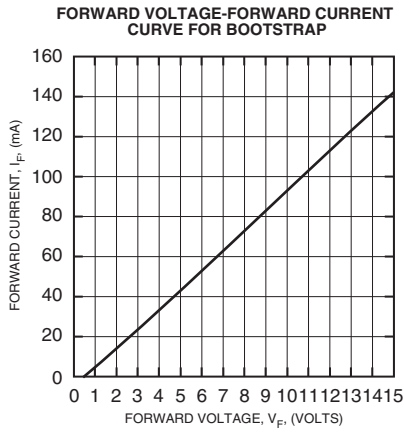
\*6 When the LVIC temperature exceeds OT trip temperature level ( $OT_t$ ), OT protection works and  $F_O$  outputs. In that case if the heatsink dropped off or is loosely fitted, do not use the DIIPM. There is a possibility that the junction temperature of the power chips has exceeded maximum  $T_j$  (150 $^\circ\text{C}$ ).

PS219B2-ST, PS219B2-AST, PS219B2-CST  
**Intellimod™ Module**  
**Dual-In-Line Intelligent Power Module**  
 5 Amperes/600 Volts

## Mechanical Characteristics and Ratings

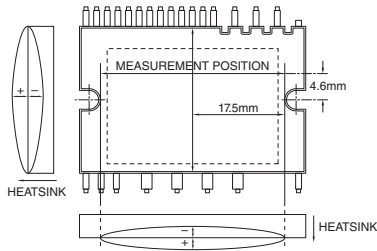
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Units
Mounting Torque		M3 Mounting Screws*8	5.2	6.1	6.9	in-lb
Terminal Pulling Strength		Control Terminal: Weight 4.9N Power Terminal: Weight 9.8N	10	—	—	s
Terminal Bending Strength		Control Terminal: Weight 2.45N Power Terminal: Weight 4.9N 90 Degree Bend	2	—	—	times
Module Weight (Typical)			—	8.5	—	Grams
Heatsink Flatness*9			-50	—	+100	μm

\*7 Bootstrap Diode (@T<sub>a</sub> = 25°C) Characteristics



\*8 Plain washers (ISO 7089-7094) are recommended.

\*9 Flatness measurement position.





Powerex, Inc., 173 Pavilion Lane, Youngwood, Pennsylvania 15697-1800 (724) 925-7272 www.pwr.com

**PS219B2-ST, PS219B2-AST, PS219B2-CST**  
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 5 Amperes/600 Volts

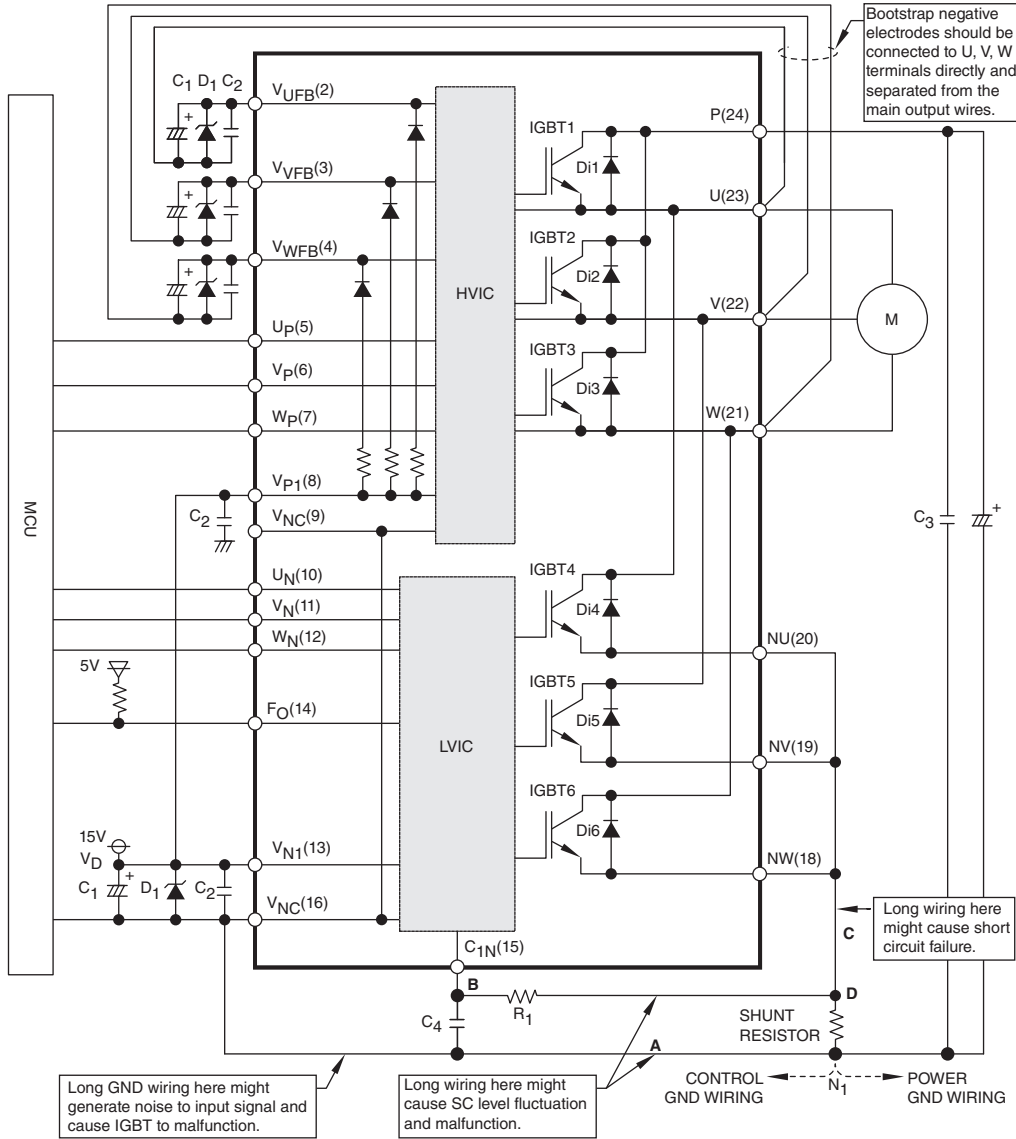
### Recommended Conditions for Use

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage	$V_{CC}$	Applied between P-N Terminals	0	300	400	Volts
Control Supply Voltage	$V_D$	Applied between $V_{P1}$ - $V_{NC}$ , $V_{N1}$ - $V_{NC}$	13.5	15.0	16.5	Volts
	$V_{DB}$	Applied between $V_{UFB-U}$ , $V_{VFB-V}$ , $V_{WFB-W}$	13.0	15.0	18.5	Volts
Control Supply Variation	$\Delta V_D$ , $\Delta V_{DB}$		-1	—	1	V/ $\mu$ s
Arm Shoot-through Blocking Time	$t_{DEAD}$	For Each Input Signal, $T_C \leq 100^\circ\text{C}$	1.0	—	—	$\mu$ s
Allowable Minimum Input	$P_{WIN(on)}$		0.7	—	—	$\mu$ s
Pulse Width*11	$P_{WIN(off)}$		0.7	—	—	$\mu$ s
$V_{NC}$ Voltage Variation	$V_{NC}$	Between $V_{NC-NU}$ , $NV$ , $NW$ (Including Surge)	-5.0	—	5.0	Volts
Junction Temperature	$T_j$		-20	—	125	$^\circ\text{C}$

\*11 DIPIPM may not respond if the input signal pulse is less than  $P_{WIN(on)}$ ,  $P_{WIN(off)}$ .

**PS219B2-ST, PS219B2-AST, PS219B2-CST**  
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## Application Circuit



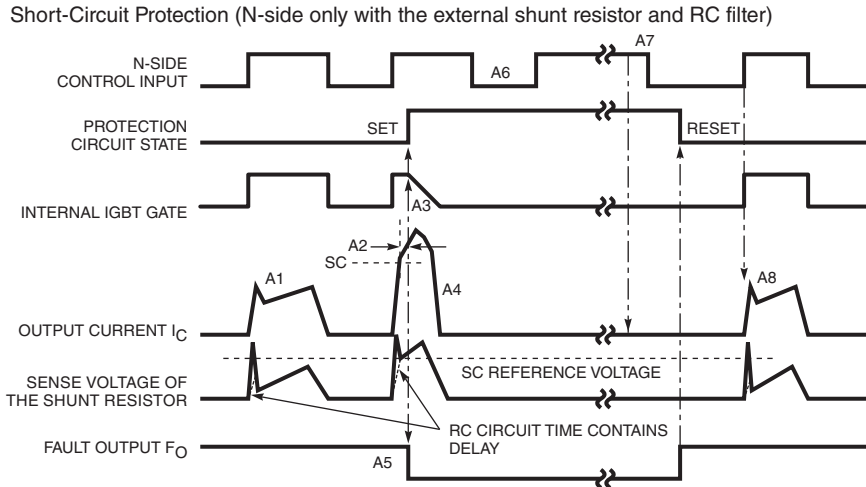
**Notes:**

- 1) It is recommended to connect Control GND wiring and Power GND wiring only at point N<sub>1</sub> (near terminal of shunt resistor) to prevent a malfunction by Power GND fluctuations.
- 2) It is recommended to insert a Zener diode D1 (24V/1W) between each pair of control supply terminals to prevent surge destruction.
- 3) To prevent surge destruction, the wiring between the DC bus smoothing capacitor and the P, N<sub>1</sub> terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N<sub>1</sub> terminals is recommended.
- 4) Time constant of R<sub>1</sub>, C<sub>4</sub> for SC protection circuit should be selected so that protection works within 2μs. (Recommended value: ≤2μs) SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type, is recommended for R<sub>1</sub>, C<sub>4</sub>.
- 5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
- 6) The point D at which the wiring to C<sub>1N</sub> filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.
- 7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2: 0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic types recommended.)
- 8) Input drive is active-high type. There is a 3.3kΩ (Min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meets the turn-on and turn-off threshold voltage.
- 9) F<sub>O</sub> output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V) by resistor makes I<sub>F0</sub> up to 1mA.
- 10) Direct coupling to the MCU without any opto-coupler or transformer isolation is possible because the HVIC is inside the module.
- 11) Two V<sub>NC</sub> terminals (9 & 16 pin) are connected inside the DIPIPM. Be sure to connect either one to the 15V power supply GND outside and leave the other one open.
- 12) IC malfunction can occur and cause the DIPIPM to operate erroneously when high frequency noise is superimposed on the control supply line. To avoid such problem, the line ripple voltage should meet dV/dt ≤ ±1V/μs and V<sub>ripple</sub> ≤ 2Vp-p.



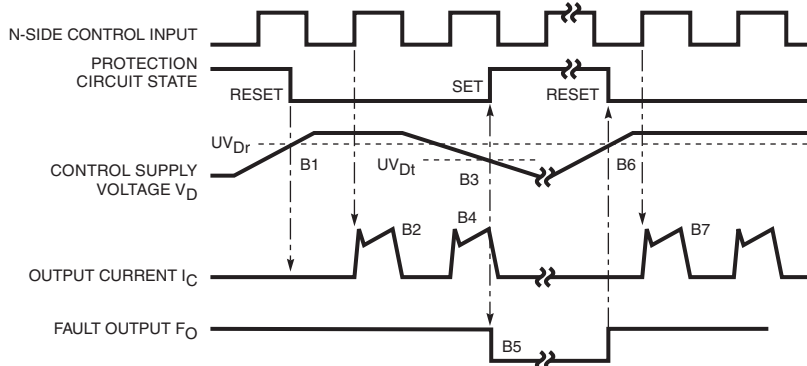
PS219B2-ST, PS219B2-AST, PS219B2-CST  
 Intellimod™ Module  
 Dual-In-Line Intelligent Power Module  
 5 Amperes/600 Volts

## Protection Function Timing Diagrams



- A1: Normal operation – IGBT turn on and conducting current.
- A2: Short-circuit current detected (SC trigger).
- A3: All N-side IGBT gate hard interrupted.
- A4: All N-side IGBTs turn off.
- A5:  $F_O$  output with a fixed pulse width of  $t_{FO(min)} = 20\mu s$ .
- A6: Input "L" – IGBT off.
- A7: Input "H" – IGBT off in spite of "H" input.
- A8: Normal operation – IGBT on and conducting current.

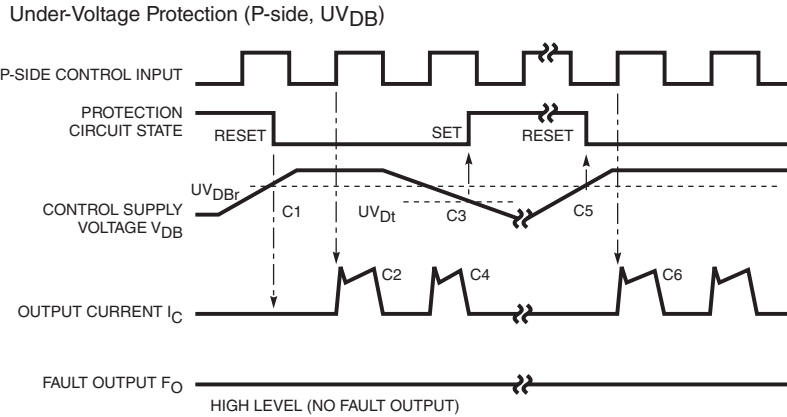
## Under-Voltage Protection (N-side, $UV_D$ )



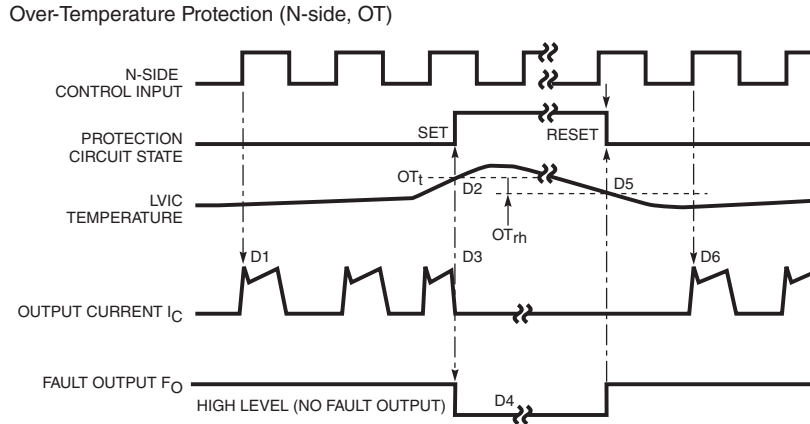
- B1: Control supply voltage rise – After the voltage level reaches  $UV_{Dr}$ , the drive circuit begins to work at the rising edge of the next input signal.
- B2: Normal operation – IGBT turn on and conducting current.
- B3: Under-voltage trip ( $UV_D$ ).
- B4: All N-side IGBTs turn off regardless of the control input level.
- B5:  $F_O$  output during under-voltage period, however, the minimum pulse width is  $20\mu s$ .
- B6: Under-voltage reset ( $UV_{Dr}$ ).
- B7: Normal operation – IGBT turn on and conducting current.

PS219B2-ST, PS219B2-AST, PS219B2-CST  
 Intellimod™ Module  
 Dual-In-Line Intelligent Power Module  
 5 Amperes/600 Volts

## Protection Function Timing Diagrams



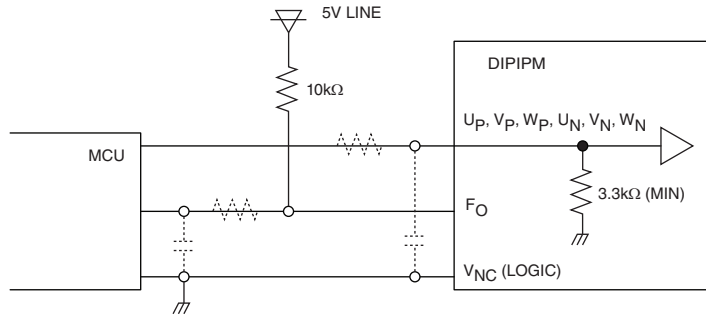
- C1: Control supply voltage rises – After the voltage level reaches  $UV_{DBr}$ , the drive circuit begins to work at the rising edge of the next input signal.
- C2: Normal operation – IGBT turn on and conducting current.
- C3: Under-voltage trip ( $UV_{DBt}$ ).
- C4: IGBT stays off regardless of the control input level, but there is no  $F_O$  signal output.
- C5: Under-voltage reset ( $UV_{Dr}$ ).
- C6: Normal operation – IGBT turn on and conducting current.



- D1: Normal operation – IGBT turn on and conducting current.
- D2: LVIC temperature exceeds over-temperature trip level ( $OT_t$ ).
- D3: All N-side IGBTs turn OFF in spite of control input condition.
- D4:  $F_O$  outputs during over-temperature period, however, the minimum pulse width is 20 $\mu$ s.
- D5: LVIC temperature is lower than over-temperature reset level.
- D6: Circuits start to operate normally when next input is applied.

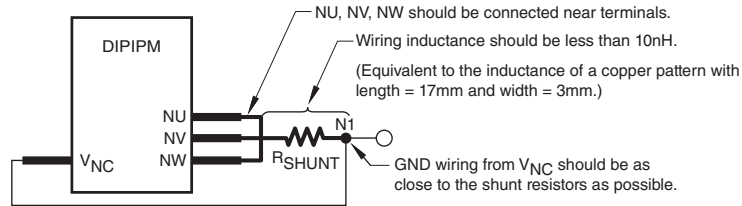
PS219B2-ST, PS219B2-AST, PS219B2-CST  
 Intellimod™ Module  
 Dual-In-Line Intelligent Power Module  
 5 Amperes/600 Volts

## Typical Interface Circuit

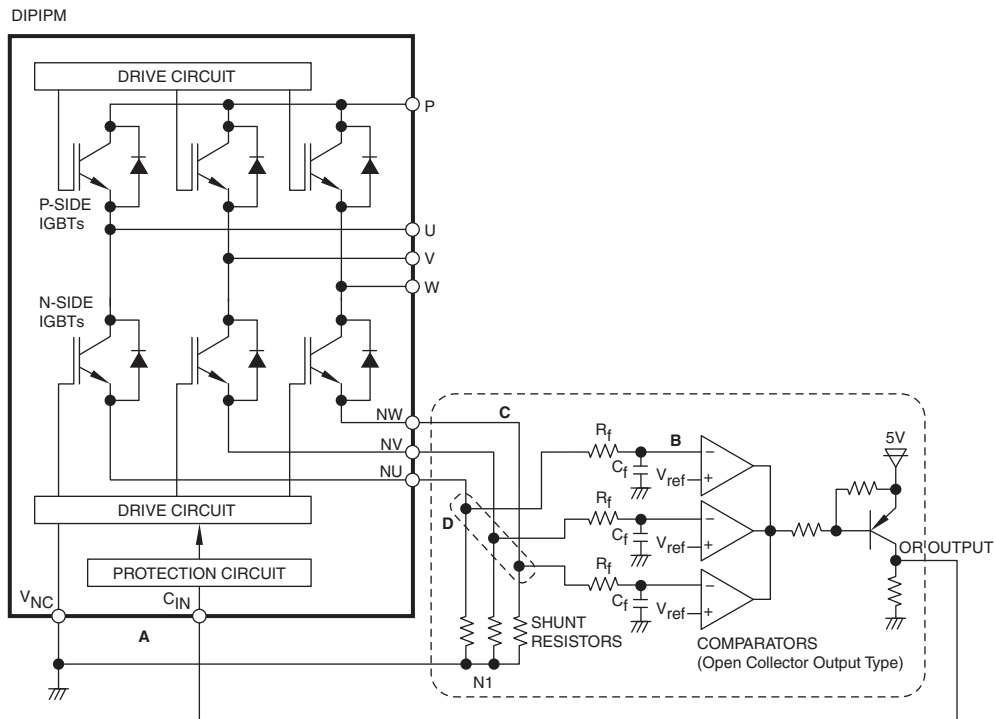


NOTE: RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. The DIPIPM input signal section integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

## Pattern Wiring Around Shunt Resistor



## External S<sub>C</sub> Protection Circuit Using Three Shunt Resistors



Notes:

- 1) It is necessary to set the time constraint  $R_f$ ,  $C_f$  of external comparator input so that the IGBT stops within  $2\mu\text{s}$  when short circuit occurs. SC interrupting time can vary with the wiring pattern, comparator speed and so on.
- 2) The threshold voltage  $V_{ref}$  should be set up as the same rating as the short circuit trip level ( $V_{SC(ref)}$ , typically 0.48V).
- 3) Select the external shunt resistance so that the SC trip-level is less than specified value ( $\leq 1.7$  times current rating).
- 4) Wiring A, B, and C should be as short as possible to avoid a malfunction.
- 5) Where the wiring to the comparator is divided, point D, should be near the shunt resistor terminal.
- 6) OR output high level should be over 0.53V (= maximum  $V_{SC(ref)}$ ).