RT9231 Data Sheet



6F, No. 35, Shin Tai Road, Chu-Pay, Hsin-Chu, Taiwan, R.O.C. Tel: (8863)5510047 Fax: (8863)5537749

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Advanced PWM and Triple Linear Power Controller

General Description

The RT9231 is a 4-in-one power controller optimized for high-performance microprocessor and computer applications. The IC integrates a PWM controller, triple linear controller as well as monitoring and protection functions into a 28-pin SOP package. The PWM controller regulates the microprocessor core voltage with a synchronous buck converter. The first linear controller supplies the computer system's AGP 1.5V or 3.3V bus power. The second linear controller provides power for the 1.5V GTL bus and the 3rd linear controller provides 1.8V power for the North/South Bridge core voltage and/or cache memory circuits.

The RT9231 features an Intel-compatible, TTL 5-bit programmable DAC that adjusts the core voltage from 2.1V to 3.5V in 0.1V increments and from 1.3V to 2.05V in 0.05V steps. The 5-bit DAC has a typical ±1% tolerance. The first linear controller is user-selectable for output level of 1.5V and 3.3V with ±2.5% accuracy. The other two linear controllers provide fixed output voltages of 1.5V ±3% and 1.8V ±3%. All the three linear controllers drive external N-MOSFET or NPNs bipolar for the pass transistor.

The RT9231 monitors all the output voltages. A power-good signal is issued when the core voltage is within ±10% of the DAC setting and the other levels are above their under-voltage levels. Additional build-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltage above 115% of the DAC setting. The PWM over-current function monitors the output current using the voltage drop across the MOSFET's $R_{DS(ON)}$, which eliminates the need for a current sensing resistor.

Ordering Information

RT9231-□ □

- Package Type
  - S: SOP-28
- Operating Temperature Range
  - C: Commercial standard
  - M: Military standard

Features:

- 4-in-one Regulated Voltages for Microprocessor Core, AGP Bus, North/South Bridge and/or Cache Memory, GTL Bus Power
- Compatible with HIP6021
- Power-good Output Voltage Monitor

Switching section

- 5-bit DAC Programmable from 1.3V to 3.5V
- ±1% DAC Accuracy
- Fast Transient Response
- Full 0% to 100% Duty Cycle Driver
- Switching Frequency from 50kHz to 500kHz
- Adaptive Non-overlapping Gate Driver
- Over-current Monitor Uses MOSFET $R_{DS(ON)}$
- Over-voltage Protection Uses Lower MOSFET

Linear Section

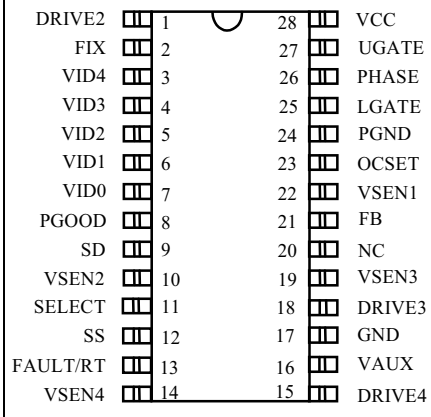
- Fixed or User-adjustable Linear Regulator Output Voltage
- MOSFET and NPN Driving Capability
- Ultra Fast Response Speed
- Under-voltage Protection
- Internal Thermal Shutdown

Applications:

- Full Motherboard Power Regulation for Computer
- Low-voltage Distributed Power Supplies

Pin Configurations

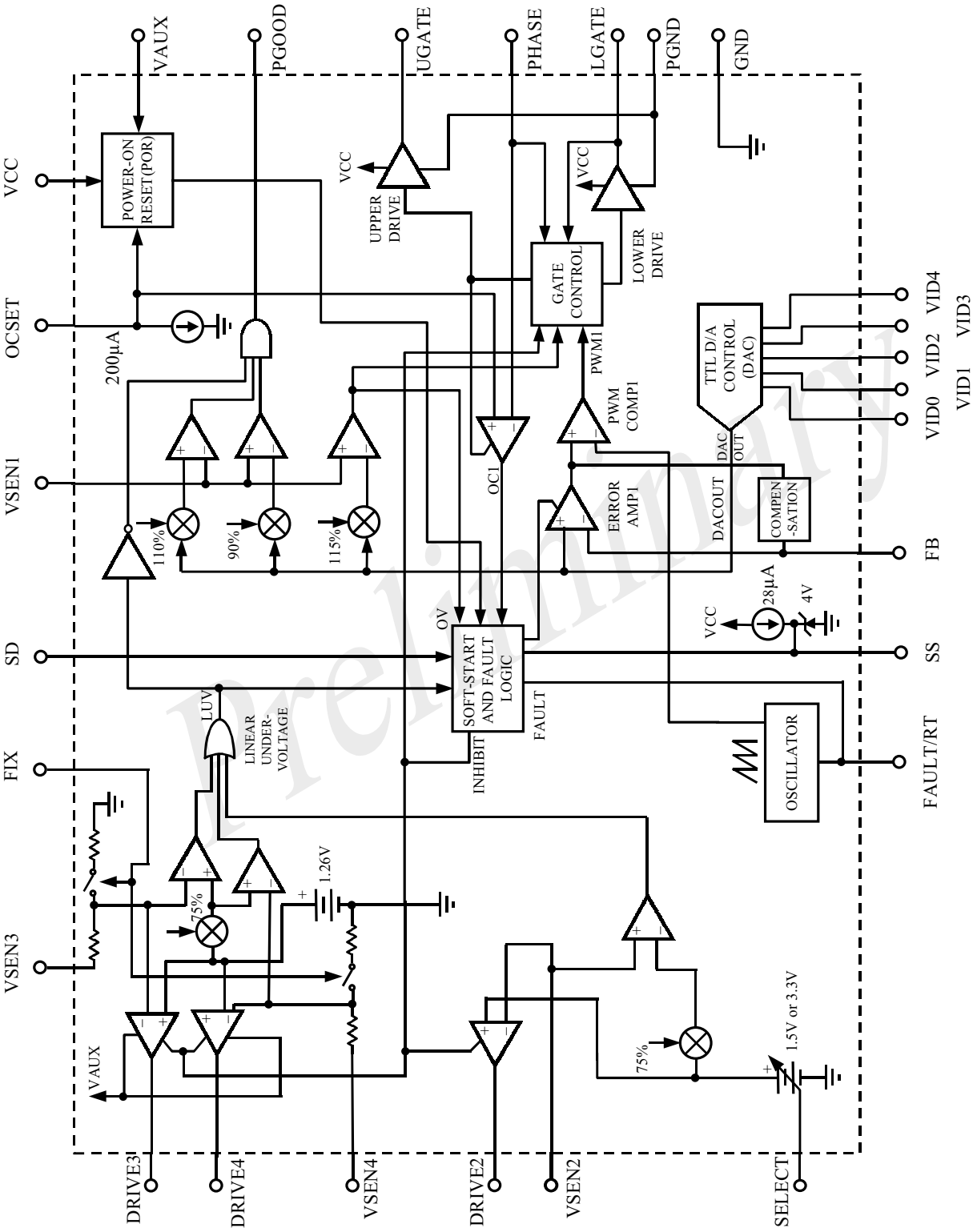
Part Number	Pin Configurations
RT9231CS	TOP



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Block Diagram



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Absolute Maximum Ratings

- Supply Voltage, V_{CC} ---------- +15V
- PGOOD, FAULT/RT and GATE Voltage ---------- GND–0.3V to V_{CC}+0.3V
- Input, Output or I/O Voltage ---------- GND–0.3V to 7V
- Ambient Temperature Range (T_A) ---------- 0℃ to +70℃
- Junction Temperature Range (T_J) ---------- 0℃ to +125℃
- Storage Temperature Range (T_{STG}) ---------- –65℃ to +150℃
- Lead Temperature (Soldering) 10 seconds (T_L) ---------- 300℃
- Thermal Impedance Junction to Ambient (θ_{JA}) ---------- 75℃/W
- Thermal Impedance Junction to Case (θ_{JC}) ---------- 25℃/W

Recommended Operating Conditions

- Supply Voltage, V_{CC} ---------- +12V±10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

CAUTION:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

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Electrical Specifications

V_{CC}=12V, PGND=0V, T_A=25℃, Unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply Current	I_{CC}	UGATE, LGATE, DRIVE2, DRIVE3, and DRIVE4 Open	-	10	-	mA
POWER-ON RESET						
Rising VCC Threshold		V_{OCSET} = 4.5V	7.5	-	9.5	V
Falling VCC Threshold		V_{OCSET} = 4.5V	7	-	9	V
Rising VAUX Threshold		V_{OCSET} = 4.5V	-	2.8	-	V
VAUX Threshold Hysteresys		V_{OCSET} = 4.5V	-	0.5	-	V
Rising V_{OCSET} Threshold			-	1.25	-	V

OSCILLATOR						
Free Running Frequency		RT = Open	180	200	225	kHz
Ramp Amplitude	ΔV_{OSC}	RT = Open	-	1.9	-	Vp-p
DAC AND BANDGAP REFERNECE						
DAC(VID0-VID4) Input Low Voltage			-	-	0.8	V
DAC(VID0-VID4) Input High Voltage			2.0	-	-	V
DACOUT Voltage Accuracy		DACOUT= 2.05~3.50V	–1	-	1	%
DACOUT Voltage Accuracy		DACOUT =1.30~2.00V	–1%	-	20mV	-
Bandgap Reference Voltage	V_{BG}		1.240	1.265	1.290	V
LINEAR REGULATORS(OUT2, OUT3, AND OUT4)						
VSEN2 Regulation voltage	$VREG_2$	SELECT <0.8V	1.462	1.500	1.538	V
VSEN2 Regulation Voltage	$VREG_2$	SELECT >2.0V	3.218	3.300	3.382	V
VSEN3 Regulation Voltage	$VREG_3$		1.455	1.500	1.545	V
VSEN4 Regulation Voltage	$VREG_4$		1.746	1.800	1.854	V
Under-Voltage Level (All Linears) (VSEN/VREG)	$VSEN3_{UV}$	VSEN3 Rising	-	75	-	%
Under-Voltage Hysteresis (All Linears) (VSEN/VREG)		VSEN3 Falling	-	100	-	mV
Output Drive Current (All Linears)		VAUX=5V	20	40	-	mA
SYNCHRONOUS PWM CONTROLLER ERROR AMPLIFIER						
DC Gain			-	65	-	dB
PWN CONTROLLER GATE DRIVER						
Upper Drive Source	R_{UGATE}	VCC=12V, VCC–V_{UGATE} =1V	-	4	7	Ω
Upper Drive Sink	R_{UGATE}	V_{UGATE}=1V	-	3	7	Ω
Lower Drive Source	I_{LGATE}	VCC=12V, V_{LGATE}=2V	-	1	-	A
Lower Drive Sink	R_{LGATE}	V_{LGATE}=1V	-	2	6	Ω
PROTECTION						
V_{OUT1} Over-Voltage Trip		VSEN1 Rising	112	115	118	%
FAULT Souring Current	I_{OVP}	V_{FAULT}=8V	10	14	-	mA
OCSET1 Current Source	I_{OCSET1}	V_{OCSET1}=4.5V	170	200	230	µA
Soft-Start Current	I_{SS}	Vss=1V	-	11	-	µA
POWER GOOD						
V_{OUT1} Upper Threshold		VSEN1 Rising	108	-	112	%
V_{OUT1} Under Voltage		VSEN1 Rising	90	-	94	%
V_{OUT1} Hysteresis(VSEN1/DACOUT)		Upper/Lower Threshold	-	2	-	%
PGOOD Voltage Low	V_{PGOOD}	I_{PGOOD}=-4mA	-	-	0.5	V

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Functional Pin Description

VCC (Pin 28)
Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin monitored for power-on reset (POR) purpose.

GND (Pin 17)
Signal ground for the IC. All voltage levels are measured with respect to this pin.

PGND (Pin 24)
This is the power ground of UGATE. Tie the synchronous PWM converter's lower MOSFET source to this pin.

VAUX (Pin 16)
This pin provides boost current for the two linear regulator output drives in the event bipolar NPN transistors (instead of N-channel MOSFETs) are employed as pass elements. The voltage at this pin is monitored for power-on reset (POR) purpose.

SS (Pin 12)
Connect a capacitor from this pin to ground. This capacitor, along with an internal 28μA (Vss>1V) current source, sets the soft-start interval of the converter.

FAULT/RT (Pin 13)
This pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) form this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$Fs = 200kHz + \frac{3.5\times 10^6}{R_T(k\Omega)} (R_T \text{ to GND})$$

Conversely, connecting a pull-up resistor (R_T) from this pin to VCC reduces the switching frequency according to the following equation:

$$Fs = 200kHz - \frac{2.8\times 10^7}{R_T(k\Omega)} (R_T \text{ to 12V})$$

Nominally, the voltage at this pin is 1.26V, in the event of an over-voltage or over-current condition, this pin is internally pulled to VCC.

PGOOD (Pin 8)
PGOOD is an open collector output used to indicate the status of the PWM converter output voltage. This pin is pulled low when the synchronous regulator output is not within ±10% of the DACOUT reference voltage, or when any of the other outputs are below their under-voltage thresholds. The PGOOD output is open for '11111'VID code.

SD (Pin 9)
This pin shuts down the entire IC. A TTL-compatible, logic level high signal applied at this pin immediately disables all outputs. When re-enabled, the IC undergoes a new soft-start cycle. Left open, this pin is pulled low by an internal pull-down current source, enabling operation.

FIX (Pin 2)
Grounding this pin bypasses the internal resistor dividers that set the voltage of the 1.5V and 1.8V linear regulators. This way, the output voltage of the two regulators can be adjusted from 1.3V up to the input voltage (+3.3V or +5V) by way of an external resistor divider corrected at the corresponding VSEN pin. The new output voltage set by the external resistor divider can be determined using the following formula:

$$V_{OUT} = 1.265V \times \left[1+ \frac{R_{OUT}}{R_{GND}}\right]$$

Where R_{OUT} is the resistor connected from VSEN to the output of the regulator, and R_{GND} is the resistor connected from VSEN to ground. Left open, this pin is pulled high enabling fixed output voltage operation.

VID0, VID1, VID2, VID3, VID4 (Pin 7, 6, 5, 4, and 3)
VID0-4 are TTL-compatible the input pins to the 5-bit DAC. The state logic of these five pins program the internal voltage reference, DACOUT. The level of DACOUT sets the

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microprocessor core converter output voltage, as well as the corresponding PGOOD and OVP thresholds. Table 1 specifies the DACOUT voltage of 32 combinations of VID levels.

OCSET (Pin 23)
Connect a resistor from this pin to the drain of the respective upper MOSFET. This resistor, an internal 200μA current source, and the upper MOSFET on-resistance set the converter over-current trip point. An over-current trip cycles the soft-start function. The voltage at this pin is monitored for power-on reset (POR) purpose and pulling this pin low with an open drain device will shut down the IC.

PHASE (Pin 26)
Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin represents the gate drive return current path and is used to monitor the voltage drop across the upper MOSFET for over-current protection.

UGATE (Pin 27)
Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

LGATE (Pin 25)
Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

FB (Pin 21)
This pin is connected to the PWM converter's output voltage.

VSEN1 (Pin 22)
This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use the signal to report output voltage status and for over-voltage protection.

DRIVE2 (Pin 1)
Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the AGP regulator's pass transistor.

VSEN2 (Pin 10)
Connect this pin to the output of the AGP linear regulator. The voltage at this pin is regulated to the level pre-determined by the logic-level status of the SELECT pin. This pin is also monitored for under-voltage events.

SELECT (Pin 11)
This pin determines the output voltage of the AGP bus switching regulator. A low TTL input sets the output voltage to 1.5V while a high input sets the output voltage to 3.3V.

DRIVE3 (Pin 18)
Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the 1.5V regulator's pass transistor.

VSEN3 (Pin 19)
Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for under-voltage events.

DRIVE4 (Pin 15)
Connect this pin to the gate of an external MOSEFT. This pin provides the drive for the 1.8V regulator's pass transistor.

VSEN4 (Pin 14)
Connect this pin to the output of the 1.8V regulator. This pin is monitored for under-voltage events.

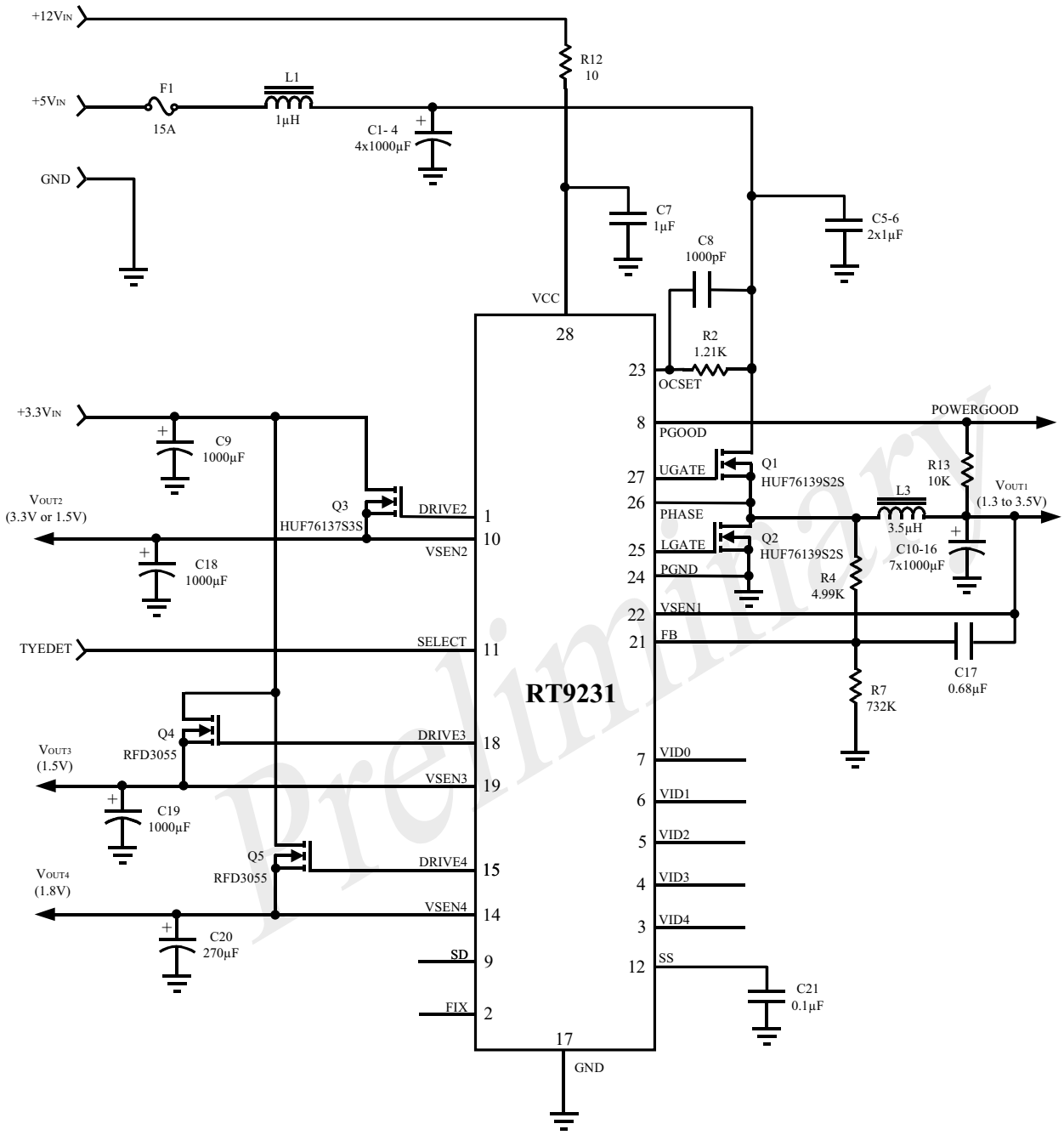
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Table 1. VOUT1 Voltage Program

Pin Name					Normal OUT1 Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	INHIBIT
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60
1	1	0	0	0	2.70
1	0	1	1	1	2.80
1	0	1	1	0	2.90
1	0	1	0	1	3.00
1	0	1	0	0	3.10
1	0	0	1	1	3.30
1	0	0	1	0	3.30
1	0	0	0	1	3.40
1	0	0	0	0	3.50

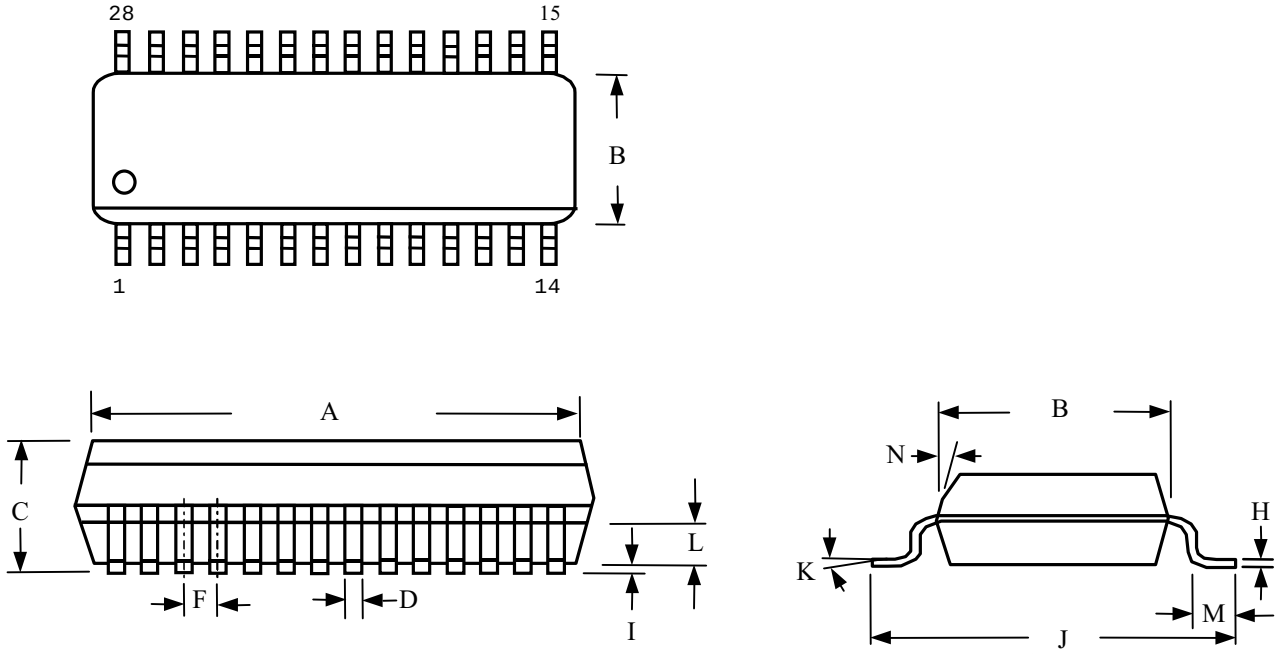
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Typical Application Circuit



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Package Information



Symbols	Dimensions In Inches			Dimensions In Millimeter		
	Min	Norm	Max	Min	Norm	Max
A	0.701	0.705	0.709	17.800	17.900	18.000
B	0.291	0.295	0.299	7.400	7.500	7.600
C	0.090	0.092	0.094	2.280	2.330	2.380
D	0.015	0.016	0.017	0.390	0.400	0.410
F	-	0.050	-	-	1.270	-
H	0.008	0.009	0.010	0.200	0.230	0.260
I	0.003	0.006	0.009	0.080	0.160	0.240
J	0.405	0.409	0.413	10.300	10.400	10.500
K	-	5°	-	-	5°	-
L	0.035	0.039	0.043	0.900	1.000	1.100
M	0.020	0.028	0.035	0.500	0.700	0.900
N	--	7°	--	--	7°	--

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