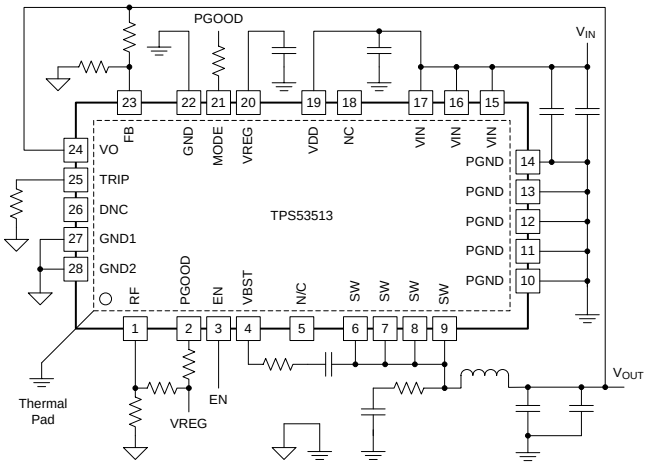
1.5 to 18 V (4.5 to 25 V bias) Input, 8-A Single Synchronous Step-Down SWIFT™ Converter

FEATURES

- **Integrated 13.8 and 5.9 mΩ MOSFETs With 8-A Continuous Output Current**
- **Supports All Ceramic Output Capacitors**
- **Reference Voltage 600 mV ±0.5% Tolerance**
- **Output Voltage Range: 0.6 V to 5.5 V**
- **D-CAP3™ Control Mode With Fast Load-Step Response**
- **Auto-Skipping Eco-mode™ for High Light-Load Efficiency**
- **FCCM for Tight Output Ripple and Voltage Requirements**
- **Eight Selectable Frequency Settings from 200 kHz to 1 MHz**
- **Pre-Charged Startup Capability**
- **Built-in Output Discharge Circuit**
- **Open-Drain Power-Good Output**
- **3.5-mm × 4.5-mm, 28-Pin, QFN Package**



APPLICATIONS

- **Server and Cloud-Computing POLs**
- **Broadband, Networking, and Optical Communications Infrastructure**
- **I/O Supplies**
- **Supported at the WEBENCH™ Design Center**

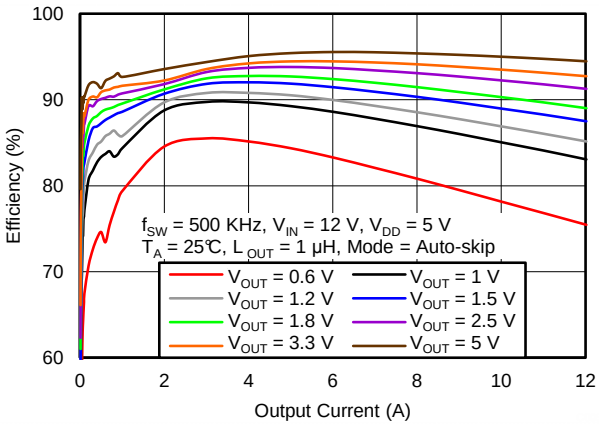
DESCRIPTION

The TPS53513 is a small-sized, synchronous buck converter with an adaptive on-time D-CAP3 control mode. The device offers ease-of-use and low external-component count for space-conscious power systems.

This device features high-performance integrated MOSFETs, accurate 0.5% 0.6-V reference, and an integrated boost switch. Competitive features include very-low external-component count, fast load-transient response, auto-skip mode operation, internal soft-start control, and no requirement for compensation

A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS53513 is available in a 28-pin QFN package and is specified from –40°C to 85°C ambient temperature.

EFFICIENCY



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE		UNIT
			MIN	MAX	
Input voltage range(2)	EN		–0.3	7.7	V
	SW	DC	–3	30	
		Transient < 10 ns	–5	32	
	VBST		–0.3	36	
	VBST(3)		–0.3	6	
	VBST when transient < 10 ns			38	
	VDD		–0.3	28	
	VIN		–0.3	30	
	VO, FB, MODE, RF		–0.3	6	
Output voltage range	PGOOD		–0.3	7.7	V
	VREG, TRIP		–0.3	6	
Temperature	Junction, T_J		–40	150	°C
	Storage, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Voltage values are with respect to the SW terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53513 RVE 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	34.1	
θ_{JB}	Junction-to-board thermal resistance(4)	18.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.8	
ψ_{JB}	Junction-to-board characterization parameter(6)	18.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	EN	–0.1	7	V
	SW	–3	27	
	VBST	–0.1	28	
	VBST(1)	–0.1	5.5	
	VDD	4.5	25	
	VIN	1.5	18	
	VO, FB, MODE, RF	–0.1	5.5	
Output voltage range	PGOOD	–0.1	7	V
	VREG, TRIP	–0.1	5.5	
T_A	Operating free-air temperature	–40	85	°C

(1) Voltage values are with respect to the SW pin.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, VREG = 5 V, EN = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VDD}	VDD bias current	T_A = 25°C, No load Power conversion enabled (no switching)		1350	1850	µA
$I_{VDDSTBY}$	VDD standby current	T_A = 25°C, No load Power conversion disabled		850	1150	µA
$I_{VIN(leak)}$	VIN leakage current	V_{EN} = 0 V			0.5	µA
VREF OUTPUT						
V_{VREF}	Reference voltage	FB w/r/t GND, T_A = 25°C	597	600	603	mV
$V_{VREFTOL}$	Reference voltage tolerance	FB w/r/t GND, T_J = 0°C to 85°C	–0.6%		0.5%	
		FB w/r/t GND, T_J = –40°C to 85°C	–0.7%		0.5%	
OUTPUT VOLTAGE						
I_{FB}	FB input current	V_{FB} = 600 mV		50	100	nA
I_{VODIS}	VO discharge current	V_{VO} = 0.5 V, Power Conversion Disabled	10	12	15	mA
SMPS FREQUENCY						
f_{SW}	VO switching frequency(1)	V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} < 0.041		250		kHz
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} = 0.096		300		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} = 0.16		400		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} = 0.229		500		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} = 0.297		600		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} = 0.375		750		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} = 0.461		850		
		V_{IN} = 12 V, V_{VO} = 3.3 V, R_{DR} > 0.557		1000		
$t_{ON(min)}$	Minimum on-time	T_A = 25°C(2)		60		ns
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	175	240	310	ns
INTERNAL BOOTSTRAP SW						
V_F	Forward Voltage	$V_{VREG–VBST}$, T_A = 25°C, I_F = 10 mA		0.15	0.25	V
I_{VBST}	VBST leakage current	T_A = 25°C, V_{VBST} = 33 V, V_{SW} = 28 V		0.01	1.5	µA

(1) Resistor divider ratio (R_{DR}) is described in Equation 1.
(2) Specified by design. Not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, VREG = 5 V, EN = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD						
V_{ENH}	EN enable threshold voltage		1.3	1.4	1.5	V
V_{ENL}	EN disable threshold voltage		1.1	1.2	1.3	V
V_{ENHYST}	EN hysteresis voltage			0.22		V
V_{ENLEAK}	EN input leakage current		–1	0	1	µA
SOFT START						
t_{SS}	Soft-start time			1		ms
PGOOD COMPARATOR						
V_{PGTH}	VDDQ PGOOD threshold	PGOOD in from higher	104%	108%	111%	
		PGOOD in from lower	89%	92%	96%	
		PGOOD out to higher	113%	116%	120%	
		PGOOD out to lower	80%	84%	87%	
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5 V	4	6		mA
t_{PGDLY}	PGOOD delay time	Delay for PGOOD going in	0.8	1.0	1.2	ms
		Delay for PGOOD coming out		2		µs
I_{PGLK}	PGOOD leakage current	V_{PGOOD} = 5 V	–1	0	1	µA
CURRENT DETECTION						
R_{TRIP}	TRIP pin resistance range		20		50	kΩ
I_{OCL}	Current limit threshold, valley	R_{TRIP} = 34.8 kΩ	6.2	8.0	9.8	A
		R_{TRIP} = 25.5 kΩ	4.2	6.2	8.2	
I_{OCLN}	Negative current limit threshold, valley	R_{TRIP} = 34.8 kΩ	–10.5	–7.9	–5.3	A
		R_{TRIP} = 25.5 kΩ	–8.7	–6.1	–3.5	
V_{ZC}	Zero cross detection offset			0		mV
PROTECTIONS						
$V_{VREGUVLO}$	VREG undervoltage-lockout (UVLO) threshold voltage	Wake-up	3.25	3.34	3.41	V
		Shutdown	3.00	3.12	3.19	
$V_{VDDUVLO}$	VDD UVLO threshold voltage	Wake-up (default)	4.15	4.25	4.35	V
		Shutdown	3.95	4.05	4.15	
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	OVP detect voltage	116%	120%	124%	
t_{OVPDLY}	OVP propagation delay	With 100-mV overdrive		300		ns
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	UVP detect voltage	64%	68%	71%	
t_{UVPDLY}	UVP delay	UVP filter delay		1		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(3)	Shutdown temperature		140		°C
		Hysteresis		40		
LDO VOLTAGE						
V_{REG}	LDO output voltage	V_{IN} = 12 V, I_{LOAD} = 10 mA	4.65	5	5.45	V
V_{DOVREG}	LDO low droop drop-out voltage	V_{IN} = 4.5 V, I_{LOAD} = 30 mA, T_A = 25°C			365	mV
I_{LDOMAX}	LDO over-current limit	V_{IN} = 12 V, T_A = 25°C	170	200		mA
INTERNAL MOSFETS						
$R_{DS(on)H}$	High-side MOSFET on-resistance	T_A = 25°C		13.8	15.5	mΩ
$R_{DS(on)L}$	Low-side MOSFET on-resistance	T_A = 25°C		5.9	7.0	mΩ

(3) Specified by design. Not production tested.

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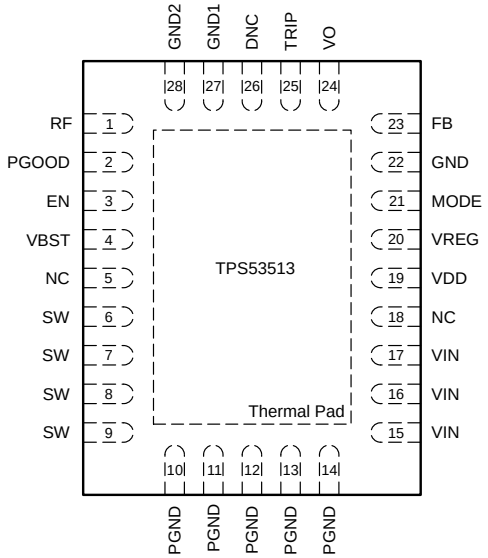
DEVICE INFORMATION

RVE PACKAGE
28-PIN
(TOP VIEW)



PIN DESCRIPTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
EN	3	I	The enable pin turns on the DC-DC switching converter.
FB	23	I	V_{OUT} feedback input. Connect this pin to a resistor divider between the VOUT pin and GND.
GND	22	G	This pin is the ground of internal analog circuitry and driver circuitry. Connect GND to the PGND plane with a short trace (For example, connect this pin to the thermal pad with a single trace and connect the thermal pad to PGND pins and PGND plane).
GND1	27	I	Connect this pin to ground. GND1 is the input of unused internal circuitry and must connect to ground.
GND2	28	I	Connect this pin to ground. GND2 is the input of unused internal circuitry and must connect to ground.
MODE	21	I	The MODE pin sets the forced continuous-conduction mode (FCCM) or Skip-mode operation. It also selects the ramp coefficient of D-CAP3 mode.
NC	5	—	Not connected. These pins are floating internally.
	18		
DNC	26	O	Do not connect. This pin is the output of unused internal circuitry and must be floating.
PGND	10	G	These ground pins are connected to the return of the internal low-side MOSFET.
	11		
	12		
	13		
	14		
PGOOD	2	O	Open-drain power-good status signal which provides startup delay after the FB voltage falls within the specified limits. After the FB voltage moves outside the specified limits, PGOOD goes low within 2 µs.
RF	1	I	RF is the SW-frequency configuration pin. Connect this pin to a resistor divider between VREG and GND to program different SW frequency settings.
SW	6	I/O	SW is the output switching terminal of the power converter. Connect this pin to the output inductor.
	7		
	8		
	9		

(1) I = Input, O = Output, P = Supply, G = Ground

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PIN DESCRIPTIONS (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
TRIP	25	I/O	TRIP is the OCL detection threshold setting pin. I_{TRIP} = 10 µA at room temp, 3000 ppm/°C current is sourced and sets the OCL trip voltage. See the Current Sense and Overcurrent Protection section for detailed OCP setting.
VBST	4	P	VBST is the supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to the SW node. Internally connected to VREG via bootstrap PMOS switch.
VDD	19	P	Power-supply input pin for controller. Input of the VREG LDO. The input range is from 4.5 to 25 V.
VIN	15	P	VIN is the conversion power-supply input pins.
	16		
	17		
VREG	20	O	VREG is the 5-V LDO output. This voltage supplies the internal circuitry and gate driver.
VO	24	I	VOUT voltage input to the controller.

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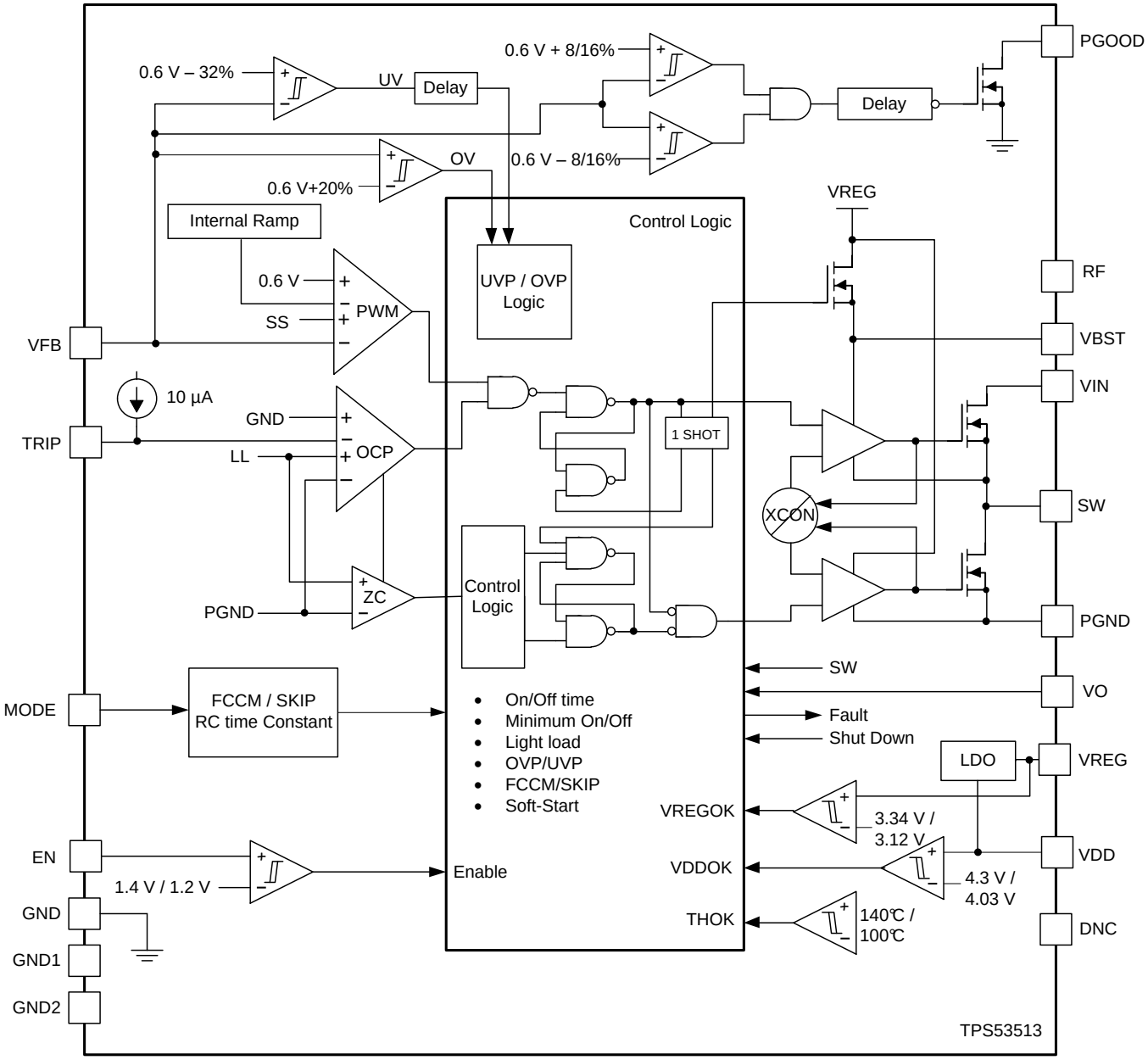
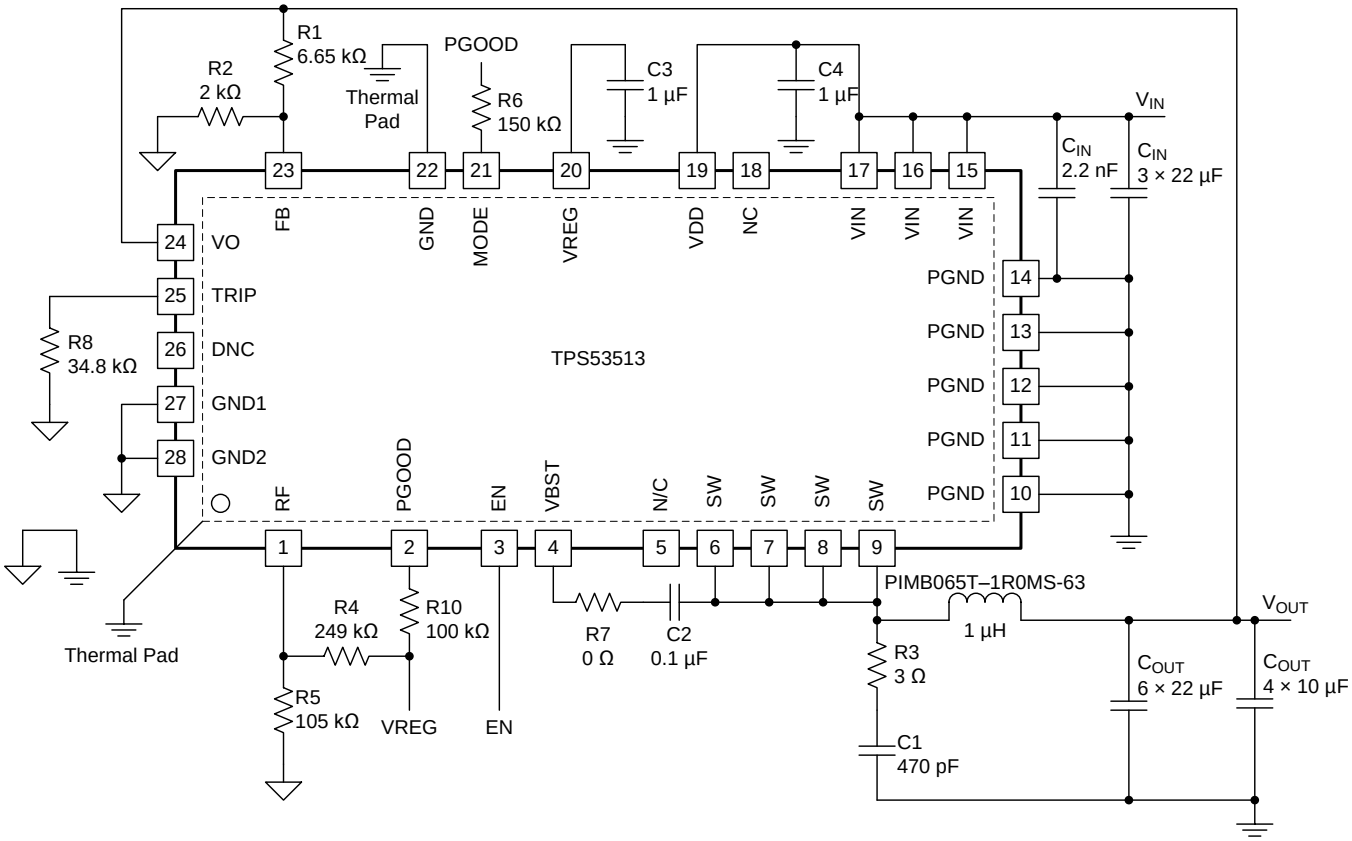
BLOCK DIAGRAM



APPLICATION CIRCUIT DIAGRAM



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TYPICAL CHARACTERISTICS

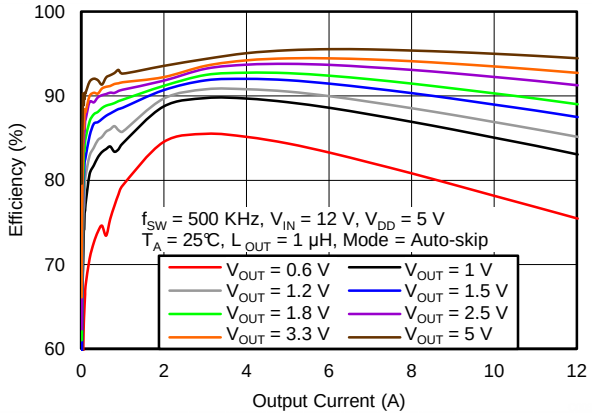

Figure 1. Efficiency vs. Output Current

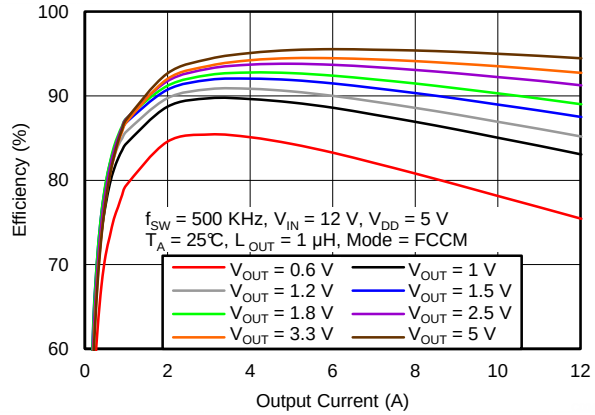

Figure 2. Efficiency vs. Output Current

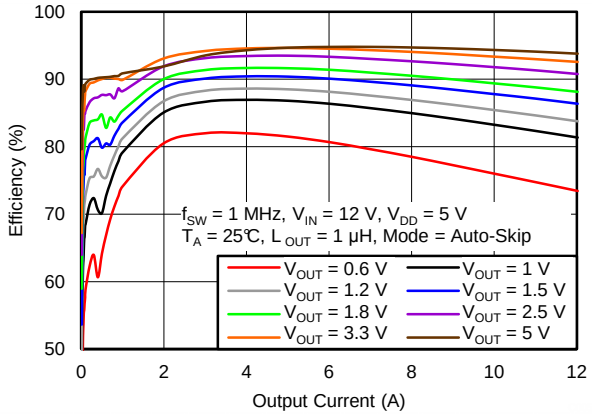

Figure 3. Efficiency vs. Output Current

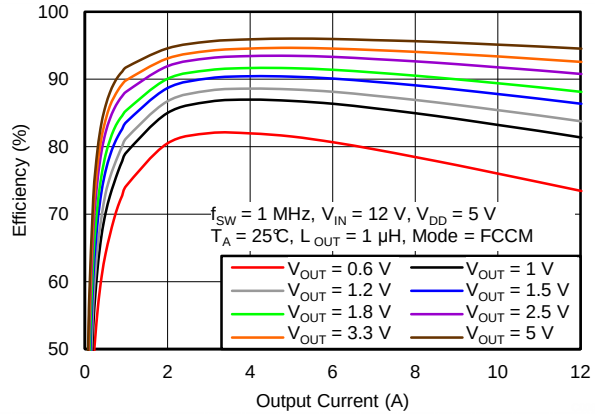

Figure 4. Efficiency vs. Output Current

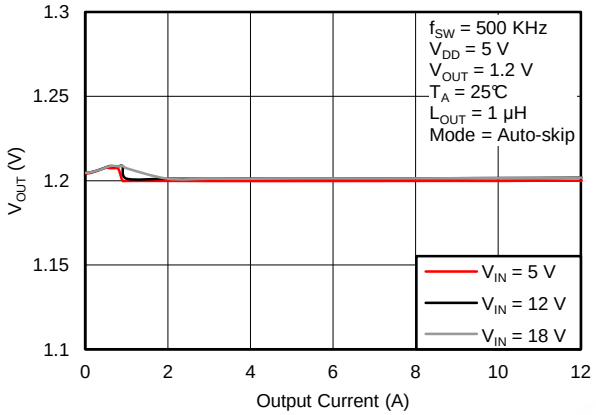

Figure 5. Output Voltage vs. Output Current

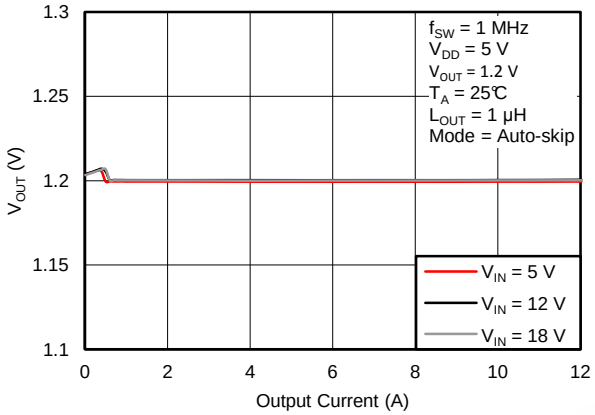

Figure 6. Output Voltage vs. Output Current

TYPICAL CHARACTERISTICS (continued)

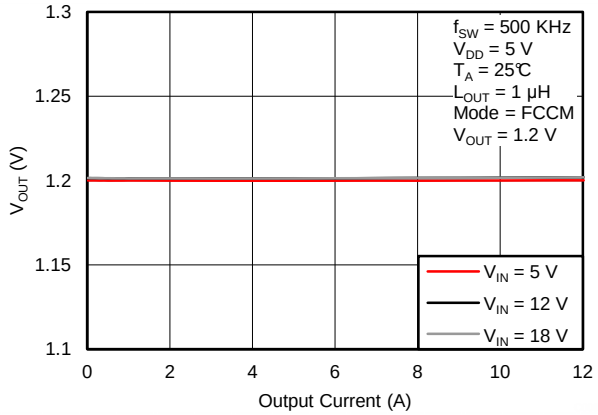

Figure 7. Output Voltage vs. Output Current

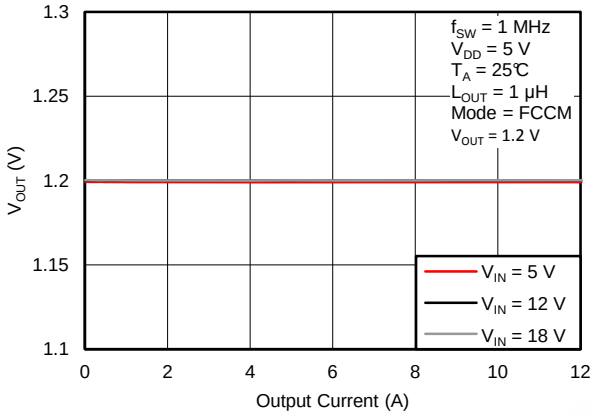

Figure 8. Output Voltage vs. Output Current

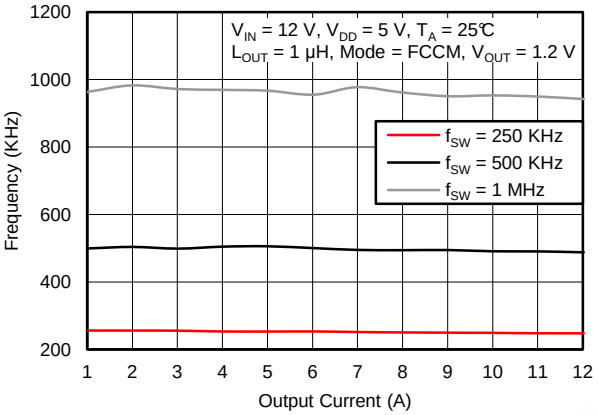

Figure 9. Switching Frequency vs. Output Current

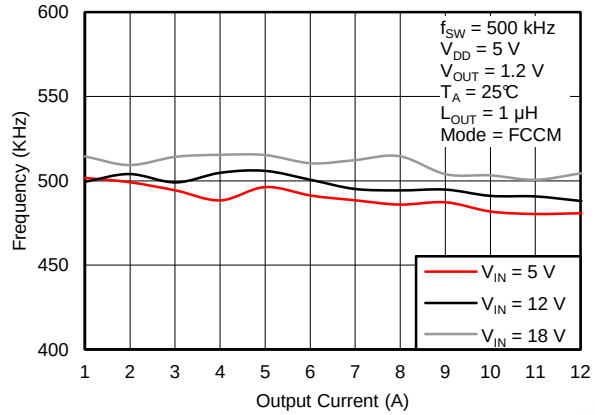

Figure 10. Switching Frequency vs. Output Current

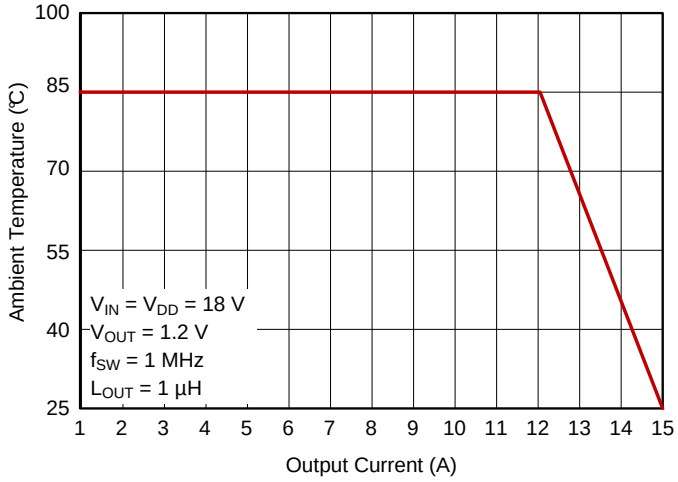

Figure 11. Safe Operating Area, V_{OUT} = 1.2 V

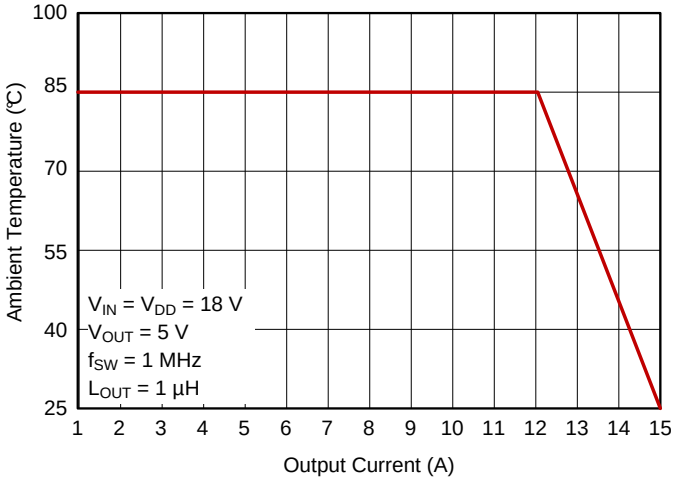

Figure 12. Safe Operating Area, V_{OUT} = 5 V

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TYPICAL CHARACTERISTICS (continued)

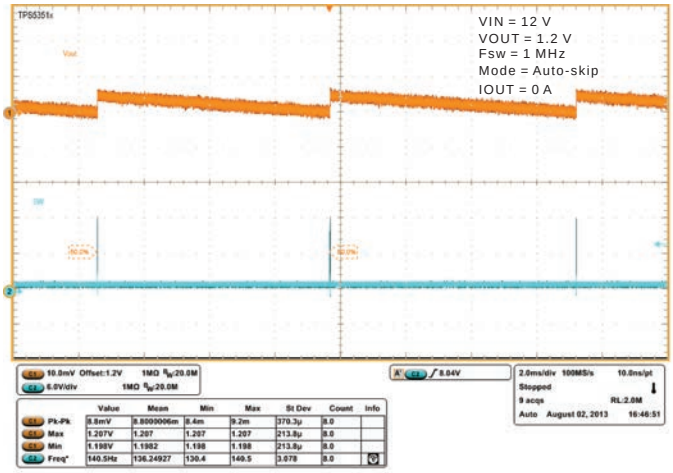

Figure 13. Auto-Skip Steady-State Operation

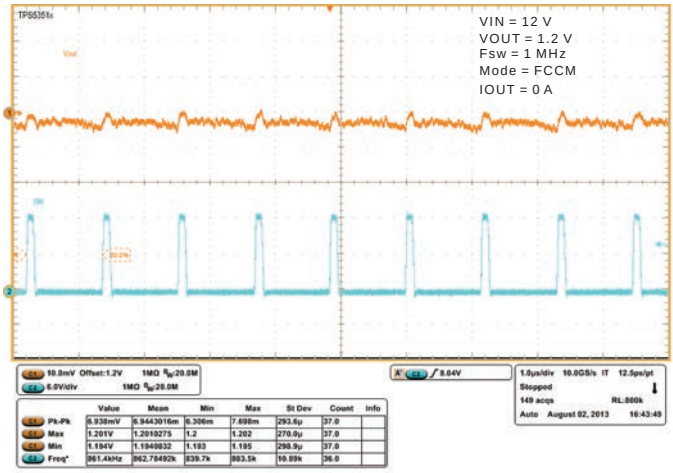

Figure 14. FCCM Steady-State Operation

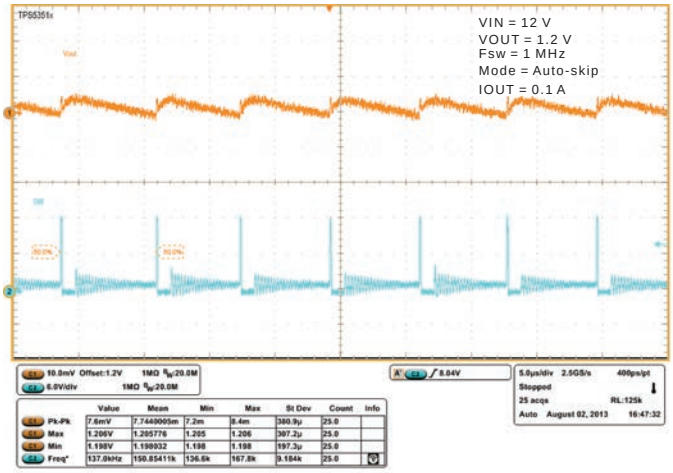

Figure 15. Auto-Skip Steady-State Operation

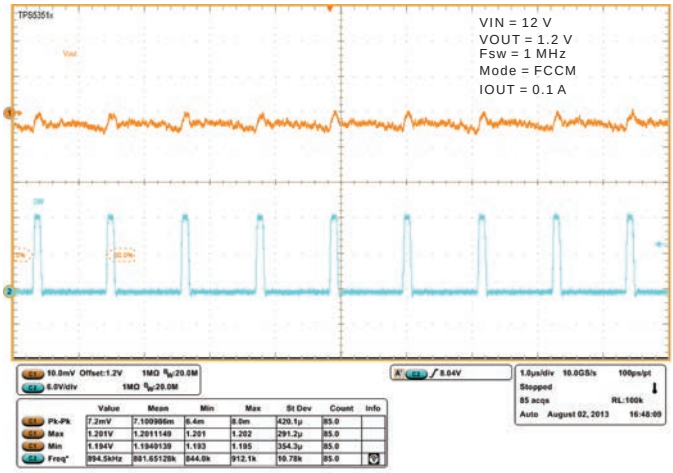

Figure 16. FCCM Steady-State Operation

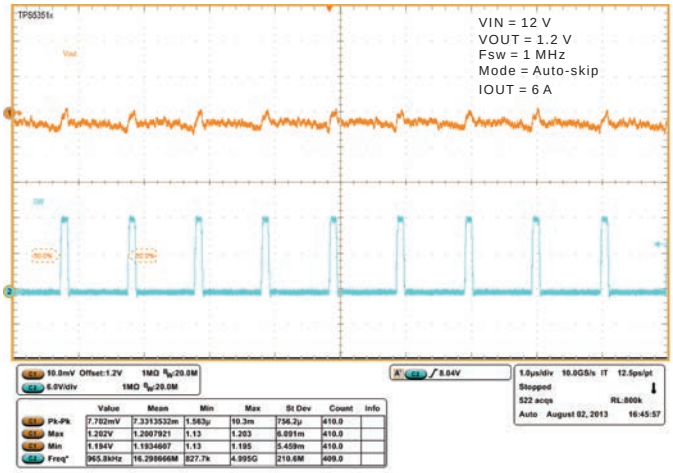

Figure 17. Auto-Skip Steady-State Operation

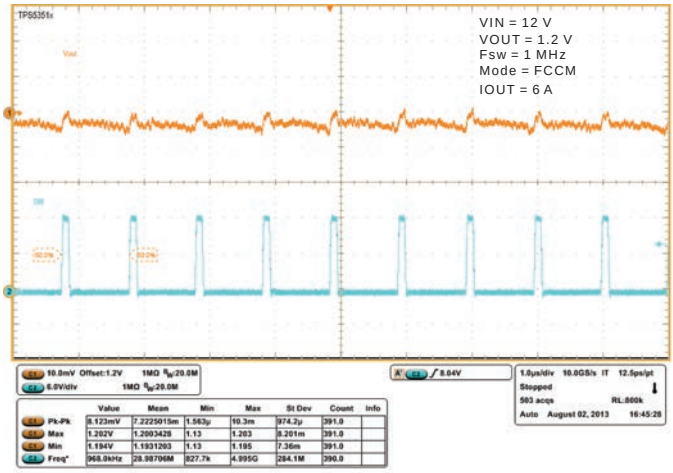

Figure 18. FCCM Steady-State Operation

TYPICAL CHARACTERISTICS (continued)

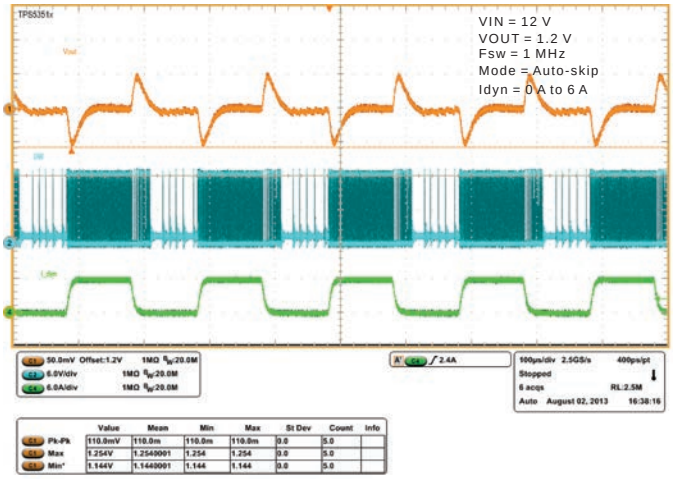

Figure 19. Auto-Skip Mode Load Transient

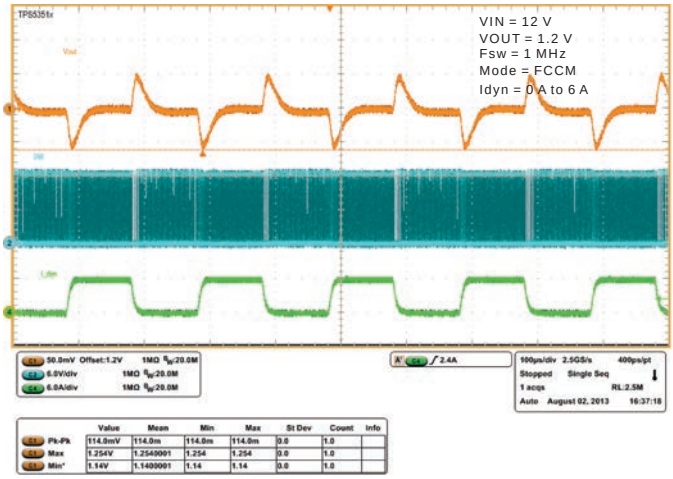

Figure 20.

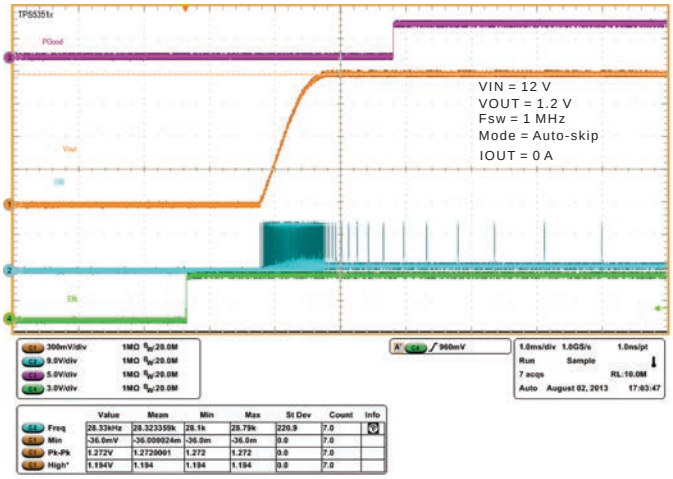

Figure 21. Start-Up

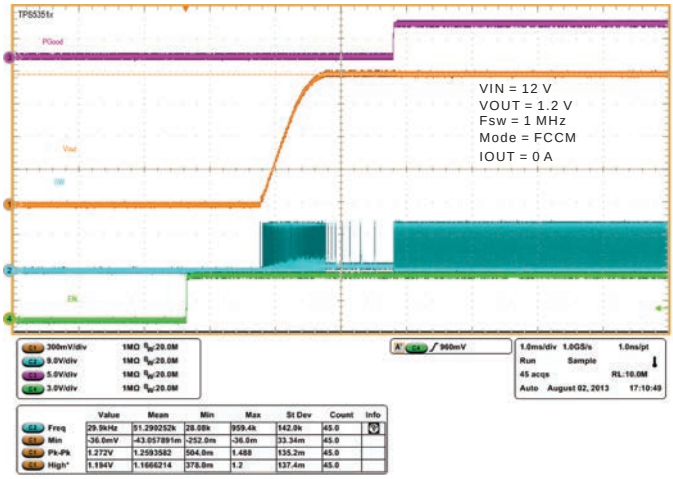

Figure 22. Start-Up

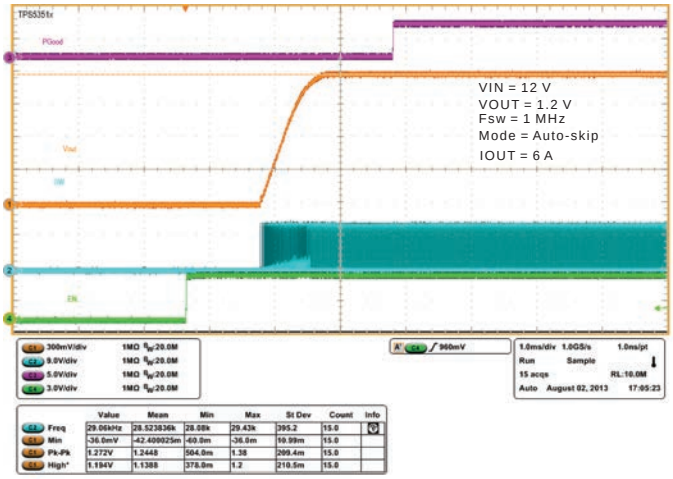

Figure 23. Start-Up

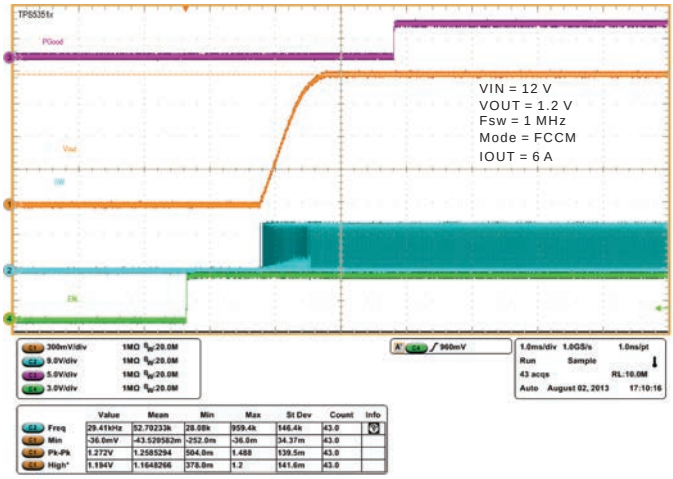

Figure 24. Start-Up

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TYPICAL CHARACTERISTICS (continued)

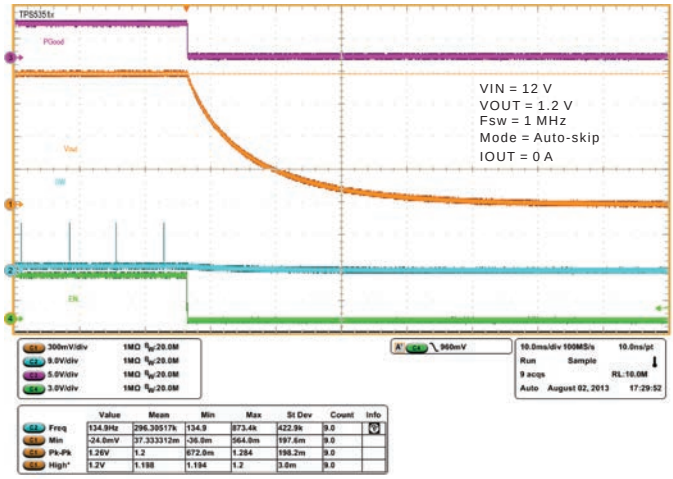

Figure 25. Shut-Down Operation

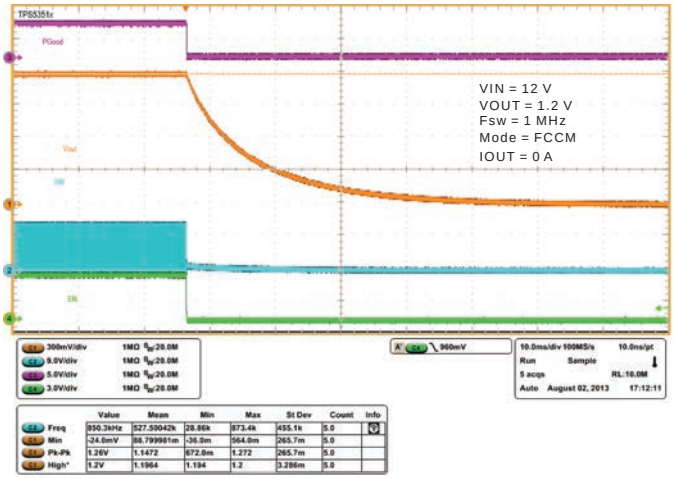

Figure 26. Shut-Down Operation

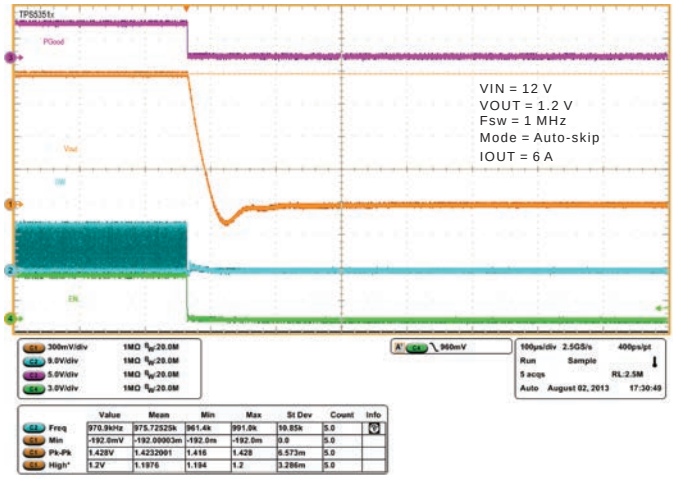

Figure 27. Shut-Down Operation

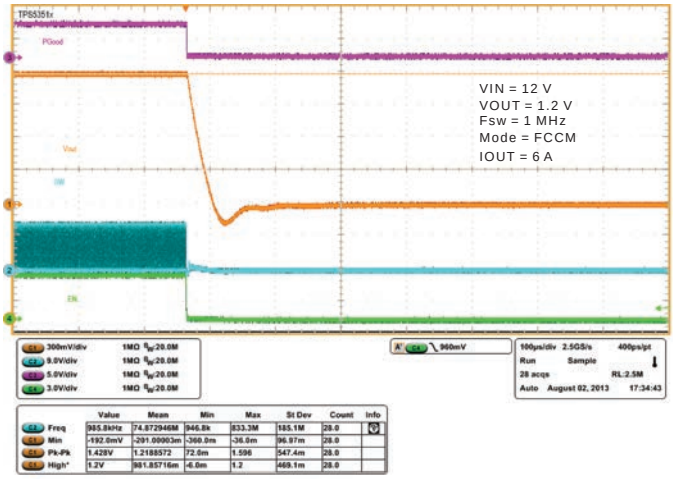

Figure 28. Shut-Down Operation

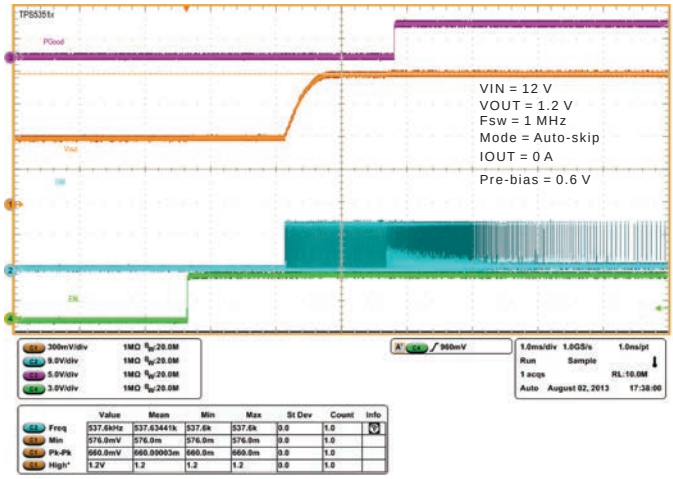

Figure 29. Pre-Bias Operation

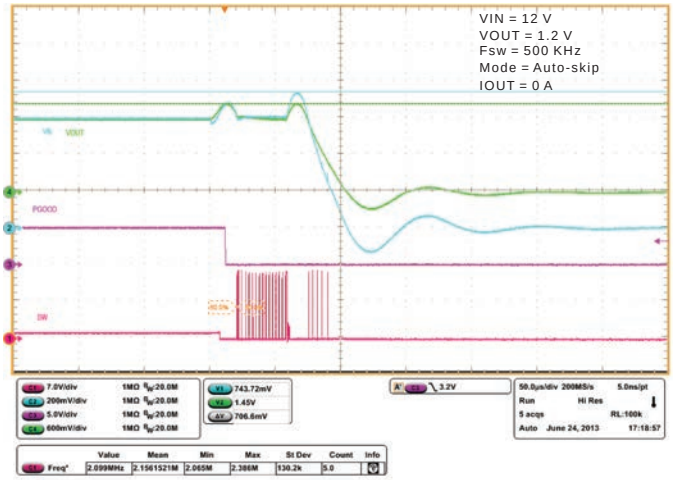

Figure 30. Overvoltage Protection

TYPICAL CHARACTERISTICS (continued)

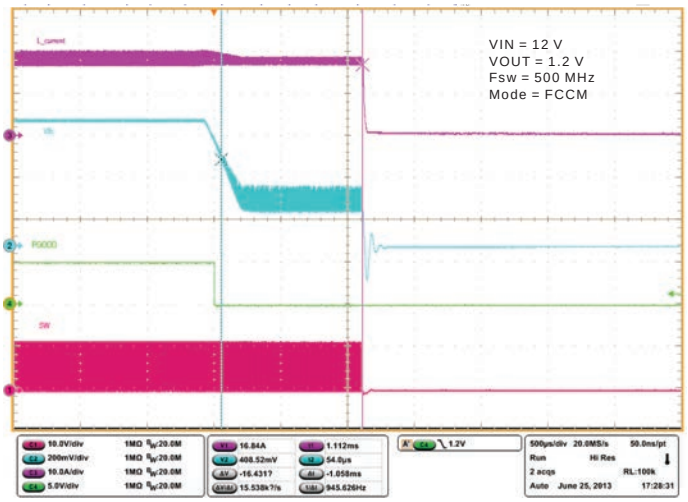

Figure 31. Overcurrent Protection

THERMAL PERFORMANCE

T_A = 23°C, f_{SW} = 500 kHz, V_{IN} = 12 V, V_{OUT} = 1.24 V, I_{OUT} = 8 A, R_{BOOT}= 0 Ω, SNB = 3 Ω + 470 pF

Inductor: L_{OUT} = 1 µH, PIMB103T-1R0MS-63, 10 mm × 11.2 mm × 3 mm, 5.3 mΩ

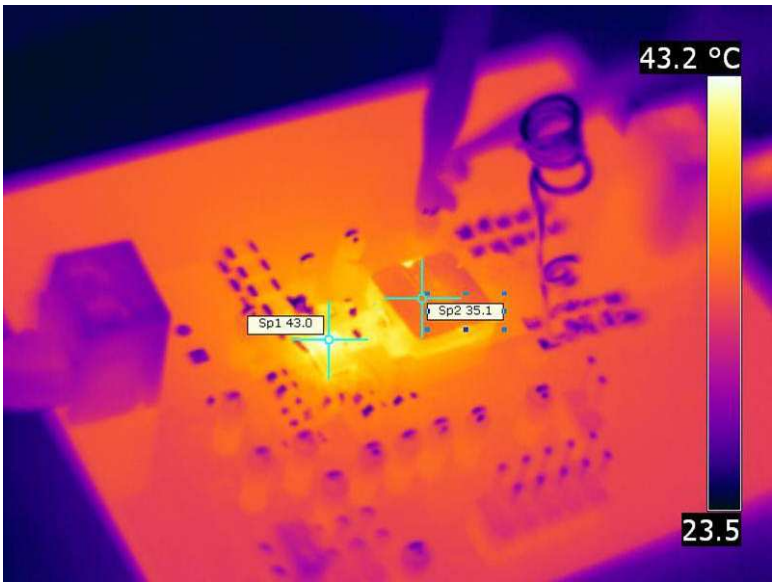

Figure 32. SP1: 43℃ (TPS53513), SP2: 35.1℃ (Inductor)

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APPLICATION INFORMATION

General Description

The TPS53513 is a high-efficiency, single-channel, synchronous-buck converter. The device suits low-output voltage point-of-load applications with 8-A or lower output current in computing and similar digital consumer applications. The TPS53513 features proprietary D-CAP3 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC-DC converters in an ideal fashion. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage ranges from 1.5 V to 18 V and the VDD input voltage ranges from 4.5 V to 25 V. The D-CAP3 mode uses emulated current information to control the modulation. An advantage of this control scheme is that it does not require a phase-compensation network outside which makes the device easy-to-use and also allows low-external component count. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltage while increasing switching frequency as needed during load-step transient.

Frequency Selection

TPS53513 allows users to select the switching frequency by using the RF pin. Table 1 lists the divider ratio and some example resistor values for the switching frequency selection. The 1% tolerance resistors with a typical temperature coefficient of ±100 ppm/ºC are recommended. If the design requires a tighter noise margin for more reliable SW-frequency detection, use higher performance resistors.

Table 1. Switching Frequency Selection

SWITCHING FREQUENCY (f_{SW}) (kHz)	RESISTOR DIVIDER RATIO (1) (R_{DR})	EXAMPLE RF FREQUENCY COMBINATIONS	
		R_{RF_H} (kΩ)	R_{RF_L} (kΩ)
1000	> 0.557	1	300
850	0.461	180	154
750	0.375	200	120
600	0.297	249	105
500	0.229	240	71.5
400	0.16	249	47.5
300	0.096	255	27
250	< 0.041	270	11.5

(1) Resistor divider ratio (R_{DR}) is described in Equation 1.

$$R_{DR} = \frac{R_{RF_L}}{\left(R_{RF_L} + R_{RF_H}\right)}$$

where

- R_{RF_L} is the low-side resistance of the RF pin resistor divider
- R_{RF_H} is the high-side resistance of the RF pin resistor divider (1)

D-CAP3 Control and Mode Selection

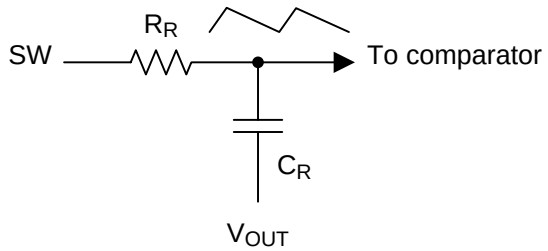

Figure 33. Internal RAMP Generation Circuit

The TPS53513 uses D-CAP3 mode control to achieve fast load transient while maintaining the ease-of-use feature. An internal RAMP is generated and fed to the VFB pin to reduce jitter and maintain stability. The amplitude of the ramp is determined by the R-C time-constant as shown in Figure 33. At different switching frequencies, (f_{SW}) the R-C time-constant varies to maintain relatively constant RAMP amplitude.

D-CAP3 Mode

From small-signal loop analysis, a buck converter using the D-CAP3 mode control architecture can be simplified as shown in Figure 34.

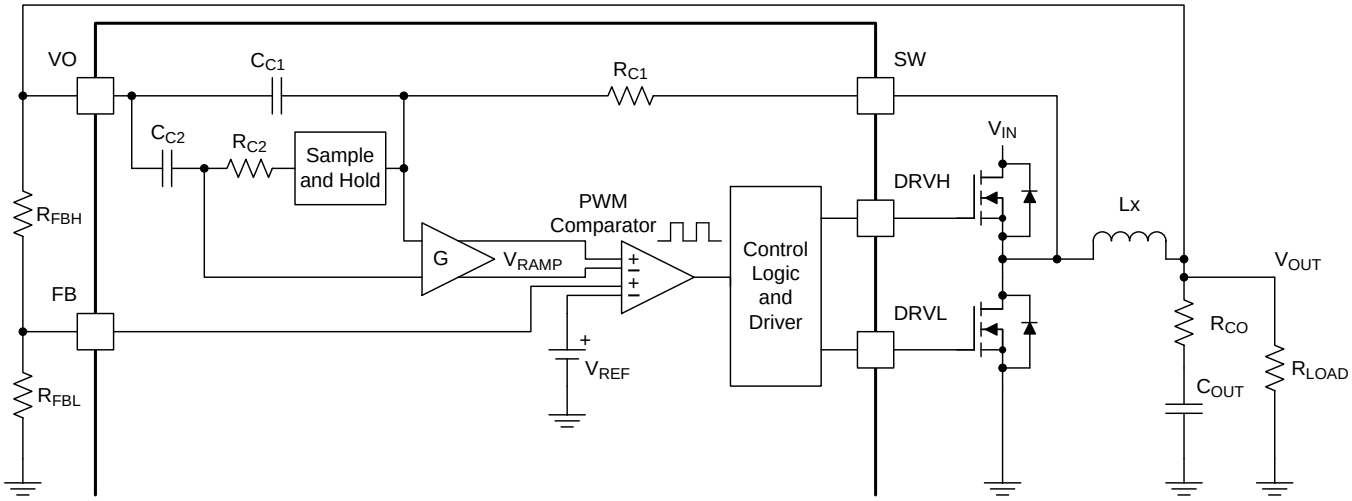

Figure 34. D-CAP3 Mode

The D-CAP3 control architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). No external current sensing network or voltage compensators are required with D-CAP3 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine it with the voltage feedback signal to regulate the loop operation. For any control topologies supporting no external compensation design, there is a minimum and/or maximum range of the output filter it can support. The output filter used with the TPS53513 is a lowpass L-C circuit. This L-C filter has double pole that is described in Equation 2.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{2}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS53513. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency.

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The inductor and capacitor selected for the output filter must be such that the double pole of Equation 2 is located close enough to the high-frequency zero so that the phase boost provided by the high-frequency zero provides adequate phase margin for the stability requirement.

Table 2. Locating the Zero

SWITCHING FREQUENCIES (f_{SW}) (kHz)	ZERO (f_Z) LOCATION (kHz)
250 and 300	6
400 and 500	7
600 and 750	9
850 and 1000	12

After identifying the application requirements, the output inductance should be designed so that the inductor peak-to-peak ripple current is approximately between 25% and 35% of the $I_{CC(max)}$ (peak current in the application). Use Table 2 to help locate the internal zero based on the selected switching frequency. In general, where reasonable (or smaller) output capacitance is desired, Equation 3 can be used to determine the necessary output capacitance for stable operation.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = f_Z \tag{3}$$

If MLCC is used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10-µF, X5R and 6.3 V, the deratings by DC bias and AC bias are 80% and 50% respectively. The effective derating is the product of these two factors, which in this case is 40% and 4-µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the system/applications.

Table 3 shows the recommended output filter range for an application design with the following specifications:

- Input voltage, V_{IN} = 12 V
- Switching frequency, f_{SW} = 600 kHz
- Output current, I_{OUT} = 8 A

The minimum output capacitance is verified by the small signal measurement conducted on the EVM using the following two criteria:

- Loop crossover frequency is less than one-half the switching frequency (300 kHz)
- Phase margin at the loop crossover is greater than 50 degrees

For the maximum output capacitance recommendation, simplify the procedure to adopt an unrealistically high output capacitance for this type of converter design, then verify the small signal response on the EVM using the following one criteria:

- Phase margin at the loop crossover is greater than 50 degrees

As indicated by the phase margin, the actual maximum output capacitance ($C_{OUT(max)}$) can continue to go higher. However, small signal measurement (bode plot) should be done to confirm the design.

Select a MODE pin configuration as shown in Table 3 to double the R-C time-constant option for the maximum output capacitance design and application. Select a MODE pin configuration to use single R-C time constant option for the normal (or smaller) output capacitance design and application.

The MODE pin also selects Skip-mode or FCCM-mode operation.

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Table 3. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF) (1)	CROSS-OVER (kHz)	PHASE MARGIN (°)	$C_{OUT(max)}$ (µF) (1)	INTERNAL RC SETTING (µs)	INDUCTOR $\Delta I/I_{CC(max)}$	$I_{CC(max)}$ (A)
0.6	10	0	0.36 PIMB065T-R36MS	3 × 100	247	70		40	33%	8
					48	62	30 x 100	80		
1.2		10	0.68 PIMB065T-R68MS	9 × 22	207	53		40	33%	
					25	84	30 x 100	80		
2.5		31.6	1.2 PIMB065T-1R2MS	4 × 22	185	57		40	34%	
					11	63	30 x 100	80		
3.3		45.3	1.5 PIMB065T-1R5MS	3 × 22	185	57		40	33%	
					9	59	30 x 100	80		
5.5		82.5	2.2 PIMB065T-2R2MS	2 × 22	185	51		40	28%	
					7	58	30 x 100	80		

(1) All $C_{OUT(min)}$ and $C_{OUT(max)}$ capacitor specifications are 1206, X5R, 10 V.

For higher output voltage at or above 2.0 V, additional phase boost might be required in order to secure sufficient phase margin due to phase delay/loss for higher output voltage (large on-time (t_{ON})) setting in a fixed on time topology based operation.

A feedforward capacitor placing in parallel with R_{UPPER} is found to be very effective to boost the phase margin at loop crossover. Refer to TI application note SLVA289 for details.

Table 4. Mode Selection and Internal RAMP R-C Time Constant

MODE SELECTION	ACTION	R_{MODE} (kΩ)	R-C TIME CONSTANT (µs)	SWITCHING FREQUENCIES f_{SW} (kHz)
Skip Mode	Pull down to GND	0	60	275 and 325
			50	425 and 525
			40	625 and 750
			30	850 and 1000
		150	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000
FCCM (1)	Connect to PGOOD	20	60	275 and 325
			50	425 and 525
			40	625 and 750
			30	850 and 1000
		150	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000
FCCM	Connect to VREG	0	120	275 and 325
			100	425 and 525
			80	625 and 750
			60	850 and 1000

(1) Device goes into Forced CCM (FCCM) after PGOOD becomes high.

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Sample and Hold Circuitry

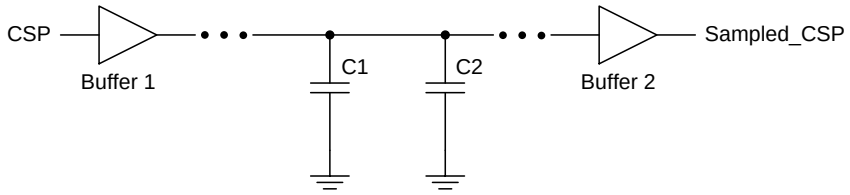

Figure 35. Sample and Hold Logic Circuitry (Patent Pending)

The sample and hold circuitry is the difference between D-CAP3 and D-CAP2. The sample and hold circuitry, which is an advance control scheme to boost output voltage accuracy higher on the TPS53513, is one of features of the TPS53513. The sample and hold circuitry generates a new DC voltage of CSN instead of the voltage which is produced by R_{C2} and C_{C2} which allows for tight output-voltage accuracy and makes the TPS53513 more competitive.

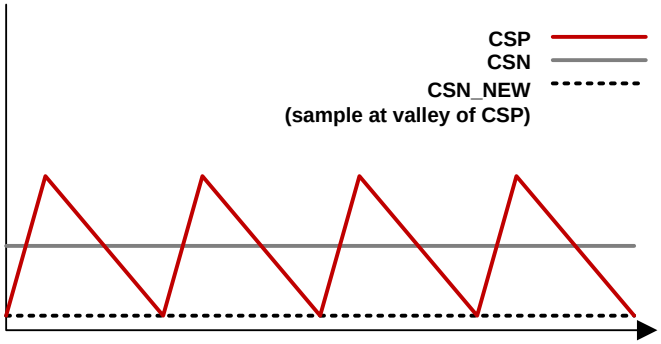

Figure 36. Continuous Conduction Mode (CCM) With Sample and Hold Circuitry

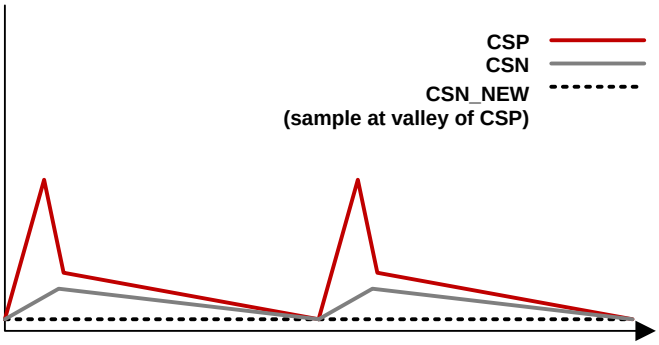

Figure 37. Discontinuous Conduction Mode (DCM) With Sample and Hold Circuitry

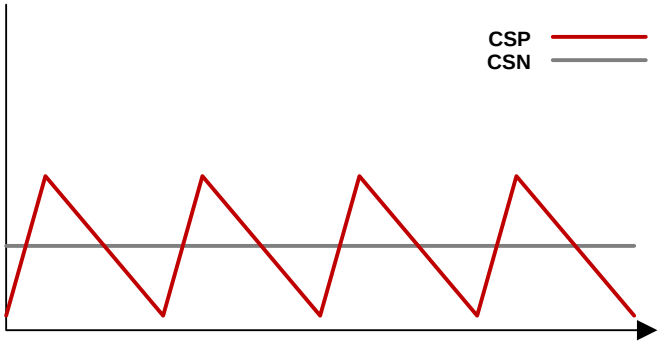

Figure 38. Continuous Conduction Mode (CCM) Without Sample and Hold Circuitry

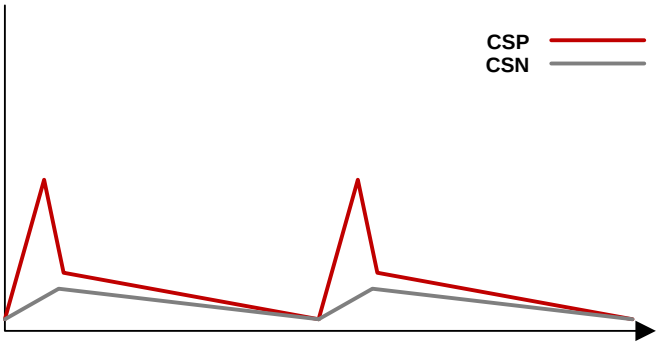

Figure 39. Discontinuous Conduction Mode (DCM) Without Sample and Hold Circuitry

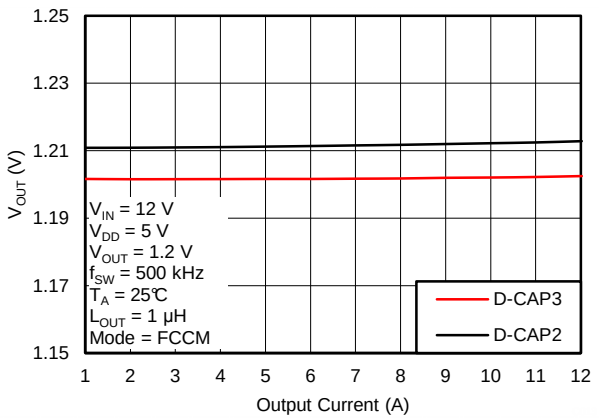

Figure 40. Output Voltage vs Output Current

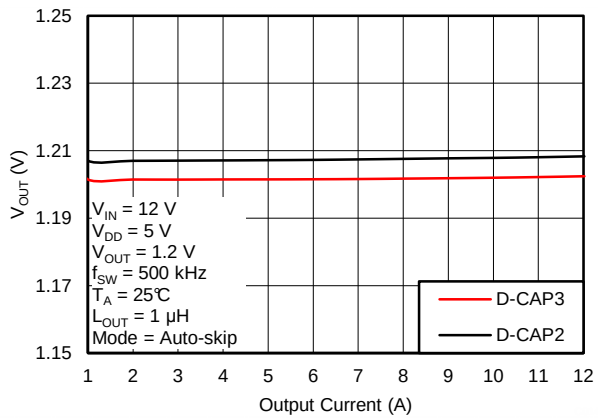

Figure 41. Output Voltage vs Output Current

Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled to GND directly or via 150-kΩ resistor, the TPS53513 automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the light-load operation $I_{O(LL)}$ (for example: the threshold between continuous- and discontinuous-conduction mode) is calculated as shown in Equation 4.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f_{SW} is the PWM switching frequency (4)

Using only ceramic capacitors is recommended for Auto-skip mode.

Adaptive Zero-Crossing

The TPS53513 uses an adaptive zero-crossing circuit to perform optimization of the zero inductor-current detection during skip-mode operation. This function allows ideal low-side MOSFET turn-off timing. The function also compensates the inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. Adaptive zero-crossing prevents SW-node swing-up caused by too-late detection and minimizes diode conduction period caused by too-early detection. As a result, the device delivers better light-load efficiency.

Forced Continuous-Conduction Mode

When the MODE pin is tied to the PGOOD pin through a resistor, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an amost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency at the cost of lower efficiency.

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Power-Good

The TPS53513 has power-good output that indicates high when switcher output is within the target. The power-good function is activated after the soft-start operation is complete. If the output voltage becomes within ±8% of the target value, internal comparators detect the power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of ±16% of the target value, the power-good signal becomes low after a 2-µs internal delay. The power-good output is an open-drain output and must be pulled-up externally.

Current Sense and Overcurrent Protection

The TPS53513 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the period that the inductor current is larger than the overcurrent trip level. In order to provide good accuracy and a cost-effective solution, the TPS53513 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. Connect the TRIP pin to GND through the trip-voltage setting resistor, R_{TRIP}. The TRIP terminal sources I_{TRIP} current, which is 10 µA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in Equation 5.

$$V_{TRIP} = R_{TRIP} \times I_{TRIP}$$

where

- V_{TRIP} is in mV
- R_{TRIP} is in kΩ
- I_{TRIP} is in µA (5)

The inductor current is monitored by the voltage between the GND pin and SW pin so that the SW pin is properly connected to the drain terminal of the low-side MOSFET. I_{TRIP} has a 3000-ppm/°C temperature slope to compensate the temperature dependency of $R_{DS(on)}$. The GND pin acts as the positive current-sensing node. Connect the GND pin to the proper current sensing device, (for example, the source terminal of the low-side MOSFET.)

Because the comparison occurs during the OFF state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, is calculated as shown in Equation 6.

$$I_{OCP} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(8 \times R_{DS(on)L}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}}$$

where

- $R_{DS(on)L}$ is the on-resistance of the low-side MOSFET
- R_{TRIP} is in kΩ (6)

Equation 6 calculates the typical DC OCP level (typical low-side on-resistance [$R_{DS(on)}$] of 5.9 mΩ should be used); in order to design for worst case minimum OCP, maximum low-side on-resistance value of 8 mΩ should be used.

During an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, the output voltage crosses the undervoltage-protection threshold and shuts down.

For the TPS53513, the overcurrent protection maximum is recommended up to 12 A only.

Overvoltage and Undervoltage Protection

The TPS53513 monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes lower than 68% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1 ms, the TPS53513 latches OFF both high-side and low-side MOSFETs drivers. The UVP function enables after soft-start is complete.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and turns on the low-side MOSFET until reaching a negative current limit. Upon reaching the negative current limit, the low-side FET is turned off and the high-side FET is turned on again for a minimum on-time. The TPS53513 operates in this cycle until the output voltage is pulled down under the UVP threshold voltage for 1 ms. After the 1-ms UVP delay time, the high-side FET is latched off and low-side FET is latched on. The fault is cleared with a reset of VDD or by re-toggling EN pin.

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Out-Of-Bounds Operation (OOB)

The TPS53513 has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, so the device is not latched off after an OOB event. OOB protection operates as an early no-fault overvoltage-protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly towards the setpoint. During the operation, the cycle-by-cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

UVLO Protection

The TPS53513 monitors the voltage on the VDD pin. If the VDD pin voltage is lower than the UVLO off-threshold voltage, the switch mode power supply shuts off. If the VDD voltage increases beyond the UVLO on-threshold voltage, the controller turns back on. UVLO is a non-latch protection.

Thermal Shutdown

The TPS53513 monitors internal temperature. If the temperature exceeds the threshold value (typically 140°C), TPS53513 shuts off. When the temperature falls approximately 40°C below the threshold value, the device turns on. Thermal shutdown is a non-latch protection.

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External Parts Selection

The external components selection is a simple process using D-CAP3™ Mode. Select the external components using the following steps

1. **CHOOSE THE SW FREQUENCY**

   The SW frequency is configured by the resistor divider on the RF pin. Select one of eight SW frequencies from 250 kHz to 1 MHz. Refer Table 1 for the relationship between the SW frequency and resistor-divider configuration.

2. **CHOOSE THE OPERATION MODE**

   Select the operation mode using Table 4.

3. **CHOOSE THE INDUCTOR**

   Determine the inductance value to set the ripple current at approximately ¼ to ½ of the maximum output current. Larger ripple current increases output ripple voltage, improves S/N ratio, and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (7)$$

   The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The peak inductor current is estimated using Equation 8.

$$I_{IND(peak)} = \frac{V_{TRIP}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (8)$$

4. **CHOOSE THE OUTPUT CAPACITOR**

   The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has two components as shown in Equation 9. Equation 10 and Equation 11 define these components.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} \quad (9)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (10)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (11)$$

5. **DETERMINE THE VALUE OF R1 AND R2**

   The output voltage is programmed by the voltage-divider resistors, R1 and R2, shown in APPLICATION CIRCUIT DIAGRAM. R1 is connected between the VFB pin and the output, and R2 is connected between the VFB pin and GND. The recommended R2 value is from 1 kΩ to 20 kΩ. Determine R1 using Equation 12.

$$R1 = \frac{V_{OUT} - 0.6}{0.6} \times R2 \quad (12)$$

LAYOUT CONSIDERATIONS

Before beginning a design using the TPS53513, consider the following:

- Place the power components (including input and output capacitors, the inductor, and the TPS53513) on the solder side of the PCB. In order to shield and isolate the small signal traces from noisy power lines, insert and connect at least one inner plane to ground.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE, and RF must be placed away from high-voltage switching nodes such as SW and VBST to avoid coupling. Use internal layers as ground planes and shield the feedback trace from power traces and components.
- GND (pin 22) must be connected directly to the thermal pad. Connect the thermal pad to the PGND pins and then to the GND plane.
- The GND1 pin (pin 27) and the GND2 pin (pin 28) are not actual GND pins and neither of these pins should be used for dedicated ground connection. The recommendation is to connect GND1 pin (pin 27) and the GND2 pin (pin 28) to the nearby ground.

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- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC-current loop.
- Place the feedback resistor near the device to minimize the VFB trace distance.
- Place the frequency-setting resistor (R_{RF}), OCP-setting resistor (R_{TRIP}) and mode-setting resistor (R_{MODE}) close to the device. Use the common GND via to connect the resistors to the GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Provide GND vias for each decoupling capacitor and ensure the loop is as small as possible.
- The PCB trace is defined as switch node, which connects the SW pins and high-voltage side of the inductor. The switch node should be as short and wide as possible.
- Use separated vias or trace to connect SW node to the snubber, bootstrap capacitor, and ripple-injection resistor. Do not combine these connections.
- Place one more small capacitor (2.2 nF- 0402 size) between the VIN and PGND pins. This capacitor must be placed as close to the device as possible.
- TI recommends placing a snubber between the SW shape and GND shape for effective ringing reduction. The value of snubber design starts at 3 Ω + 470 pF.
- Consider R,C,Cc network (Ripple injection network) component placement and place the AC coupling capacitor, Cc, close to the device, and R and C close to the power stage.
- See Figure 42 for the layout recommendation.

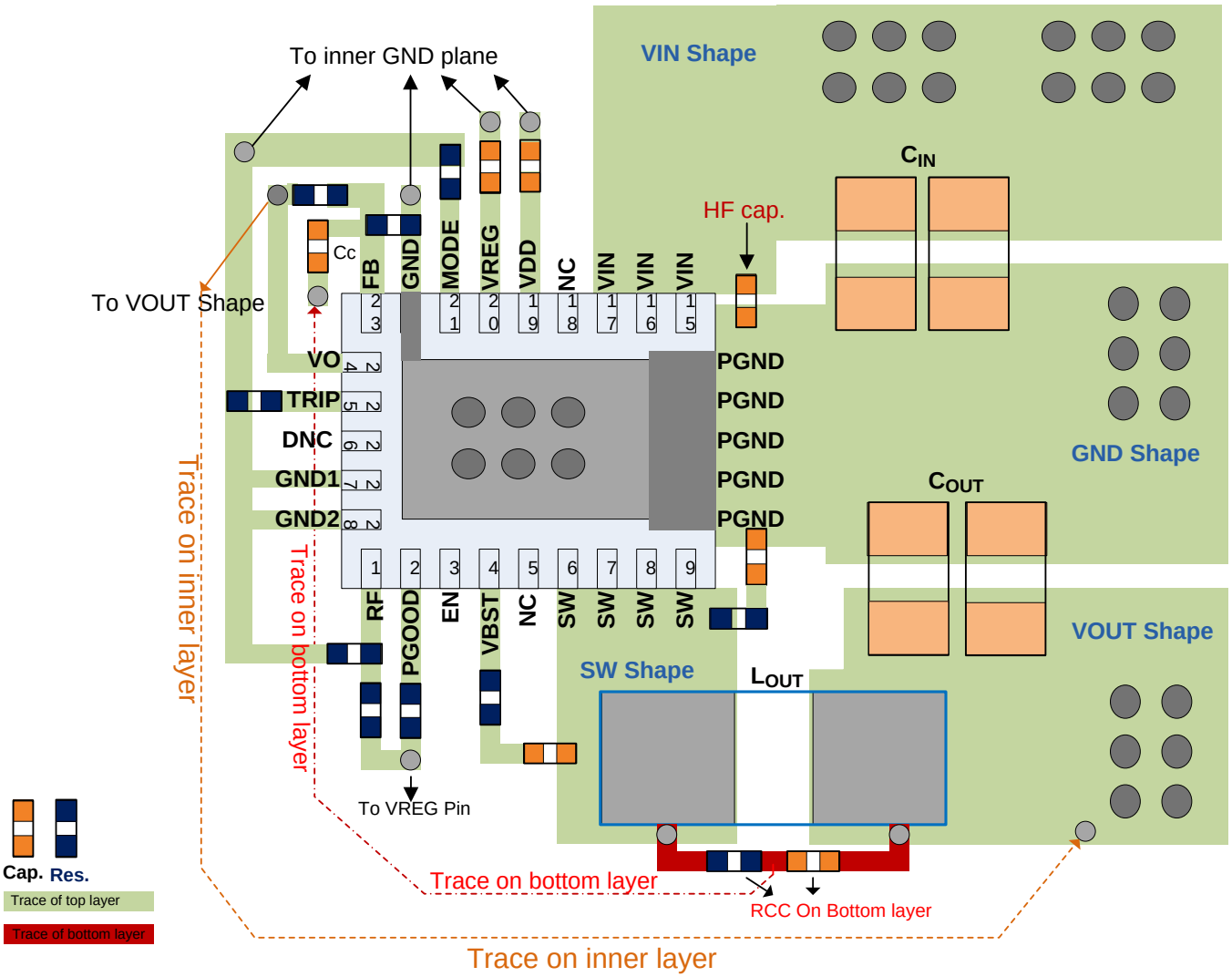

Figure 42. Layout Recommendation

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REVISION HISTORY

Changes from Original (SEPTEMBER 2013) to Revision A	Page
• Added updates to FEATURES, APPLICATIONS, DESCRIPTION and front page graphics	1
• Changed device dimensions from 3,5 mm × 4,5 mm to 3.5 mm × 4.5 mm	1
• Added updates to Electrical Specifications	2
• Added updates to Electrical Specifications	3
• Added updates to PIN DESCRIPTIONS	5
• Added updates to BLOCK DIAGRAM	7
• Added THERMAL PERFORMANCE section	14
• Added updates to APPLICATION INFORMATION section	15

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53513RVER	ACTIVE	VQFN	RVE	28	3000	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS53513	Samples
TPS53513RVET	ACTIVE	VQFN	RVE	28	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS53513	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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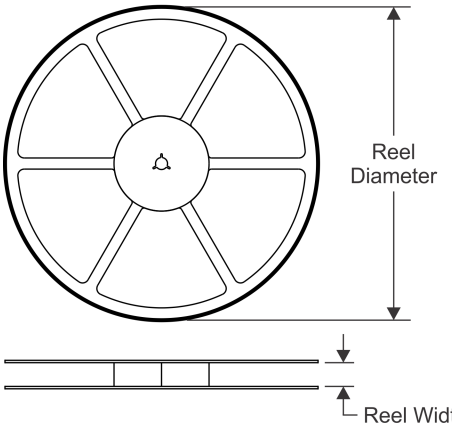
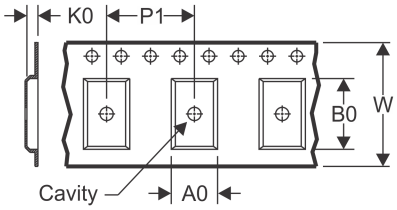
TAPE AND REEL INFORMATION

REEL DIMENSIONS

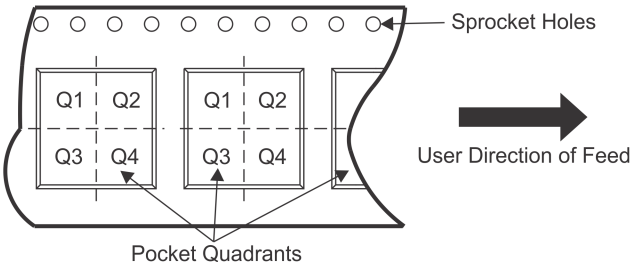


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

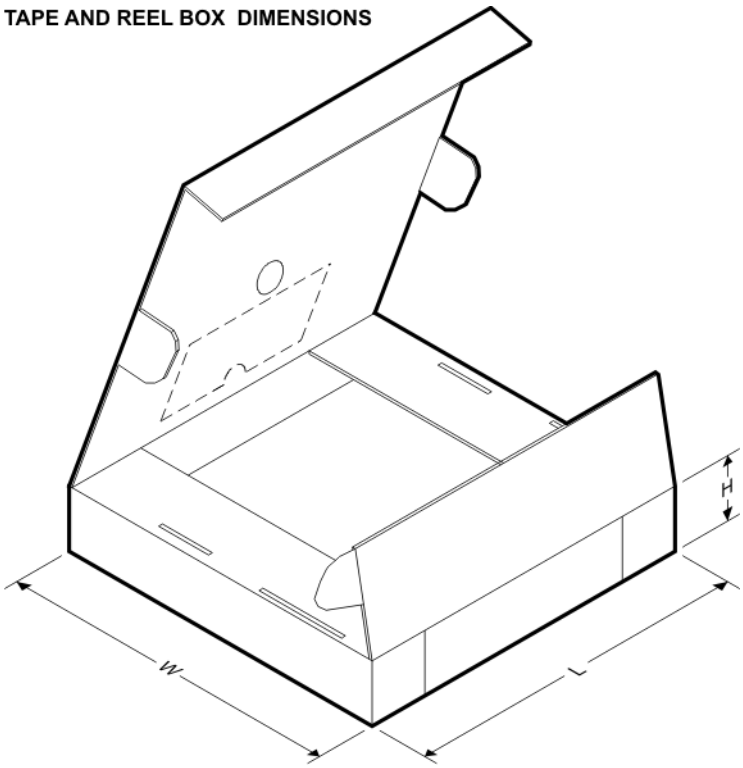
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53513RVER	VQFN	RVE	28	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TPS53513RVET	VQFN	RVE	28	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

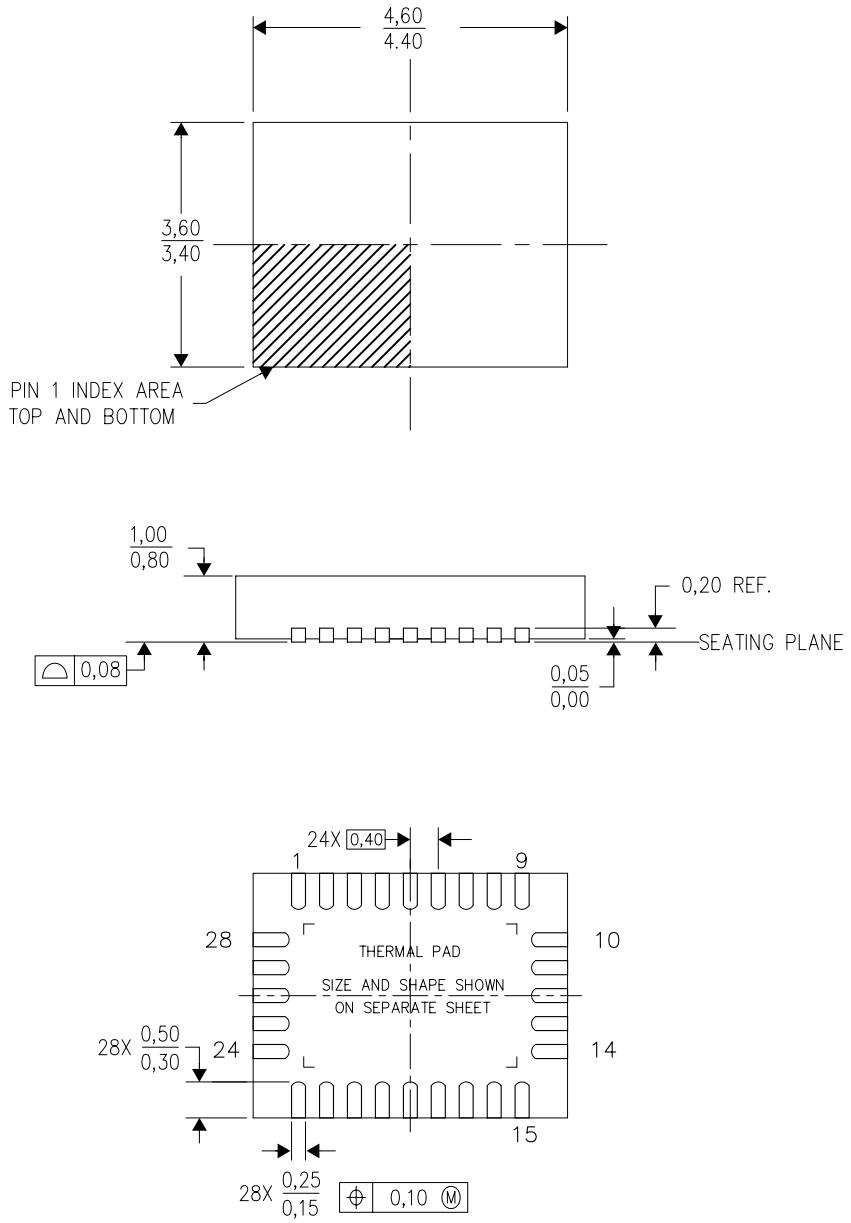
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53513RVER	VQFN	RVE	28	3000	367.0	367.0	35.0
TPS53513RVET	VQFN	RVE	28	250	210.0	185.0	35.0

RVE (R-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-220.

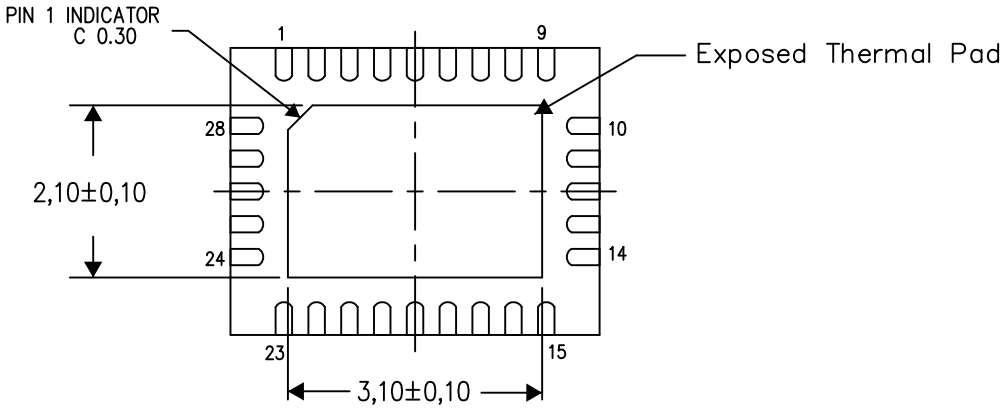
RVE (R–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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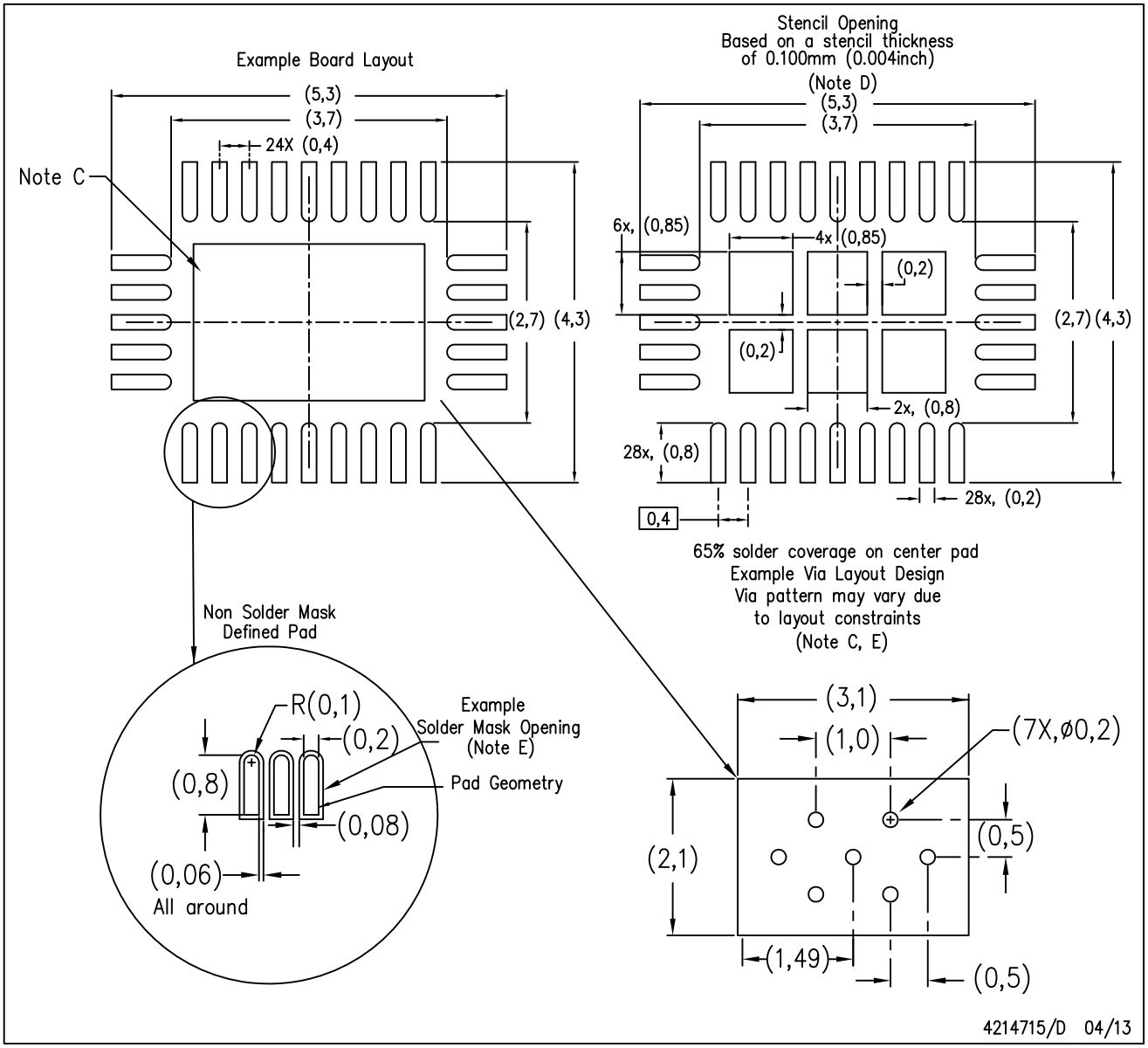
NOTE: All linear dimensions are in millimeters

RVE (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Electroformed stencils offer adequate release at thicker values/lower Area Ratios. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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