Mar. 16, 2007

Preliminary

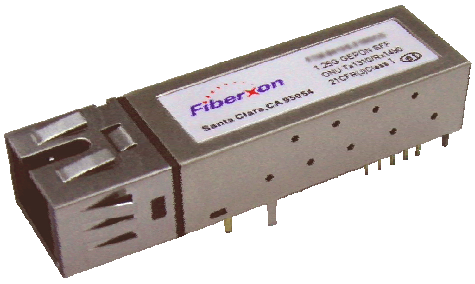
2x5 SFF GEPON ONU Diplexer

FTM-9412S-F20F(G)

FTM-9412S-F20FD(G)

(IEEE 802.3ah™-2004 1000BASE-PX20-U)

Members of Flexon™ Family



Standard

- Compliant with SFF MSA
- Compliant with IEEE Std 802.3ah™ -2004 1000BASE-PX20-U
- Compliant with FCC 47 CFR Part 15, Class B
- Compliant with FDA 21 CFR 1040.10 and 1040.11, Class I

Features

- Single fiber bi-directional data links with symmetric 1.25Gbps upstream and 1.25Gbps downstream
- Integrated with micro-optics WDM filter for dual wavelength Tx/Rx operation at 1310/1490nm
- 1310nm burst-mode transmitter with FP laser
- 1490nm continuous-mode receiver with PIN-TIA
- 1550nm optical signal rejection
- 0 to 70℃ operating case temperature
- 2×5 SFF package with SC receptacle form
- Single 3.3V power supply
- LVPECL compatible data input/output interface
- LVTTL transmitter burst-mode control
- LVTTL receiver signal-detected indication
- Low EMI and excellent ESD protection
- Class I laser safety standard IEC-60825 compliant

Description

FTM-9412S-F20F(G)/F20FD(G) is Optical Network Unit (ONU) for IEEE802.3ah™-2004 1000BASE-PX20-U application.

The transceiver is the high performance module for 1.25Gbps data link in single fiber by using 1310nm burst-mode transmitter and 1490nm continuous-mode receiver with 1550nm optical signal rejection.

The transmitter section uses a multiple quantum well 1310nm FP laser and is Class Ⅰ laser compliant product according to international safety standard IEC-60825.

The receiver section uses an integrated 1490nm PIN and preamplifier mounted in an optical header and limiting post-amplifier IC.

The optical burst output can be enabled by a LVTTL logic high-level input of TX_BRST. Signal Detected (SD) output is provided to indicate the detection of an input optical signal of receiver.

Applications

- Gigabit Ethernet Passive Optical Networks (GEPON) – ONU side
- Gigabit Ethernet Point-to-Point Bi-directional Transmission
- Media Converts for Fiber-In-The-Loop (FITL)

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Regulatory Compliance

The transceivers have been tested according to American and European product safety and electromagnetic compatibility regulations (See Table 1). For further information regarding regulatory certification, please refer to Flexon™ regulatory specification and safety guidelines, or contact with Fiberxon, Inc. America sales office listed at the end of documentation.

Table 1 - Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class Ⅰ(>500 V)
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B	Compliant with standards
Immunity	IEC 61000-4-3	Compliant with standards
Laser Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1,2	Compliant with Class I laser product
Component Recognition	UL and CSA	Compliant with standards

Absolute Maximum Ratings

Absolute Maximum Ratings are those values, beyond which, some damages may occur to the devices. Exposure to conditions above the Absolute Maximum Ratings listed in Table 2 may negatively impact the reliability of the products.

Table 2 - Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Ambient Temperature	T_{STG}	-40	85	°C	
Operating Case Temperature	T_C	0	70	°C	
Operating Humidity	H_{OPR}	5	95	%	
Power Supply Voltage	V_{CC}	0	4	V	
Input Voltage		GND	Vcc	V	
Receiver Damaged Threshold		+7		dBm	
Soldering Temperature			260/10	°C/s	1
			400	°C	2

Note 1: Soldering on lead only, for FTM-9412S-F20FG and FTM-9412S-F20FDG

Note 2: Only for soldering by iron and 10 seconds on leads only, for FTM-9412S-F20F and FTM-9412S-F20FD

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Recommended Operating Conditions

Table 3 - Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	3.3V±5%
Operating Case Temperature	T_C	0		70	°C	
Operating Humidity Range	H_{OPR}	5		95	%	
Data Rate			1.25		Gbit/s	
Data Rate Drift		-100		+100	PPM	

Optical and Electrical Characteristics

Table 4 - Transmitter Optical and Electrical Characteristics (0°C <T_C<70°C and 3.13V<V_{CC}<3.47V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Optical Center Wavelength	λ_C	1276		1356	nm	
Optical Spectrum Width (RMS)	$\Delta\lambda$			2.8	nm	
Average Launch Power	P_{OUT}	0		+4	dBm	1
Average Launch Power-OFF Transmitter	P_{OFF}			-45	dBm	
Extinction Ratio	ER	9			dB	2
Total Jitter	TJ			0.35	UI	
Rise/Fall Time (20%-80%)	T_R/T_F			260	ps	2.3
Burst Turn On Time	T_{BURST_ON}			30	ns	4
Burst Turn Off Time	T_{BURST_OFF}			30	ns	
Burst Enable Duration	T_{EN_DUR}	600			ns	
Burst Disable Duration	T_{DIS_DUR}	100			ns	
$RIN_{15}OMA$				-115	dB/Hz	
Optical Return Loss Tolerance				15	dB	
Transmitter Reflectance				-10	dB	
Optical Eye Diagram	Compliant With IEEE Std 802.3ah™-2004					2,5
Data Input Differential Swing	V_{IN}	200		1600	mV	6
Common-Mode Input Voltage	V_{CM}	V_{CC}-1.49	V_{CC}-1.32	V_{CC}- V_{IN}/4	V	7
Input Differential Impedance	Z_{IN}	90	100	110	Ω	
Power Supply Current	I_{CC_TX}			200	mA	
Transmitter Burst Control Voltage - Low	$V_{TDIS,\ L}$	0		0.8	V	8
Transmitter Burst Control Voltage -High	$V_{TDIS,\ H}$	2.0		V_{CC}	V	

Note 1: Launched into 9/125um Single Mode Fiber.

Note 2: Measured with PRBS 2^7-1 test pattern @1.25 Gbit/s.

Note 3: Measured with the Bessel-Thompson filter OFF.

Note 4: Refer to Timing Parameter Definition in Burst Mode Sequence.

Note 5: Transmitter eye mask definition is {0.22UI, 0.375UI, 0.20UI, 0.20UI, 0.30UI}.

Note 6: Compatible with LVPECL/CML input, AC coupled internally. (See Recommended Interface Circuit)

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Note 7: Only for FTM-9412S-F20FD(G)

Note 8: TX_BRST (See Pin Function Definitions)

Table 5 - Receiver Optical and Electrical Characteristics (0°C <T_C<70°C and 3.13V<V_{CC}<3.47V)

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Wavelength		1480		1500	nm	
Sensitivity	P_{SEN}			-26.5	dBm	1
Saturation	P_{SAT}	-3			dBm	
Signal-Detected Assert Level	P_{SDA}			-27	dBm	2
Signal-Detected Deassert Level	P_{SDD}	-39			dBm	3
Signal-Detected Hysteresis	P_{SDA}- P_{SDD}	0.5		6	dBm	
Receiver Reflectance				-12	dB	
WDM Filter Isolation	ISO(1550)	38			dB	1550nm
	ISO(1650)	35			dB	1650nm
Power Supply Current	I_{CC_RX}			120	mA	
Data Output Differential Swing	V_{OUT}	400		1600	mV	4
Signal-Detected Voltage - Low	$V_{SD,\ L}$	0		0.8	V	5
Signal-Detected Voltage - High	$V_{SD,\ H}$	2.0		V_{CC}	V	
Signal-Detected Assert Time	T_{ASS}			100	μs	
Signal-Detected Deassert Time	T_{DAS}			100	μs	

Note 1: Measured with a PRBS 2^7-1 test pattern @1.25Gbit/s and ER=9dB, BER =10^{-12}.

Note 2: An increase in optical power above the specified level will cause the Signal Detect output to switch from a low state to a high state.

Note 3: A decrease in optical power below the specified level will cause the Signal Detect output to switch from a high state to a low state.

Note 4: LVPECL output, AC coupled internally, guaranteed in the full range of input optical power (-3dBm to -27dBm) (See Recommended Interface Circuit)

Note 5: SD (See Pin Function Definitions)

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Table 6 - Electrical Input/Output Coupling Mode

P/N	Input (TD+/TD-)	Output (RD+/RD-)
FTM-9412S-F20F(G)	Internal AC Coupling	Internal AC Coupling
FTM-9412S-F20FD(G)	Internal DC Coupling	Internal AC Coupling

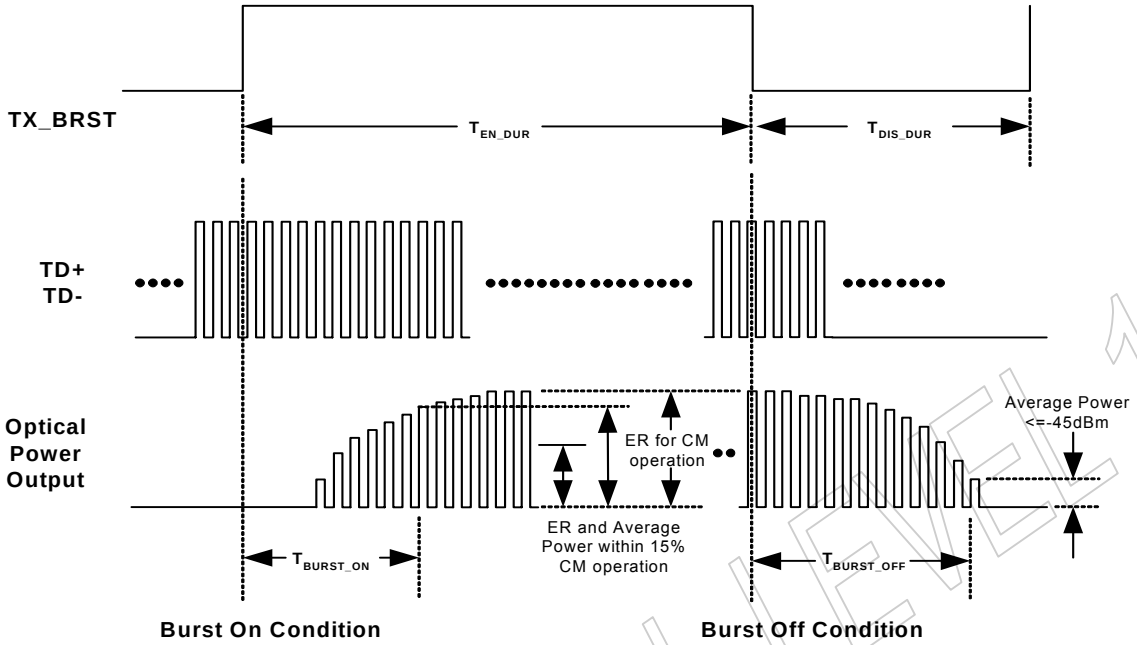

Figure 1 Timing Parameter Definition in Burst Mode Sequence

Recommended Interface Circuit

Figure 2 shows the recommended interface schemes for FTM-9412S-F20F(G)

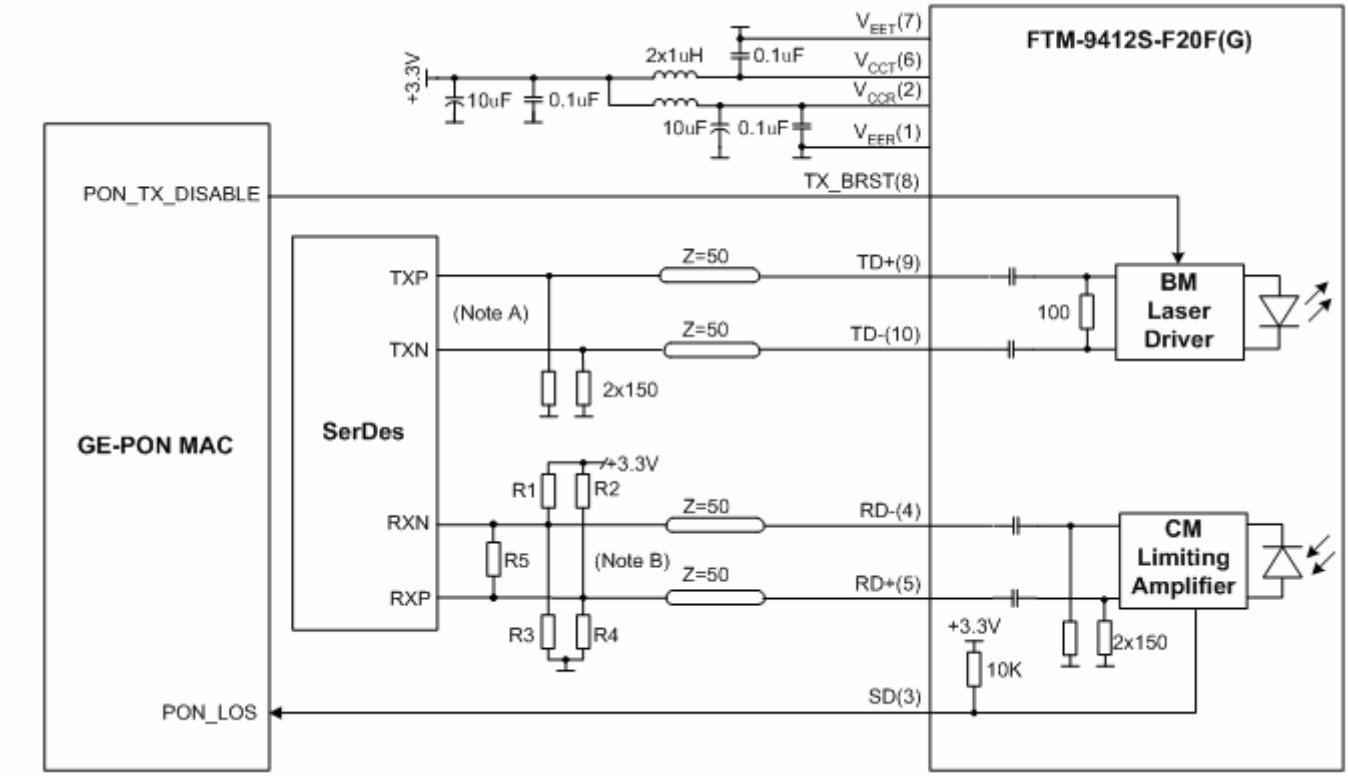

Figure 2 Recommended Interface Circuit (FTM-9412S-F20F(G))

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Note A: Open emitter output internally.

Note B: LVPECL output, AC coupled internally.

Input stage in SerDes IC is assumed with high impedance and internal bias to Vcc-1.3V

R1=R2=R3=R4=N.C, R5=100Ω

Input stage in SerDes IC is assumed without internal bias to Vcc-1.3V

R1=R2=82Ω,R3=R4=130Ω,R5=N.C

Figure 3 shows the recommended interface schemes for FTM-9412S-F20FD(G)

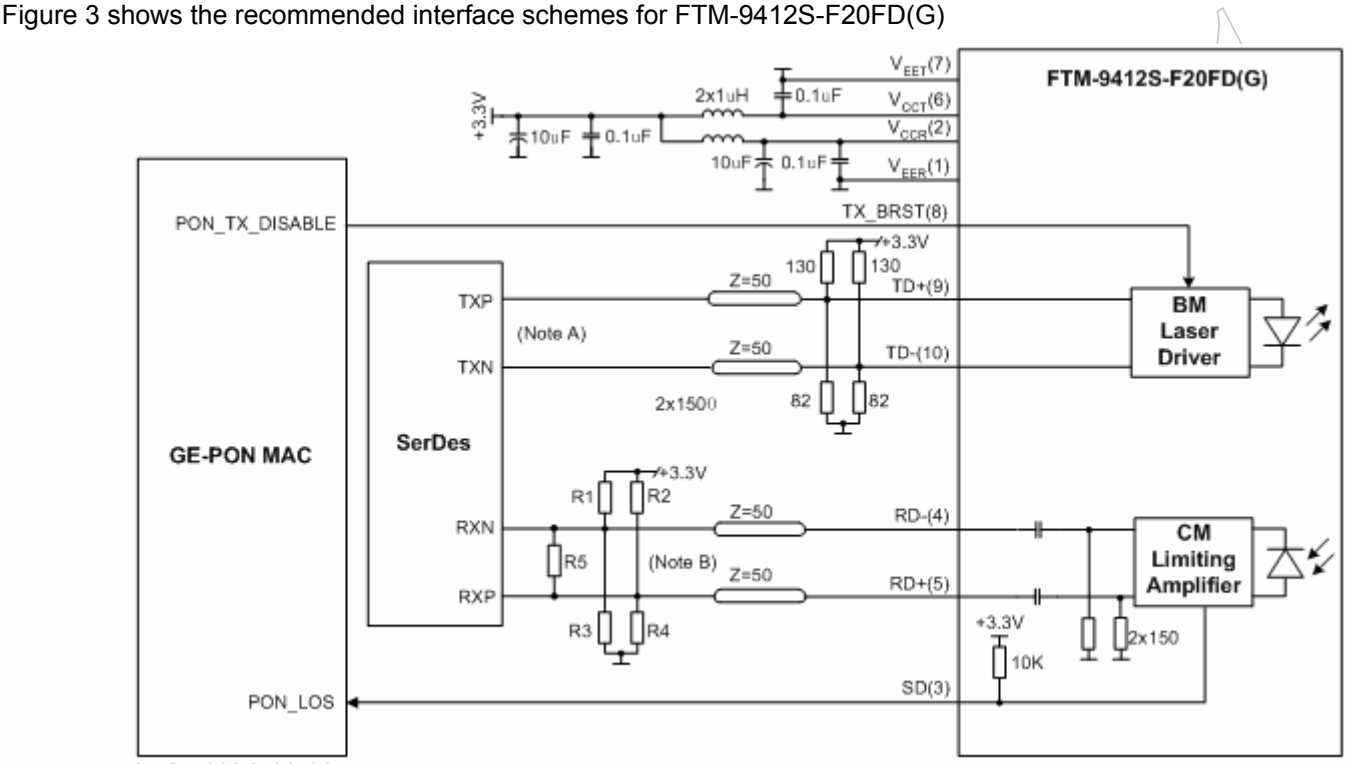

Figure 3 Recommended Interface Circuit (FTM-9412S-F20FD(G))

Note A: Open emitter output internally.

Note B: LVPECL output, AC coupled internally.

Input stage in SerDes IC is assumed with high impedance and internal bias to Vcc-1.3V

R1=R2=R3=R4=N.C, R5=100Ω

Input stage in SerDes IC is assumed without internal bias to Vcc-1.3V

R1=R2=82Ω,R3=R4=130Ω,R5=N.C

Pin Definitions

2×5 SFF planform in Figure 4 below shows the pin information of electrical interface and mounting studs. Functions are described in Table 7 with some accompanying notes.

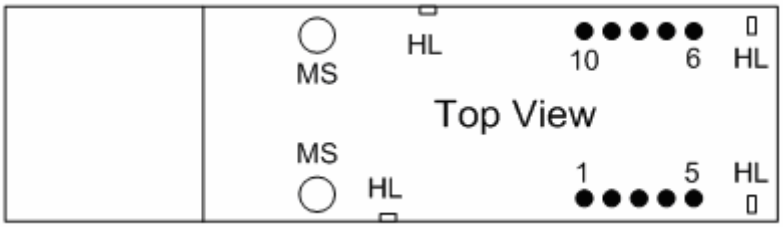

Figure 4 2×5 SFF Planform

Table 7 - Pin Function Definitions

Pin No.	Name	Description	Notes
1	V_{EER}	Receiver Signal Ground	
2	V_{CCR}	Receiver Power Supply	
3	SD	Receiver Signal-Detected Indication	1
4	RD-	Inverted Receiver Data Output	2
5	RD+	Non-inverted Receiver Data Output	
6	V_{CCT}	Transmitter Power Supply	
7	V_{EET}	Transmitter Signal Ground	
8	TX_BRST	Transmitter Burst Control	3
9	TD+	Transmitter Non-inverted Data Input	4
10	TD-	Transmitter Inverted Data Input	
MS	MS	Mounting Studs	5
HL	HL	Housing Leads	6

Note 1: TTL logic output, with internal 10KΩ pull-up resistor.
Optical Signal-Detected: High; Optical Signal Loss: Low

Note 2: LVPECL logic output, AC coupled internally. (See Recommended Interface Circuit)

Note 3: A positive level enable optical signal output under burst mode.
(See Timing Parameter Definition in Burst Mode Sequence)

Note 4: Note 4: Compatible with LVPEC input
(See Recommended Interface Circuit and Table 6 - Electrical Input/Output Coupling Mode)

Note 5: The mounting studs are provided for transceiver mechanical attachment to circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground. The holes in the circuit board must be tied to chassis ground.

Note 6: The housing leads may be provided for additional signal grounding. These additional grounds may improve signal integrity, EMC, or ESD performance. The holes in the circuit board must be included and be tied to signal ground.

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Mechanical Design Diagram

The form factor is 2×5 SFF.

The mechanical design diagram is shown in Figure 5. (Dimension in mm)

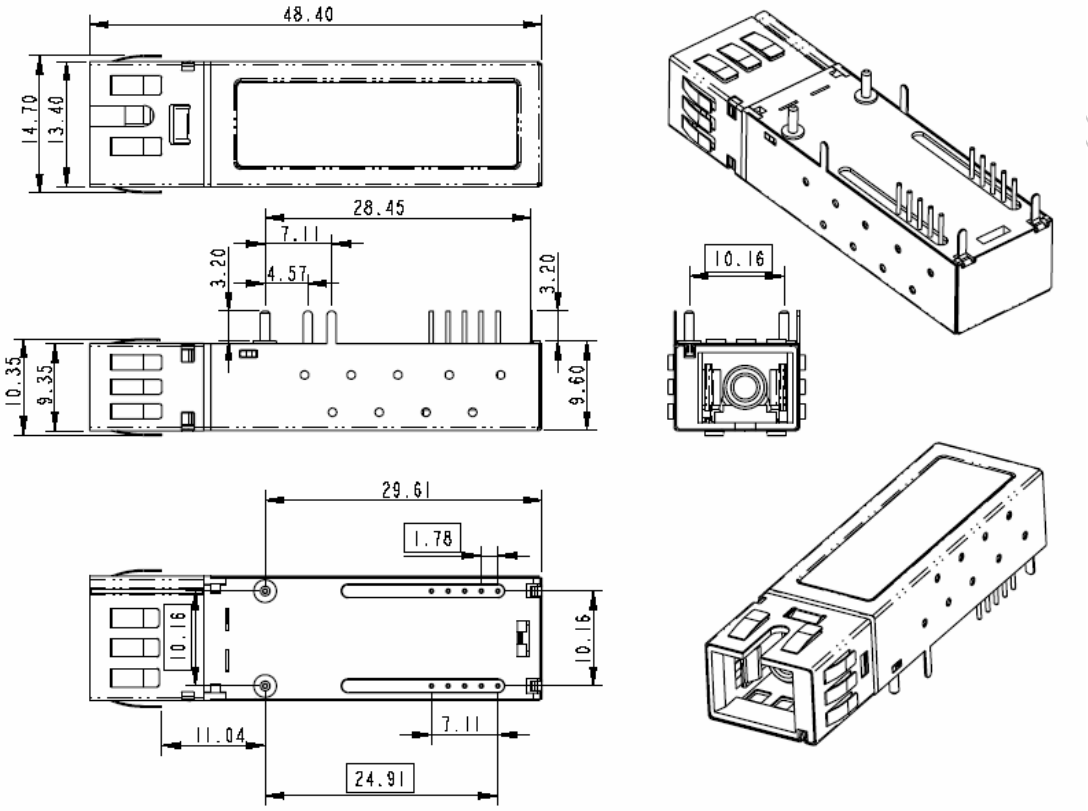

Figure 5 Mechanical Design Diagram

Ordering Information

Part No.	Product Description
FTM-9412S-F20F	1310nm(TX)/1490nm(RX), SC/UPC receptacle 2×5 SFF for GEPON ONU 20km (PX20) application, 0°C ~ 70°C(case temperature), Tx AC Coupling, Rx AC Coupling
FTM-9412S-F20FD	1310nm(TX)/1490nm(RX), SC/UPC receptacle 2×5 SFF for GEPON ONU 20km (PX20) application, 0°C ~ 70°C(case temperature), Tx DC Coupling, Rx AC Coupling
FTM-9412S-F20FG	1310nm(TX)/1490nm(RX), SC/UPC receptacle 2×5 SFF for GEPON ONU 20km (PX20) application, 0°C~70°C(case temperature), Tx AC Coupling, Rx AC Coupling, RoHS compliance
FTM-9412S-F20FDG	1310nm(TX)/1490nm(RX), SC/UPC receptacle 2×5 SFF for GEPON ONU 20km (PX20) application, 0°C~70°C(case temperature), Tx DC Coupling, Rx AC Coupling, RoHS compliance

Related Documents

For further information, please refer to the following documents:

- IEEE Std 802.3ah™-2004

Obtaining Document

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Revision History

Reversion	Initiate	Review	Approve	Subject	Release Date
Pre 1a	Johnny Yang	Peter Tang	Peter Tang	Initial datasheet (Doc No. DS3493013-1a)	2006-04-06
Pre 1b	Jacob Cai	Johnny Yang	Peter Tang	Revised datasheet Change the product picture (Doc No. DS3493013-1b)	2006-06-30
Pre 1c	Jacob Cai	Johnny Yang	Peter Tang	Revised datasheet Change the Mechanical Design Diagram in Figure 5 (Doc No. DS3493013-1c)	2006-08-09
Pre 1d	Jacob Cai	Johnny Yang	Peter Tang	Revised datasheet 1. Change Mechanical Design Diagram in Figure 5; (Doc No. DS3493013-1d)	2006-11-10
Pre 1e	Jacob Cai	Johnny Yang	Peter Tang	Revised datasheet 1. Change the photo in cover page; 2. Change Figure 4; 3. Update Table 7 and its notes. (Doc No. DS3493013-1e)	2007-1-19
Pre 1f	Jacob Cai	Johnny Yang	Peter Tang	Revised datasheet 1. Update “Product Description” in “Ordering Information” section. 2. Update Figure 5; 3. Update “Average Launch Power” item in Table 4; (Doc No. DS3493013-1f)	2007-3-16

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