CSD23202W10 12V P 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 超低 Q_g 和 Q_{gd}
- 小尺寸封装 1mm x 1mm
- 薄型，0.62mm 高度
- 无铅
- 栅极静电放电 (ESD) 保护 - 3kV
- 符合 RoHS 环保标准
- 无卤素

2 应用范围

- 电池管理
- 负载开关
- 电池保护

3 说明

这款 12V，44mΩ 器件设计用于在超薄且具有出色散热特性的 1mm × 1mm 小外形
封装内提供最低的导通电阻和栅极电荷。

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	-12		V
Q_g	栅极电荷总量 (-4.5V)	2.9		nC
Q_{gd}	栅漏栅极电荷	0.28		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = –1.5V	82	mΩ
		V_{GS} = –1.8V	67	mΩ
		V_{GS} = -2.5V	54	mΩ
		V_{GS} = -4.5V	44	mΩ
$V_{GS(th)}$	阈值电压	–0.60		V

订购信息(1)

器件	数量	介质	封装	出货
CSD23202W10	3000	7 英寸卷带	1 x 1mm 晶圆级封装	卷带封装
CSD23202W10T	250	7 英寸卷带		

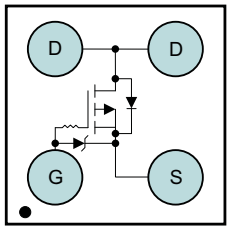
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-12	V
V_{GS}	栅源电压	-6	V
I_D	持续漏极电流(1)	–2.2	A
I_{DM}	脉冲漏极电流(2)	–25	A
I_G	持续栅极钳位电流	-0.5	A
	脉冲栅极钳位电流	-7	A
P_D	功率耗散(1)	1	W
T_J, T_{stg}	运行结温和储存温度范围	-55 至 150	°C

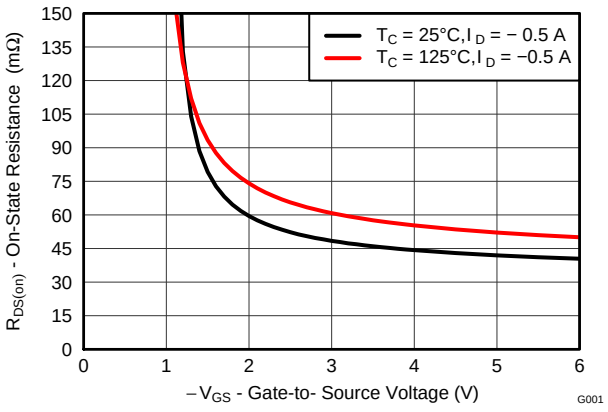
(1) 器件在 105ºC 温度下运行
(2) $R_{\theta JA}$ 典型值 = 195°C/W，脉宽 ≤ 100µs，占空比 ≤ 1%

顶视图



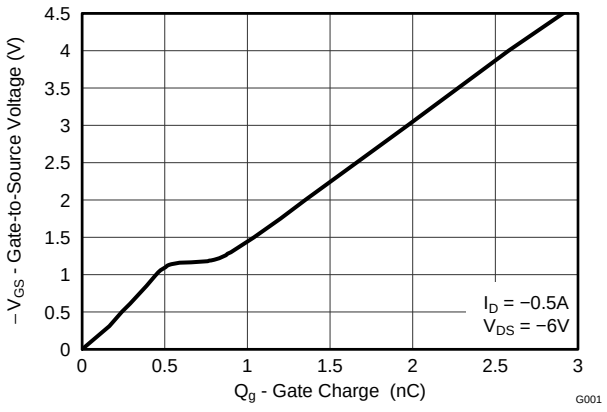
P0097-01

$R_{DS(on)}$ 与 V_{GS} 间的关系



G001

栅极电荷



G001

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

目录

1 特性 1
2 应用范围 1
3 说明 1
4 修订历史记录 2
5 **Specifications** 3
5.1 Electrical Characteristics 3
5.2 Thermal Information 3
5.3 Typical MOSFET Characteristics 4
6 器件和文档支持 7
6.1 商标 7
6.2 静电放电警告 7
6.3 术语表 7
7 机械封装和可订购信息 8
7.1 CSD23202W10 封装尺寸 8
7.2 焊盘布局建议 9
7.3 卷带封装信息 9

4 修订历史记录

日期	修订版本	注释
2014 年 8 月	*	最初发布。

版权 © 2014, Texas Instruments Incorporated

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 µA	–12			V
BV_{GSS}	Gate-to-Source Voltage;	V_{DS} = 0 V, I_G = –250 µA	–6		–7.2	V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –9.6 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 µA	–0.4	–0.6	–0.9	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = –1.5 V, I_D = –0.5 A		82	123	mΩ
		V_{GS} = –1.8 V, I_D = –0.5 A		67	92	mΩ
		V_{GS} = –2.5 V, I_D = –0.5 A		54	66	mΩ
		V_{GS} = –4.5 V, I_D = –0.5 A		44	53	mΩ
g_{fs}	Transconductance	V_{DS} = –1.2 V, I_D = –0.5 A		5.6		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –6.0 V, f = 1 MHz		394	512	pF
C_{OSS}	Output Capacitance			238	310	pF
C_{RSS}	Reverse Transfer Capacitance			29	37	pF
Q_g	Gate Charge Total (–4.5 V)	V_{DS} = –6 V, I_D = –0.5 A		2.9	3.8	nC
Q_{gd}	Gate Charge Gate-to-Drain			0.28		nC
Q_{gs}	Gate Charge Gate-to-Source			0.55		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.29		nC
Q_{OSS}	Output Charge	V_{DS} = –6 V, V_{GS} = 0 V		2.0		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –0.5 A R_G = 0 Ω		9		ns
t_r	Rise Time			4		ns
$t_{d(off)}$	Turn Off Delay Time			58		ns
t_f	Fall Time			21		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_S = –0.5 A, V_{GS} = 0 V		–0.66	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= –6 V, I_F = –0.5 A, di/dt = 100 A/µs		3.7		nC
t_{rr}	Reverse Recovery Time			12		ns

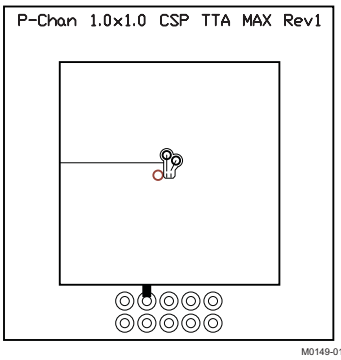
5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

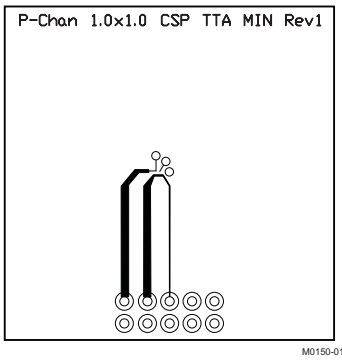
THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1)		195		°C/W
	Junction-to-Ambient Thermal Resistance(2)		65		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

Copyright © 2014, Texas Instruments Incorporated



Typical $R_{\theta JA}$ = 65°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Typical $R_{\theta JA}$ = 195°C/W when mounted on minimum pad area of 2 oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

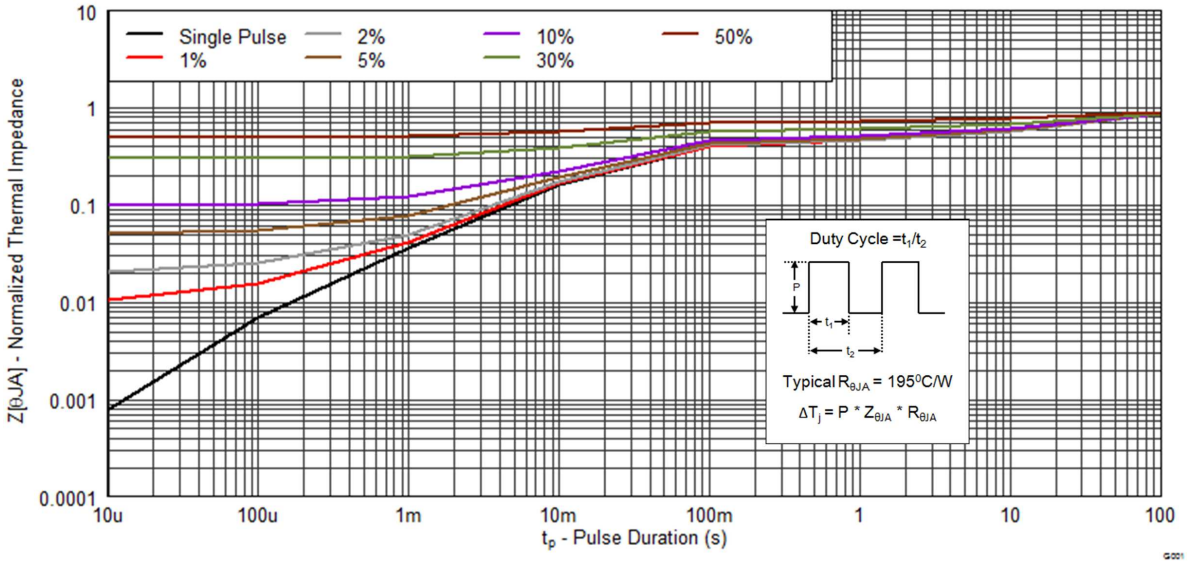


Figure 1. Transient Thermal Impedance

Copyright © 2014, Texas Instruments Incorporated

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

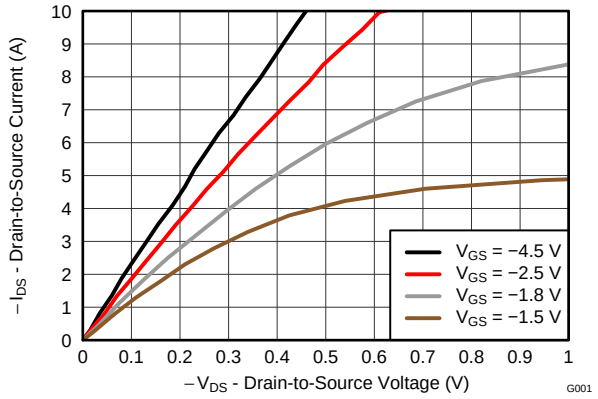


Figure 2. Saturation Characteristics

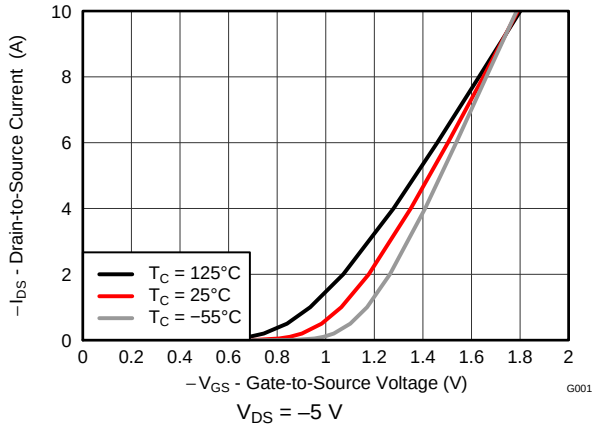


Figure 3. Transfer Characteristics

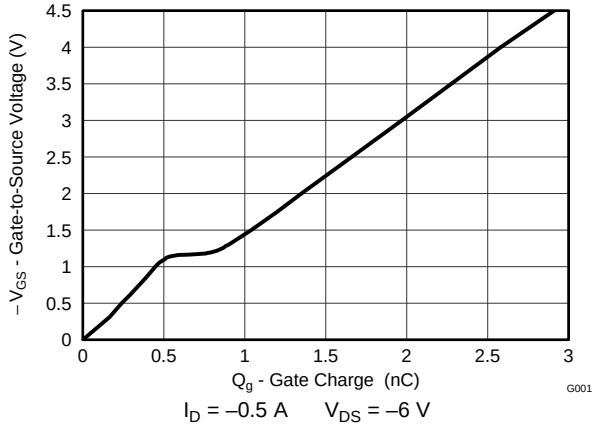


Figure 4. Gate Charge

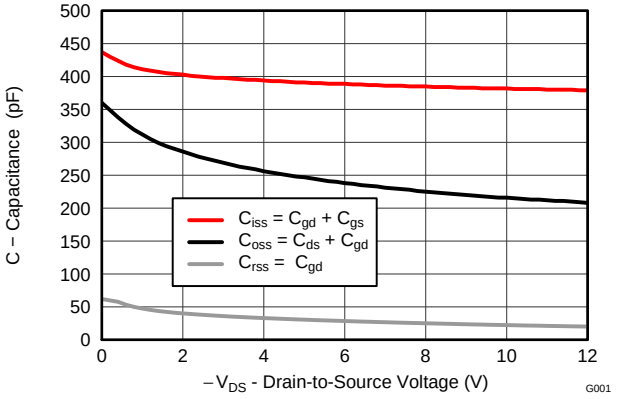


Figure 5. Capacitance

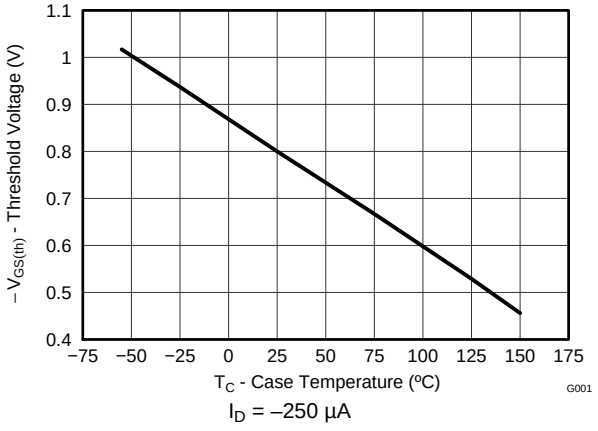


Figure 6. Threshold Voltage vs Temperature

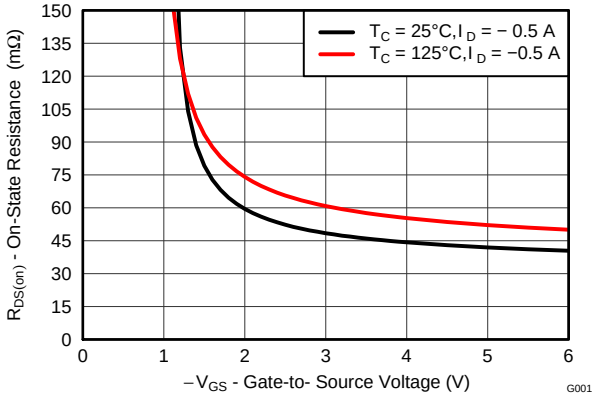


Figure 7. On-State Drain-to-Source Resistance vs Gate-to-Source Voltage

Copyright © 2014, Texas Instruments Incorporated

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

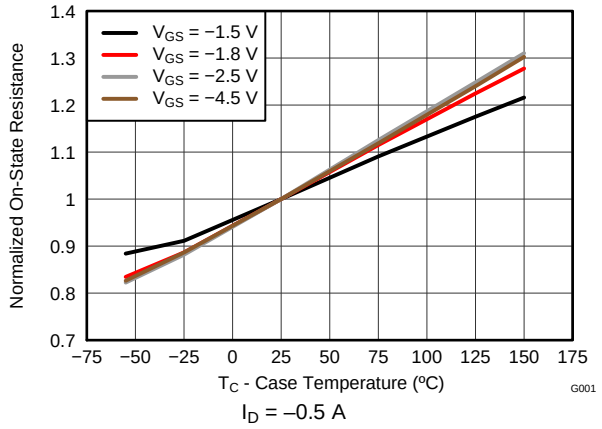


Figure 8. Normalized On-State Resistance vs Temperature

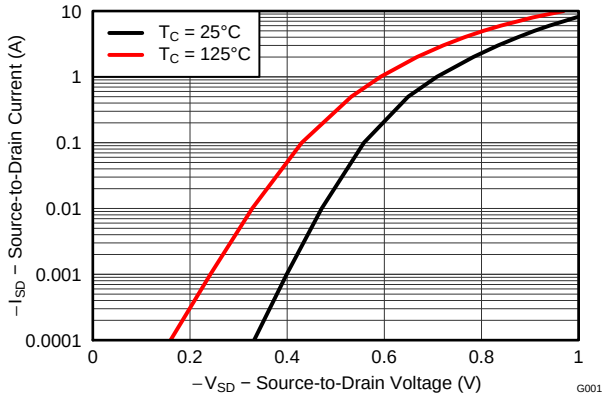


Figure 9. Typical Diode Forward Voltage

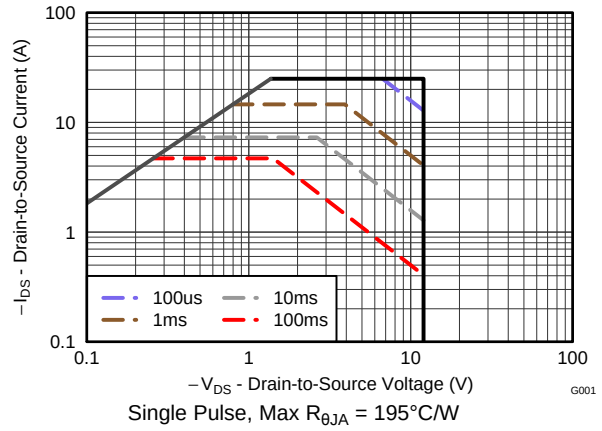


Figure 10. Maximum Safe Operating Area

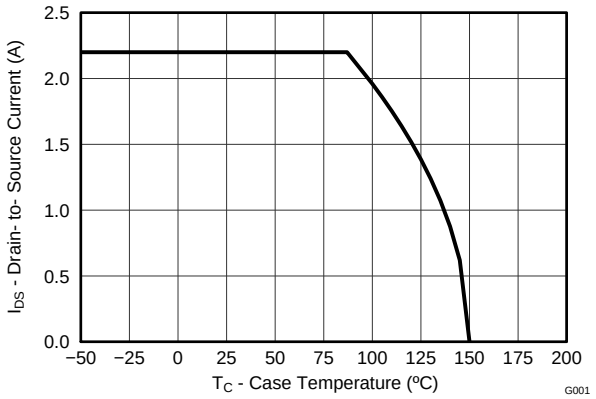


Figure 11. Maximum Drain Current vs Temperature

版权 © 2014, Texas Instruments Incorporated

6 器件和文档支持

6.1 商标

NexFET is a trademark of Texas Instruments.

6.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.3 术语表

SLYZ022 — *TI 术语表*。

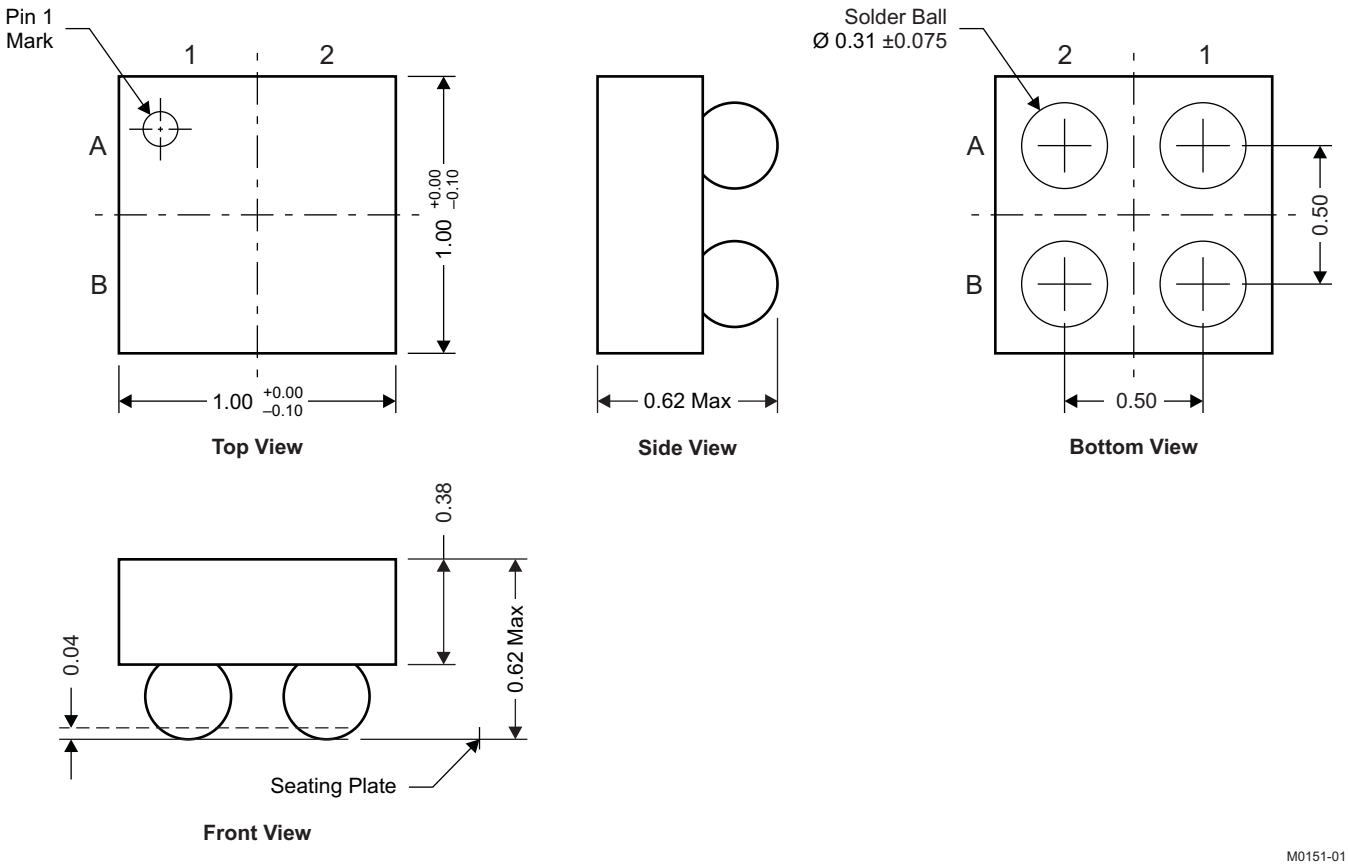
这份术语表列出并解释术语、首字母缩略词和定义。

版权 © 2014, Texas Instruments Incorporated

7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 CSD23202W10 封装尺寸



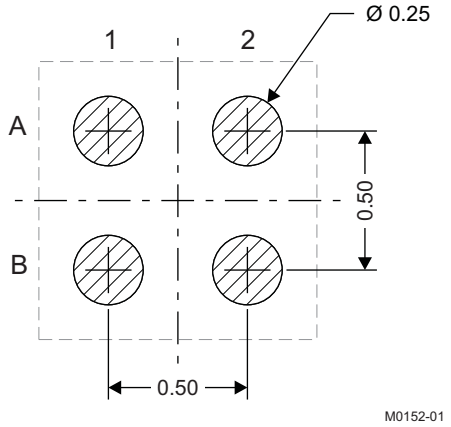
NOTE: 全部尺寸单位为 mm（除非另外注明）。

引脚配置表

位置	名称
B1	源极
A1	栅极
A2，B2	漏极

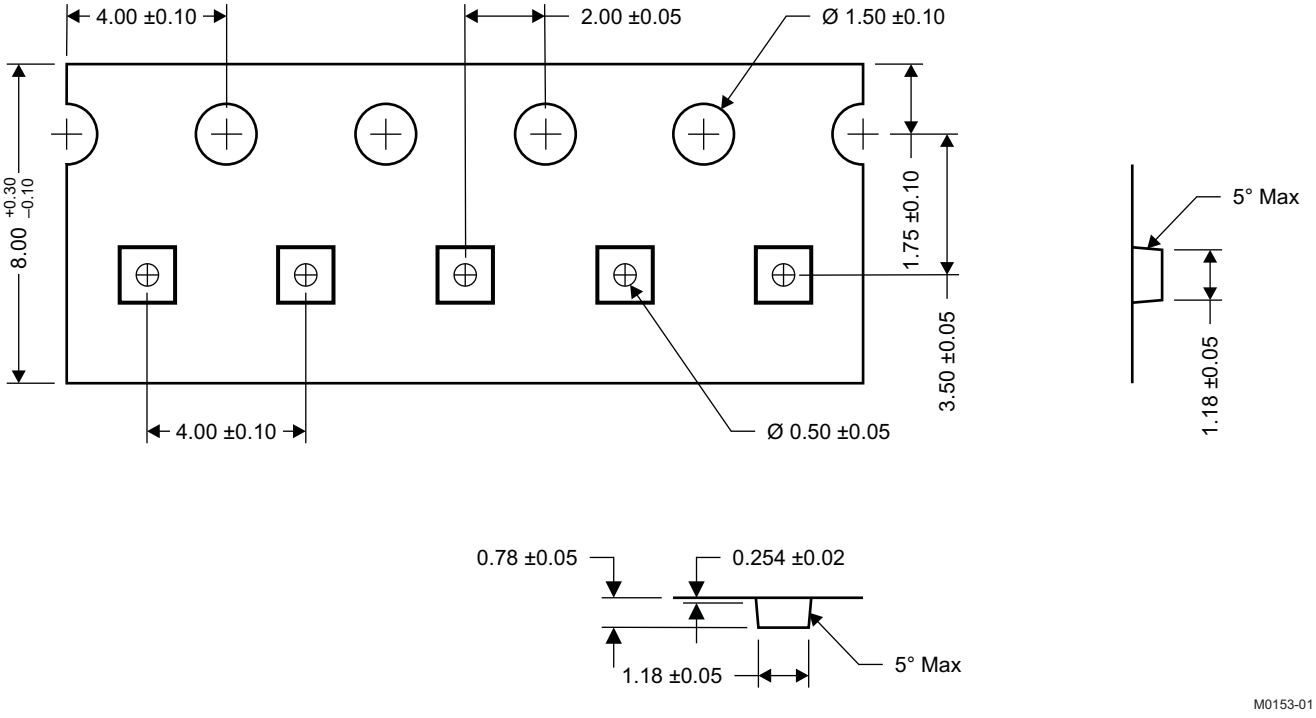
版权 © 2014, Texas Instruments Incorporated

7.2 焊盘布局建议



NOTE: 全部尺寸单位为 mm（除非另外注明）。

7.3 卷带封装信息



NOTE: 全部尺寸单位为 mm（除非另外注明）。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23202W10	ACTIVE	DSBGA	YZB	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		202	Samples
CSD23202W10T	ACTIVE	DSBGA	YZB	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

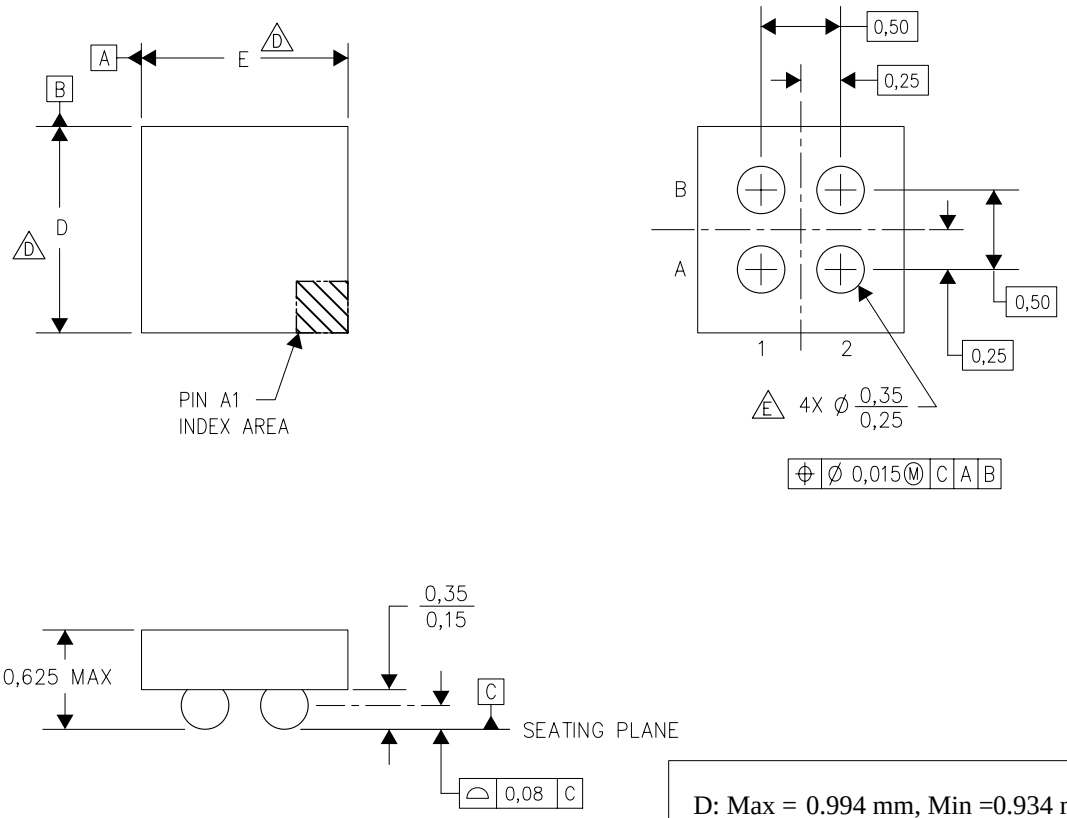
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

YZB (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



D: Max = 0.994 mm, Min =0.934 mm

E: Max = 0.99 mm, Min = 0.93 mm

4205055/D 07/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZB package can have dimension D ranging from 0.94 to 1.65 mm and dimension E ranging from 0.94 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEB (Drawing #4204178) for tin–lead (SnPb) balls.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司