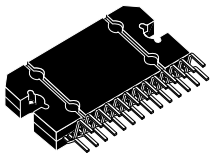
STA5100

140W MONO BASH® DIGITAL FIDELITY POWER AMPLIFIER

- MONOCHIP BRIDGE MONO AMPLIFIER FOR BASH® ARCHITECTURE
- 110W OUTPUT POWER @ R_L = 4 Ω, THD = 0.5%
- 140W OUTPUT POWER @ R_L = 4 Ω, THD = 10%
- HIGH DYNAMIC PREAMPLIFIER INPUT STAGES
- EXTERNAL PROGRAMMABLE FEEDBACK TYPE COMPRESSORS
- AC COUPLED INPUT TO CLASS AB BRIDGE OUTPUT AMPLIFIER
- PRECISION RECTIFIERS TO DRIVE THE DIGITAL CONVERTER
- ON-OFF SEQUENCE/ TIMER WITH MUTE AND STANDBY
- PROPORTIONAL OVER POWER OUTPUT CURRENT TO LIMIT THE DIGITAL CONVERTER
- ABSOLUTE POWER BRIDGE OUTPUT TRANSISTOR POWER PROTECTION
- ABSOLUTE OUTPUT CURRENT LIMIT
- INTEGRATED THERMAL PROTECTION
- POWER SUPPLY OVER VOLTAGE PROTECTION
- FLEXIWATT POWER PACKAGE WITH 27 PIN
- **BASH® licence required**

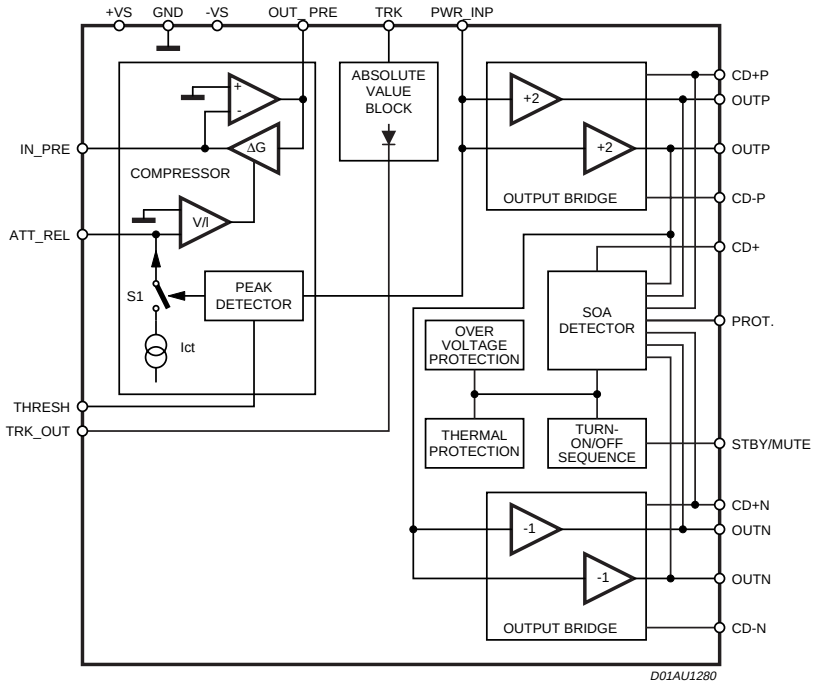


FLEXIWATT27

DESCRIPTION

The STA5100 is a fully integrated power module designed to implement a BASH® amplifier when used in conjunction with STABP01 digital processor.

BLOCK DIAGRAM



DESCRIPTION (continued)

Notice that normally only one Digital Converter is needed to supply a stereo or multi-channel amplifier system, therefore most of the functions implemented in the circuit have summing outputs

The signal circuits are biased by fixed negative and positive voltages referred to Ground. Instead the final stages of the output amplifiers are supplied by two external voltages that are following the audio signal . In this way the headroom for the output transistors is kept at minimum level to obtain a high efficiency power amplifier.

The Compressor circuits, one for each channel, performs a particular transfer behavior to avoid the dynamic restriction that an adaptive system like this requires. To have a high flexibility the attack / release time and the threshold levels are externally programmable. The tracking signal for the external digital converter is generated from the Absolute Value block that rectifies the audio signal present at the compressor output. The outputs of these blocks are decoupled by a diode to permit an easy sum of this signal for the multichannel application. The output power bridges have a dedicated input pin to perform an AC decoupling to cancel the compressor output DC offset. The gain of the stage is equal to 4 (+12dB). A sophisticated circuit performs the output transistor power detector that , with the digital converter, reduces the power supply voltage . Moreover, a maximum current output limiting and the over temperature sensor have been added to protect the circuit itself. The external voltage applied to the STBY/MUTE pin forces the two amplifiers in the proper condition to guarantee a silent turn-on and turn-off.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$+V_S$	Positive supply voltage referred to pin 13 (GND)	30	V
$-V_S$	Negative supply voltage referred to pin 13 (GND)	-24	V
V_{CD+}	Positive supply voltage tracking rail referred to pin 13 (GND)	22	V
V_{CD+}	Positive supply voltage operated to Vs+(1)	0.3	V
V_{CD-}	Negative supply voltage referred to -Vs (1)	-0.3	V
V_{CD-}	Negative supply voltage tracking rail referred to pin 13 (GND)	-22	V
V_{Att_Rel}	Pin 3 Negative & Positive maximum voltage reffered to GND (pin 13)	-0.5 to +20	V
V_{Pwr_Imp}	VTrk Pin 7, 10 Negative & Positive maximum voltage referred to GNC (pin 13)	-20 to +20	V
V_{In_pre}	Pin 8 Negative & Positive maximum voltage referred to GND (pin 13)	-0.5 to +0.5	V
$V_{threshold}$	Pin 17 Negative & Positive maximum voltage referred to GND (pin 13)	-7 to +0.5	V
$I_{stb-max}$	Pin 11 maximum input current (Internal voltage clamp at 5V)	500	µA
$V_{stbymute}$	Pin 11 negative maximum voltage referred to GND (pin 13)	-0.5	V

Notes: 1. V_{CD-} must not be more negative than -Vs and V_{CD+} must not be more positive than $+V_S$

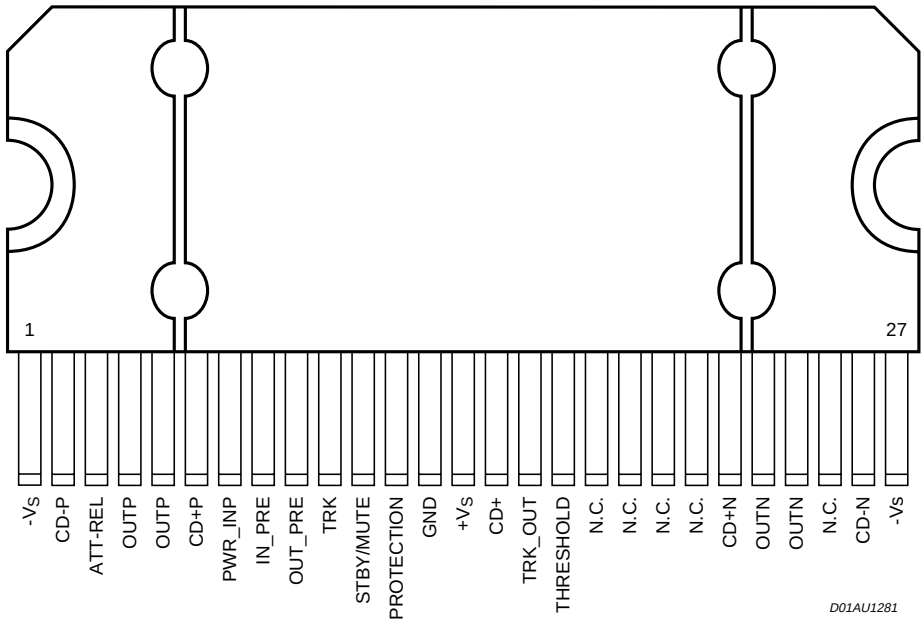
THERMAL DATA

Symbol	Parameter		Value	Unit
T_j	Max Junction temperature		150	°C
$R_{th\ j_case}$	Thermal Resistance Junction to case	max	1	°C/W

OPERATING RANGE

Symbol	Parameter	Value	Unit
$+V_S$	Positive supply voltage	+20 to +30	V
$-V_S$	Negative supply voltage	-10 to -22	V
ΔV_{S+}	Delta positive supply voltage	5V ≤ (Vs+ - VCD+) ≤ 10V	V
V_{CD+}	Positive supply voltage tracking rail	+3 to +17	V
V_{CD-}	Negative supply voltage tracking rail	-3 to -17	V
I_{in_Max}	Current at pin In_Pre related to compressor behaviour	-1 to +1	mA peak
$V_{trheshold}$	Voltage at pin Threshold	-5 to 0	V
T_{amb}	Ambient Temperature Range	0 to 70	°C
I_{sb_max}	Pin 11 maximum input current (Internal voltage clmp at 5V)	200	µA

PIN CONNECTION



PIN FUNCTION

N°	Name	Description
1	-Vs	Negative Bias Supply
2	CD-P	Channel P Time varying tracking rail negative power supply
3	Att_Rel	Attack release rate
4	OutP	Channel P
5	OutP	Channel P
6	CD+P	Channel P positive power supply
7	Pwr_Inp	Input to power stage
8	In_pre	Pre-amp input (virtual ground)
9	Out_pre	Output channel
10	Trk	Absolute value block input
11	Stby/mute	Standby/mute input voltage control
12	Protection	Protection signal for STABP01 digital processor
13	Gnd	Analog Ground
14	+Vs	Positive Bias Supply
15	CD+	Time varying tracking rail positive power supply
16	Trk_out	Reference output for STABP01 digital processor
17	Threshold	Compressor threshold input
18	N.C.	
19	N.C.	
20	N.C.	
21	N.C.	
22	CD+N	Channel N positive power supply
23	OutN	Channel N
24	OutN	Channel N
25	N.C.	
26	CD-N	Channel N Time varying tracking rail negative power supply
27	-Vs	Negative Bias Supply

ELECTRICAL CHARACTERISTCS (Test Condition: Vs+ = 26V, Vs- = -22V, V_{CD+} = 17V, V_{CD-} = -17V, R_L = 4Ω, external components at the nominal value f = 1KHz, Tamb = 25°C unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PREAMPLIFIER AND COMPRESSOR						
$V_{out\ clamp}$	Maximum Voltage at Out_pre pin		10	11	12	Vpeak
I_{in}	Audio input current				0.8	mA
$V_{control}$	Voltage at Attack_Release pin	Attenuation = 0dB Attenuation = 6dB Attenuation = 26dB	 0.35 6	0 0.5 9	 0.65 12	V V V
VC_{omp_Th}	Input voltage range for the compression		-5		-1	V
Z_{th}	Input impedance of Threshold pin		100			KΩ
Voffset	Output Offset at Out_pre pin with:	V_{CRT}= 0V; Attenuation = 0dB V_{CRT}= 0.5V; Attenuation = 6dB V_{CRT}= 9V; Attenuation = 26dB	-10 -250 -450		10 250 450	mV mV mV
THD	Distortion at Out_pre:	V_{CRT}= 0V; Attenuation = 0dB V_{CRT}= 0.5V; Attenuation = 6dB V_{CRT}= 9V; Attenuation = 26dB		0.01	 5 5	% % %
EN	Noise at Out_pre pin :	V_{CRT}= 0V; Attenuation = 0dB V_{CRT}= 0.5V; Attenuation = 6dB V_{CRT}= 9V; Attenuation = 26dB		10(2) 50 60		µV µV µV
I_{ct}	Attack time current at pin Attack_release			1.5		mA

2. This value is due to the thermal noise of the external resistors R_r and R_i.

TRACKING PARAMETERS						
G_{trk}	Tracking reference voltage gain		13	14	15	V
V_{trk_out}	Tracking ref. output voltage		0	20		V
I_{trk_out}	Current capability		5	6	7	mA
Z_{trk_in}	Input impedance (T_{rk})			1		MΩ
OUTPUT BRIDGE						
G_{out}	Half Output bridge gain		5.5	6	6.5	dB
G_{ch}	Output bridge differential gain		11	12	13	dB
ΔG_{ch}	Output bridges gain mismatch		-1		1	dB
P_{out}	Continuous Output Power	THD = 0.5% THD = 10%	100 125	110 140		W W
THD	Total harmonic distortion of the output bridge	Po = 5W		0.01		%
		f = 20Hz to 20KHz; Po = 50W			0.1	%
V_{Off}	Output bridge D.C. offset				50	mV
EN	Noise at Output bridge pins	f = 20Hz to 20KHz; Rg = 50Ω		12		µV
Z_{br_in}	Input impedance		100	140	180	KΩ

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{dson}	Output power Rdson	I_O = 1A		100	200	mΩ
OLG	Open Loop Voltage Gain			100		dB
GB	Unity Gain Bandwidth			1.4		MHz
SR	Slew Rate			7		V/µs
PROTECTION						
V_{stby}	Stby voltage range		0		0.8	V
V_{mute}	Mute voltage range		1.6		3	V
V_{play}	Play voltage range		4		5	V
T_{h1}	First Over temperature threshold			130		°C
T_{h2}	Second Over temperature threshold			150		°C
Unbal. Ground	Upper Unbalancing ground threshold	Referred to $(CD^+ - CD^-)/2$		5		V
Unbal. Ground	Lower Unbalancing ground threshold	Referred to $(CD^+ - CD^-)/2$		-5		V
UV_{th}	Under voltage threshold	|Vs+| + |Vs-|		20		V
$P_{d_reg.}$	Power dissipation threshold for system regulation	I_{prot} = 50µA; @ Vds = 10V	50		62	W
P_{d_max}	Switch off power dissipation threshold	@ Vds = 10V		96		W
I_{prot}	Protection current slope	for Pd > Pd_{reg}		400		µA/W
I_{lct}	Limiting Current threshold		11	12	13	A
I+Vs	Positive supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		4 30 30		mA mA mA
I-Vs	Negative supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		4 30 30		mA mA mA
ICD+	Positive traking rail supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		100 110 110		µA mA mA
ICD-	Negative traking rail supply current	Stby (Vstby/mute pin = 0V) Mute (Vstby/mute pin = 2.5V) Play (Vstby/mute pin = 5V no signal)		100 110 110		µA mA mA

FUNCTIONAL DESCRIPTION

The circuit contains all the blocks to build a mono amplifier. It is based on the Output Bridge Power Amplifier, and its protection circuit. Moreover, the compression function and a signal rectifier are added to complete the circuit.

The operation modes are driven by The Turn-on/off sequence block. In fact the IC can be set in three states by the Stby/mute pin:

Standby ($V_{pin} < 0.8V$), Mute ($1.6V < V_{pin} < 3V$), and Play ($V_{pin} > 4V$).

In the Standby mode all the circuits involved in the signal path are in off condition, instead

in Mute mode the circuits are biased but the Speakers Outputs are forced to ground potential.

These voltages can be get by the external RC network connected to Stby/Mute pin.

The same block is used to force quickly the I.C. In standby mode or in mute mode when the I.C. dangerous condition has been detected. The RC network in these cases is used to delay the Normal operation restore.

The protection of the I.C. are implemented by the Over Temperature, Unbalance Ground, Output Short circuit, Under voltage, and output transistor Power sensing as shown in the following table:

Table 1. Protection Implementation

Fault Type	Condition	Protection strategy	Action time	Release time
Chip Over temperature	Tj > 130 °C	Mute	Fast	Slow Related to Turn_on sequence
Chip Over temperature	Tj > 150 °C	Standby	Fast	Slow, Related to Turn_on sequence
Unbalancing Ground	|Vgnd| > ((CD+) - (CD-))/2 + 5V	Standby	Fast	Slow, Related to Turn_on sequence
Short circuit	Iout > 12A	Standby	Fast	Slow, related to Turn_on sequence
Under Voltage	|Vs+| + |Vs-|< 20V	Standby	Fast	Slow, related to Turn_on sequence
Extra power dissipation at output transistor	Pd tr. > 50W	Reducing DIGITAL CONVERTER output voltage.	Related to the DIGITAL CONVERTER	Related to the DIGITAL CONVERTER
Maximum power dissipation at output transistor	Pd tr. > 96W	Standby	Fast	Slow, related to Turn_on sequence

See the POWER PROTECTION paragraph for the details

Compression

An other important function implemented, to avoid high power dissipation and clipping distortion, is the Compression of the signal input. In fact the preamplifier stage performs a voltage gain equal to 5, fixed by Ri and Rr external resistor, but in case of high input signal or low power supply voltage, its gain could be reduced of 26dB. This function is obtained with a feedback type compressor that , in practice, reduces the impedance of the external feedback network. The behavior of compression it's internally fixed but depends from the Audio input voltage signal level, and from the Threshold voltage applied to the Threshold pin. The attack and release time are programmable by the external RC network connected to the Att_Rel pins.

The constraints of the circuit in the typical application are the following:

Vthreshold range = -5 to 0

Vin peak max = 8V

Vout peak max = 10V

Gain without compression (G) = 5

Max Attenuation ratio = 26 dB

The following graph gives the representation of the Compressor activation status related to the Vthreshold and the input voltage. The delimitation line between the two fields, compression or not, is expressed by the formula :

$$V_{in} = \frac{2 \cdot |Vthreshold|}{G}$$

Where G is the preamplifier gain without compression.

In the compression region the gain of the preamplifier will be reduced

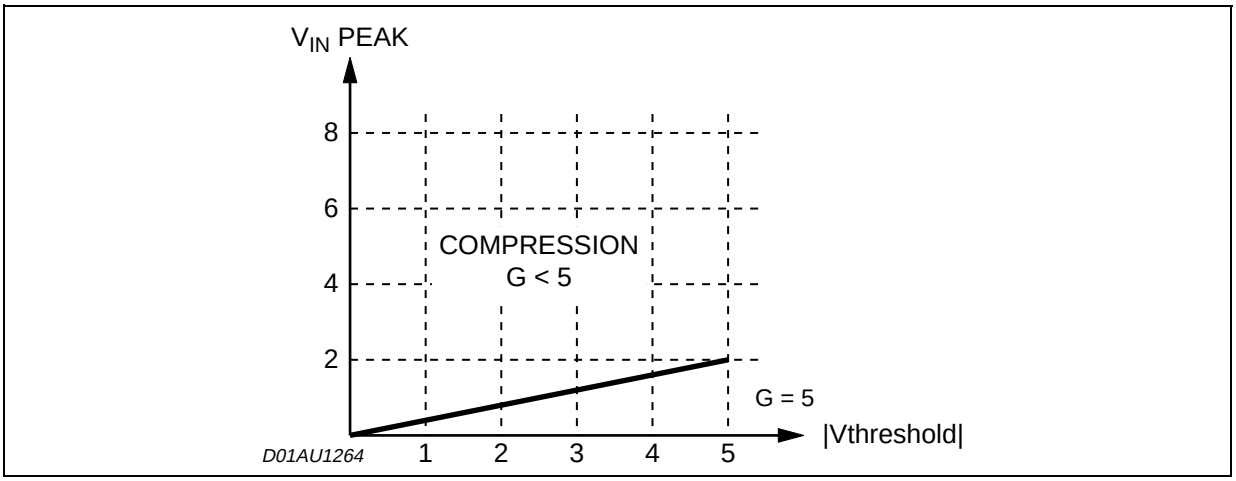
(G = 2·Vthreshold/Vin) to maintain at steady state the output voltage equal 2*|Vthreshold| .

Instead in the other region the compressor will be off (G = 5).

The delimitation line between the two fields can be related to the output voltage of the preamplifier: in this case the formula is :

$$V_{out} = 2 \cdot |Vthreshold|$$

Figure 1. Compressor activation field



The relative attenuation introduced by the variable gain cell is the following :

$$Attenuation = 20\log\frac{2}{5} \cdot \frac{|V_{th}|}{V_{in_peak}}$$

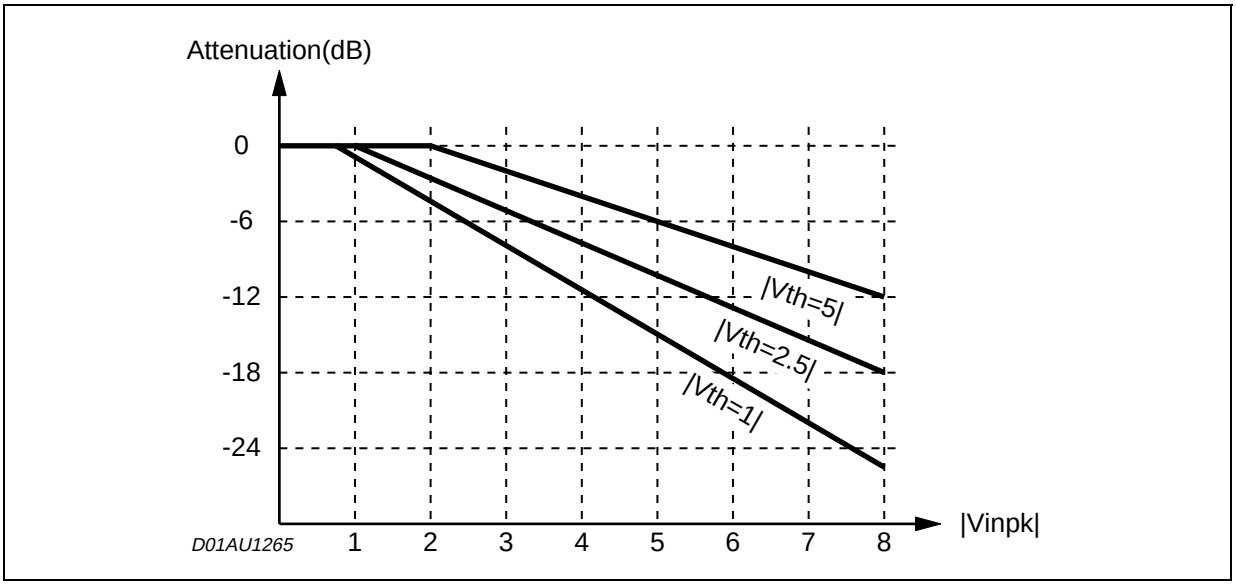
The total gain of the stage will be:

$$Gdb = 20\log5 + Attenuation$$

The maximum input swing is related to the value of input resistor, to guarantee that the input current remain under Iin_Max value (1 mA).

$$R_i > \frac{V_{in_peak}}{I_{in_max}}$$

Figure 2. Compressor attenuation vs. input amplitude



ABSOLUTE VALUE BLOCK

The absolute value block rectifies the signal after the compression to extract the control voltage for the external digital converter. The output voltage swing is internally limited, the gain is internally fixed to 14.

The input impedance of the rectifier is very high , to allow the appropriate filtering of the audio signal before the rectification (between Out_pre and Trk pins).

OUTPUT BRIDGE

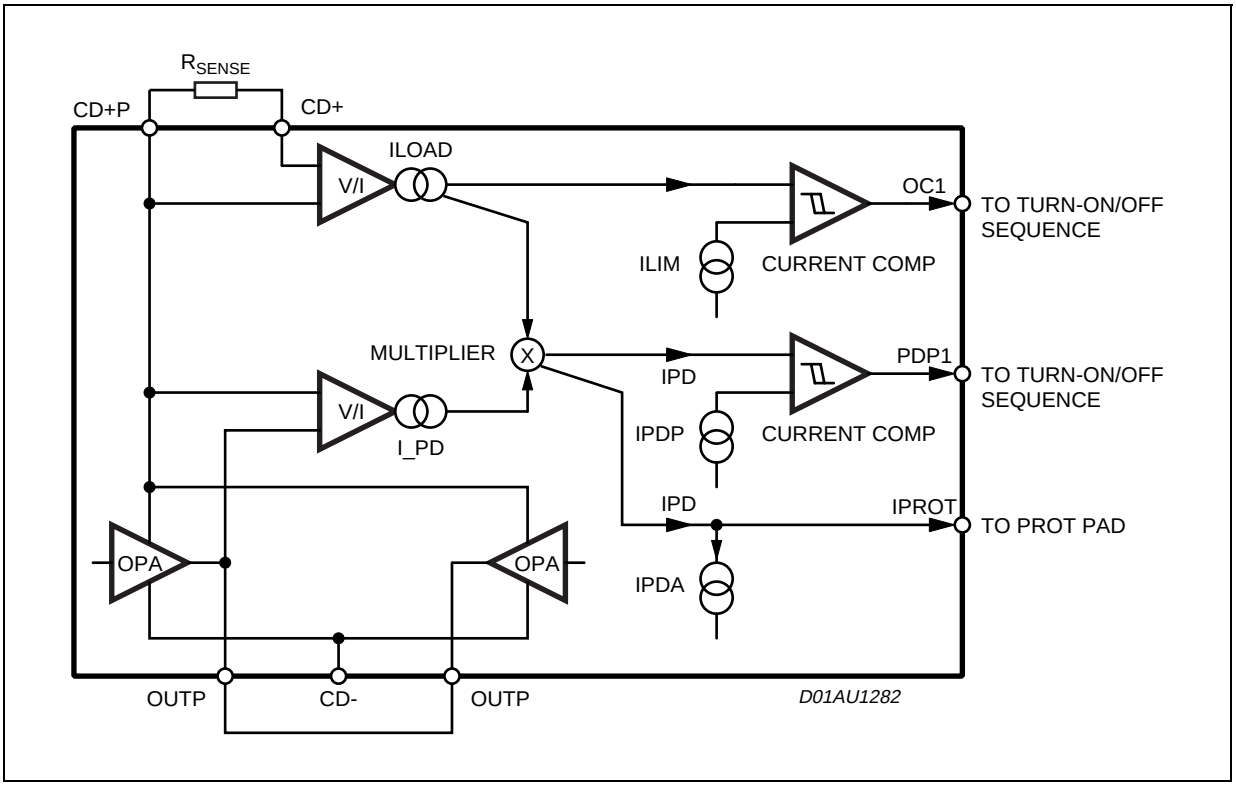
The Output bridge amplifier makes the single-ended to Differential conversion of the Audio signal using two power amplifiers, one in non-inverting configuration with gain equal to 2 and the other in inverting configuration with unity gain. To guarantee the high input impedance at the input pins, Pwr_Inp1 and Pwr_Inp2, the second amplifier stages are driven by the output of the first stages respectively.

POWER PROTECTION

To protect the output transistors of the power bridge a power detector is implemented (fig 3).

The current flowing in the power bridge and trough the series resistor Rsense is measured reading the voltage drop between CD+1 and CD+. In the same time the voltage drop on the relevant power (Vds) is internally measured. These two voltages are converted in current and multiplied: the resulting current , Ipd, is proportional to the instantaneous dissipated power on the relevant output transistor. The current Ipd is compared with the reference current Ipda, if bigger (dissipated power > 50W) a current, Iprot, is supplied to the Protection pin. The aim of the current Iprot is to reduce the reference voltage for the digital converter supplying the power stage of the chip, and than to reduce the dissipated power. The response time of the system must be less than 200µSec to have an effective protection. As further protection, when Ipd reaches an higher threshold (when the dissipated value is higher then 96W) the chip is shut down, forcing low the Stby/Mute pin, and the turn on sequence is restarted.

Figure 3. Power Protection Block Diagram



In fig. 4 there is the power protection strategy pictures. Under the curve of the 50W power, the chip is in normal operation, over 96W the chip is forced in Standby. This last status would be reached if the digital converter does not respond quikly enough reducing the stress to less than 96W.

The fig.5 gives the protection current, Iprot, behavior. The current sourced by the pin Prot follows the formula:

$$I_{prot} \equiv \frac{(P_d - P_{d_av_th}) \cdot 5 \cdot 10^{-4}}{1.25V}$$

for $P_d < P_{d_av_th}$ the $I_{prot} = 0$

Independently of the output voltage, the chip is also shut down in the folowing conditions:

When the currentthrough the sensing resistor, R_{sense}, reaches 12A (Voltage drop (CD+) - (CD+1) = 700mV).

When the average junction temperature of the chip reaches 150°C.

When the ground potential differ from more than 5V from the half of the power supply voltage, ((CD+)-(CD-))/2

When the sum of the supply voltage |Vs+| + |Vs-| <20V

The output bridge is muted when the average junction temperature reaches 130°C.

Figure 4. Power protection threshold

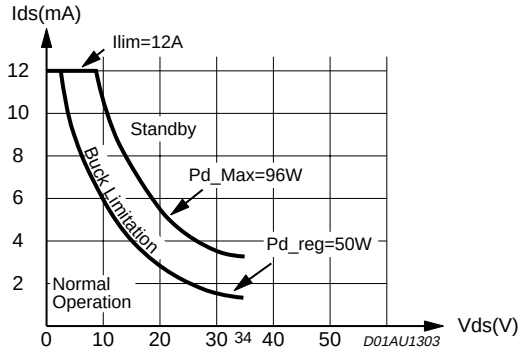


Figure 5. Protection current behaviour

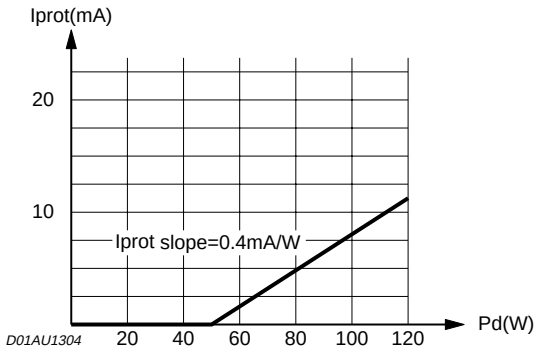
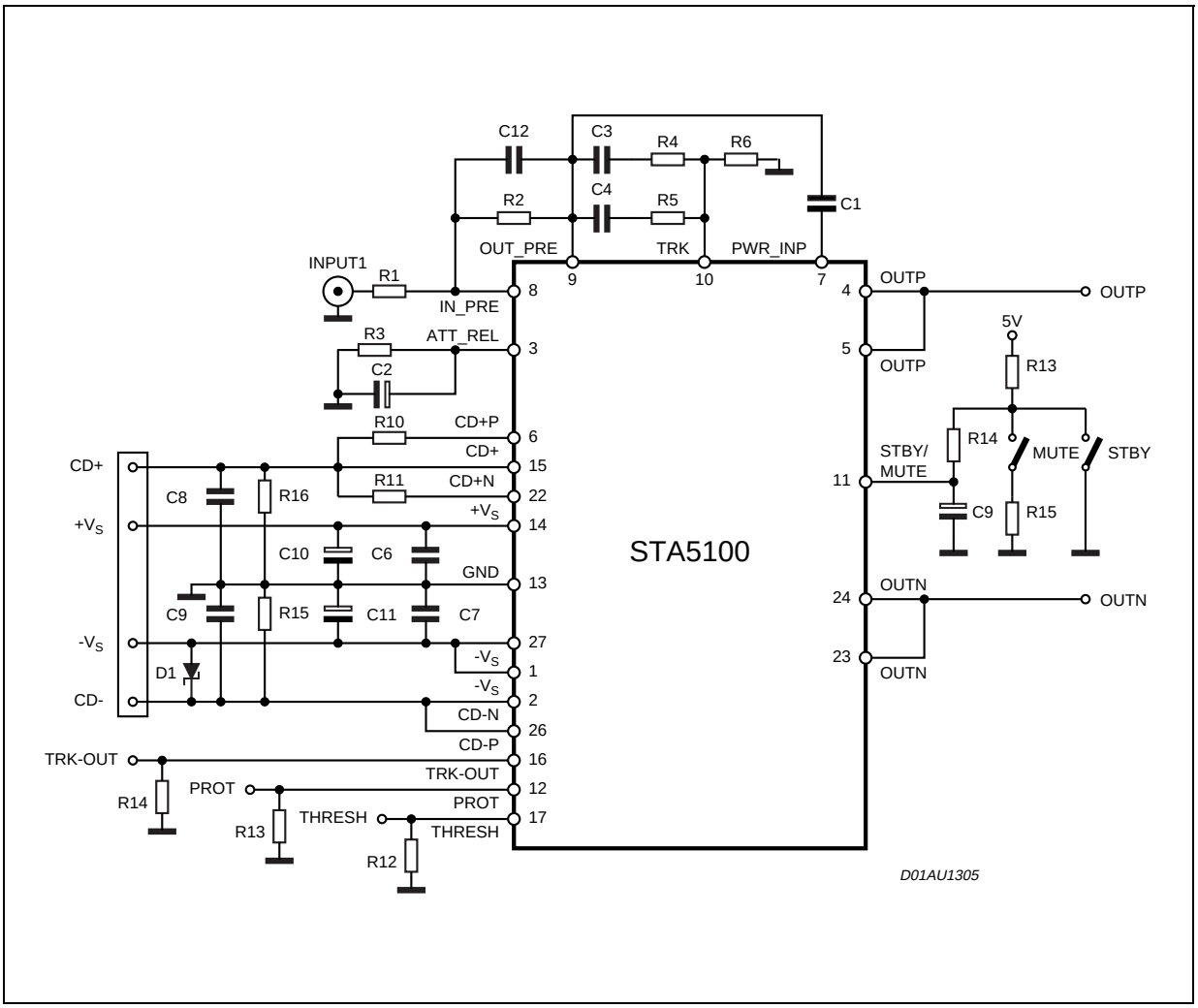


Figure 6. Test and Application Circuit



EXTERNAL COMPONENTS

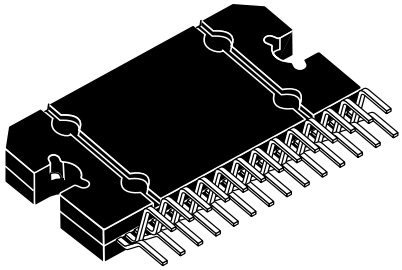
Name	Function	Value	Formula
Ri R1	Input resistor	10KΩ (|G| = 5, Rr = 50KΩ)	$R_i = \frac{Rr}{\|G\|}$
Rr R2	Feedback resistor	50KΩ (|G| = 5, Ri = 10KΩ	$Rr = \|G\| \cdot Rr$
Cac C1	AC Decoupling capacitor	100nF (fp = 16Hz, Rac =100KΩ)	$Cac = \frac{1}{2\pi \cdot fp \cdot Rac}$
Cct C2	Capacitor for the attack time	2.2µF (Tattack = 13mSec, Vcontrol = 9V, Ict = 1.5mA)	$Cct = attack\frac{Ict}{Vcontrol}$
R3	Release constant time Resistor	470KΩ (t = 1 Sec. , Cct = 2.2 µF)	$Rct = \frac{\tau}{Cct}$
R4	Resistor for tracking input voltage filter	10KΩ	
R5	Resistor for tracking input voltage filter	56KΩ	
R6	Resistor for tracking input voltage filter	10KΩ	
C3	Capacitor for Tracking input voltage filter	1nF	
C4	Dc decoupling capacitor	1µF	
R7	Bias Resistor for Stby/Mute function	10KΩ	
R8	Stby/Mute constant time resistor	30KΩ	
R9	Mute resistor	30KΩ	
C5	Capacitor for Stby/Mute resistor	2.2µF	
R10 = R11	Sensing resistor for SOA detector	60mΩ 5% 4W	
R12	Conversion resistor for threshold voltage	100KΩ	
C6 = C7	Power supply filter capacitor	100nF	
R15 = R16	Centering resistor	400 Ω , 1W	
C8 = C9	Tracking rail power supply filter	680nF	
R13	Protection	1KΩ	
R14	TRK_out	40KΩ	
C10 = C11	Power supply filter capacitor	470 µF , 63V	
C12	Feedback capacitor	100pF	
D1	Schottky diode	SB360	

Note: Vcontrol is the voltage at Att_Rel pin.

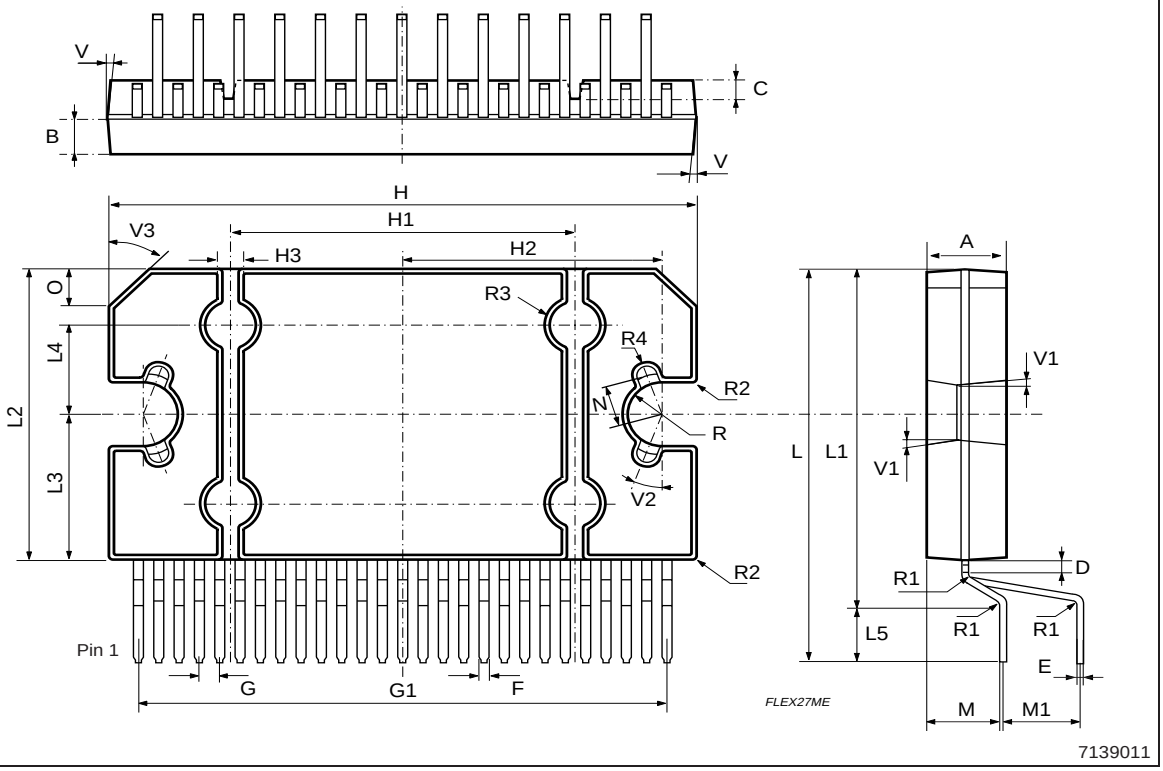
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



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