



STV6412A

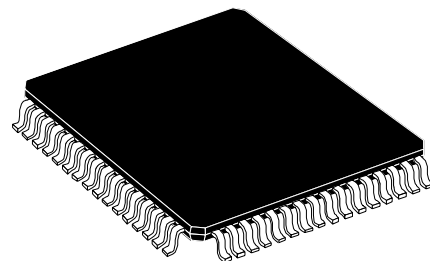
AUDIO/VIDEO SWITCH MATRIX

FEATURES

- I²C Bus Control
- Standby Mode with Interrupt Signal Output
- Video Section
 - 4 CVBS Inputs, 3 CVBS Outputs (one with Selectable Chroma Trap Filter)
 - 3 Y/C Inputs, 2 Y/C Outputs
 - 6 dB Gain on all CVBS/Y and C Outputs
 - Integrated 150 Ω Buffers
 - 1 Y/C Adder
 - 2 RGB/FB Inputs, 1 Tri-state RGB/FB Output with 6 dB Adjustable Gain (from +3dB to +9dB)
 - Video Muting on all Outputs
 - 2 Slow Blanking Inputs/Outputs
 - Sync Bottom Clamp on all CVBS/Y and RGB Inputs, Average Clamp on C Inputs
 - Bandwidth: 15 MHz
 - Crosstalk: 50 dB Minimum
- Audio Section
 - 4 Stereo Inputs, 3 Stereo Outputs
 - 1 Mono-Sound Output
 - Stereo-to-Mono Sound Capability
 - 0/6/9 dB Selectable Gain on one Stereo Input
 - Full Range Volume Control with Soft Control
 - Audio Muting on all Outputs

DESCRIPTION

The STV6412A is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides all the audio and video routings required in a full two SCART set-top box design.



TQFP64
(14 x 14 x 1.40 mm)
(Thin Full Plastic Quad Flat Pack)

ORDER CODE: STV6412ADT

Table of Contents

1 GENERAL OVERVIEW	3
1.1 PIN CONNECTIONS	3
2 ELECTRICAL CHARACTERISTICS	7
2.1 ABSOLUTE MAXIMUM RATINGS	7
2.1.1 Thermal Data	7
2.1.2 Latch Up	7
2.2 RECOMMENDED OPERATING CONDITIONS	7
2.3 AUDIO SECTION CHARACTERISTICS	8
2.4 VIDEO SECTION CHARACTERISTICS	9
2.5 CHROMA SECTION CHARACTERISTICS	10
2.6 BLANKING SECTION	10
2.7 I ² C BUS CHARACTERISTICS	12
3 I²C BUS SELECTION	13
3.1 I ² C BUS ADDRESSES	13
3.2 POWER-ON RESET — BUS REGISTER INITIAL CONDITIONS	17
4 INPUT/OUTPUT GROUPS	19
5 APPLICATION DIAGRAM	22
6 PACKAGE MECHANICAL DATA	23

1 GENERAL OVERVIEW

1.1 PIN CONNECTIONS

Figure 1. Pinout Diagram

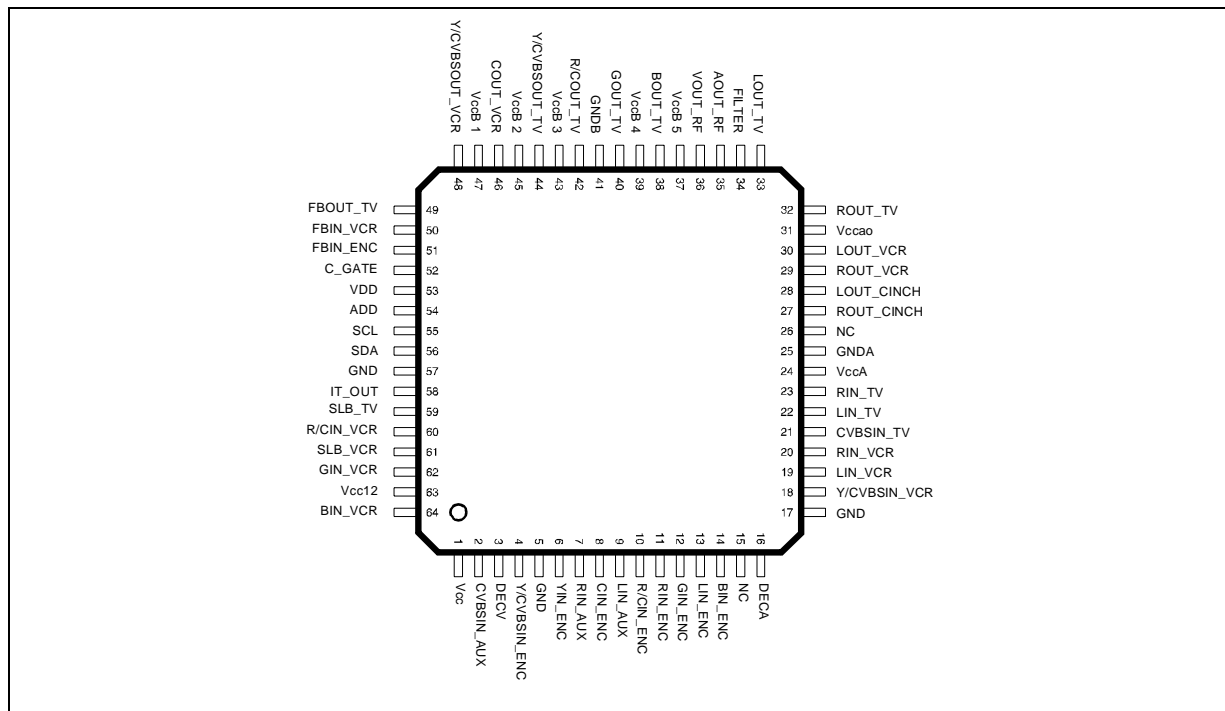


Figure 2. Pin Description

Pin No.	Symbol	Description
1	V _{CC}	+5 V Supply
2	CVBSIN_AUX	CVBS Input from Auxiliary
3	DECV	Video Decoupling Capacitor
4	Y/CVBSIN_ENC	Y/CVBS Input from Encoder
5	GND	Ground
6	YIN_ENC	Y Input from Encoder
7	RIN_AUX	Audio Right Input from Auxiliary
8	CIN_ENC	Chroma Input from Encoder
9	LIN_AUX	Audio Left, Input from Auxiliary
10	R/CIN_ENC	Red/Chroma Input from Encoder
11	RIN_ENC	Audio Right, Input from Encoder
12	GIN_ENC	Green Input from Encoder
13	LIN_ENC	Audio Left, Input from Encoder
14	BIN_ENC	Blue Input from Encoder
15	NC	Not Connected
16	DECA	Audio Decoupling Capacitor
17	GND	Ground
18	Y/CVBSIN_VCR	Y/CVBS Input from VCR SCART
19	LIN_VCR	Audio Left, Input from VCR SCART

STV6412A

Pin No.	Symbol	Description
20	RIN_VCR	Audio Right, Input from VCR SCART
21	CVBSIN_TV	CVBS Input from TV SCART
22	LIN_TV	Audio Left, Input from TV SCART
23	RIN_TV	Audio Right, Input from TV SCART
24	V _{CCA}	Audio Supply Voltage - or - Audio Supply Decoupling
25	GNDA	Audio Ground
26	NC	Not Connected
27	ROUT_CINCH	Audio Right Output to Cinch
28	LOUT_CINCH	Audio Left Output to Cinch
29	ROUT_VCR	Audio Right Output to VCR SCART
30	LOUT_VCR	Audio Left Output to VCR SCART
31	V _{CCA0}	Audio Output Supply Voltage - or - Main Audio Supply Voltage
32	ROUT_TV	Audio Right Output to TV SCART
33	LOUT_TV	Audio Left Output to TV SCART
34	FILTER	Chroma Trap Filter
35	AOUT_RF	Audio (L+R) Output to RF Modulator
36	VOUT_RF	CVBS Video Output to RF Modulator
37	V _{CCB5}	Video Output Buffer Supply Pin
38	BOUT_TV	Blue Output to TV SCART
39	V _{CCB4}	Video Output Buffer Supply Pin
40	GOUT_TV	Green Output to TV SCART
41	GNDB	Video Buffer Ground
42	R/COUT_TV	Red/Chroma Output to TV SCART
43	V _{CCB3}	Video Output Buffer Supply Pin
44	Y/CVBSOUT_TV	Y/CVBS Output to TV SCART
45	V _{CCB2}	Video Output Buffer Supply Pin
46	COUT_VCR	Chroma Output to VCR SCART
47	V _{CCB1}	Video Output Buffer Supply Pin
48	Y/CVBSOUT_VCR	Y/CVBS Output to VCR SCART
49	FBOUT_TV	Fast Blanking Output to TV SCART
50	FBIN_VCR	Fast Blanking Input from VCR SCART
51	FBIN_ENC	Fast Blanking Input from Encoder
52	C_GATE	External MOS Command for C_VCR bidirectional mode
53	V _{DD}	+5 V I ² C Supply
54	ADD	I ² C Address Selection
55	SCL	I ² C Bus Clock
56	SDA	I ² C Bus Data
57	GND	Ground Digital
58	IT_OUT	Interrupt Output
59	SLB_TV	Slow Blanking Input/Output from TV SCART
60	R/CIN_VCR	Red Input (or C Input) from VCR SCART
61	SLB_VCR	Slow Blanking Input/Output from VCR SCART
62	GIN_VCR	Green Input from VCR SCART
63	V _{CC12}	+12 V Supply
64	BIN_VCR	Blue Input from VCR SCART

Figure 3. STV6412A Block Diagram

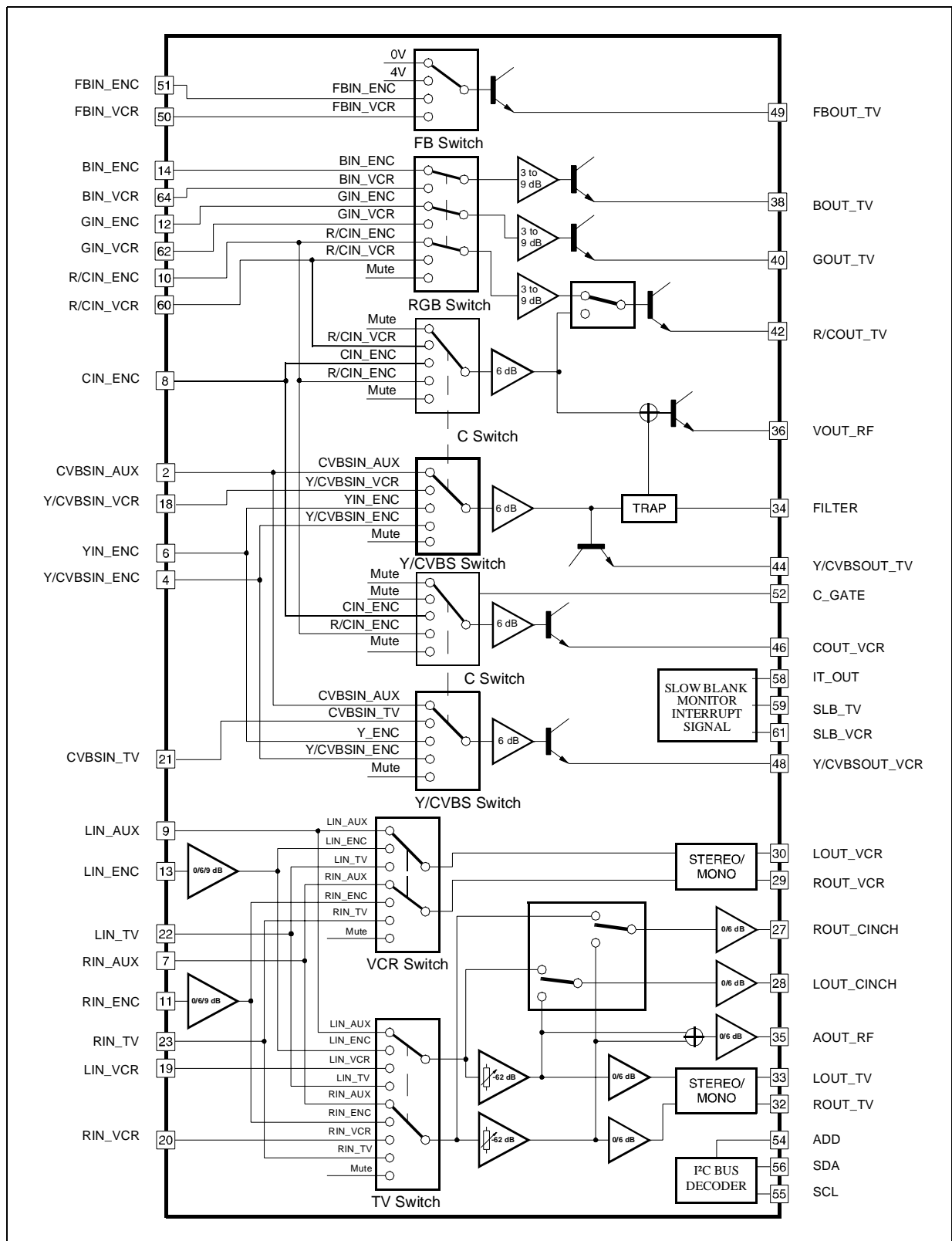
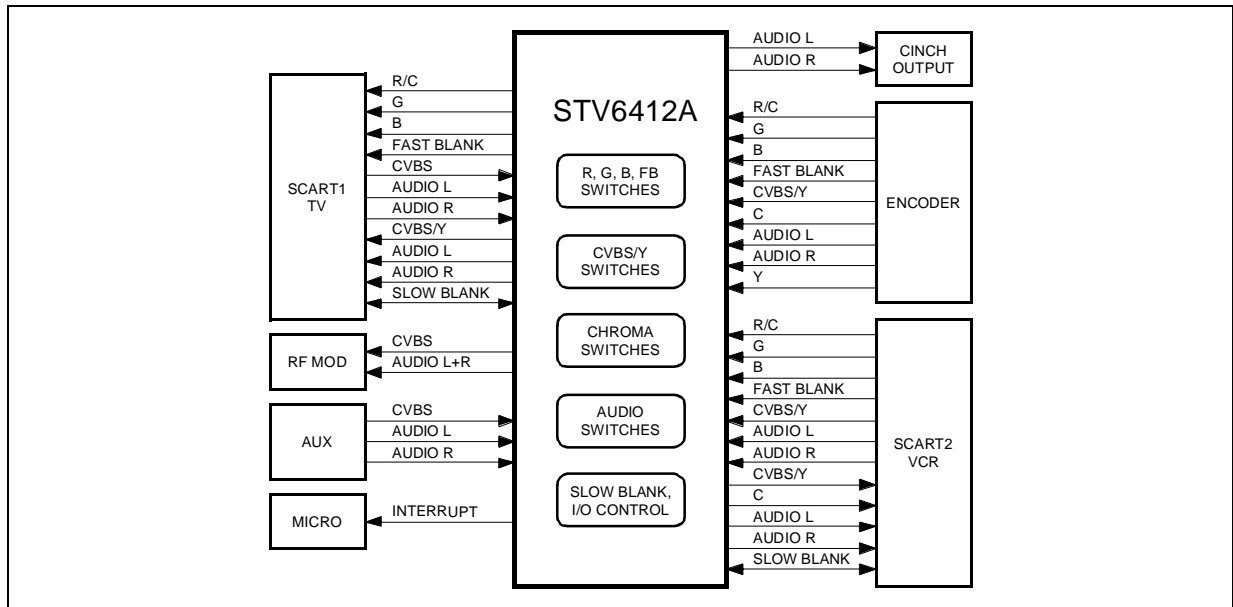


Figure 4. Functional Block Diagram



2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units	
V_{CC12}	Supply voltage for:	- Slow blanking sections	13.2	V
V_{CCAO}		- Audio drivers	13.2	V
V_{CCA}		- Internal Digital Audio parts	10	V
V_{DD}		- Digital parts	6	V
V_{CC}, V_{CCBi}		- Video sections	6	V
V_I	Voltage at Pin I to GND:	- Audio pins	0, V_{CCA}	V
		- Video pins	0, V_{CC} or V_{CCBi}	V
		- Bus pins	0, 5.5	V
		- Slow blanking pins	0, V_{CC12}	V
V_{ESD}	Maximum ESD voltage allowed. 100 pF capacitor discharged through 1.5 k Ω serial resistor (Human Body Model)	± 4	kV	
T_{oper}	Operating Ambient Temperature	0, +70	$^{\circ}C$	
T_{stg}	Storage Temperature	-20, +150	$^{\circ}C$	

2.1.1 Thermal Data

Symbol	Parameter	Value	Units
$R_{th(j-a)}$	Junction-ambient Thermal Resistance (Maximum)	48	$^{\circ}C/W$

2.1.2 Latch Up

At an ambient temperature of 25 $^{\circ}C$, all pins meet the following specifications:

- I trigger = 200 mA or I trigger = 200 mA.
- Pin 58 (IT_OUT) does not meet this specification and the trigger current must be limited to -100 mA.

2.2 Recommended Operating Conditions

$T_{amb} = 25^{\circ}C$, $V_{CCAO} = 12 V$, $V_{CC} = 5 V$, $V_{CC12} = 12 V$, $V_{DD} = 5 V$

$R_{GA} = 600 \Omega$, $R_{LOUTA} = 10 k\Omega$, $R_{GV} = 50 \Omega$, $R_{LOUTV} = 150 \Omega$, unless otherwise specified.

Table 1. Supply Voltages

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DD}	Digital Supply Voltage		4.75	5	5.25	V
V_{CCAO}	Audio Operating Supply Voltage	- Decoupling capacitor on V_{CCA}	11.2	12	12.8	V
		- Connected to V_{CCA}	8.5	9	9.5	V
V_{CC}	Video Operating Supply Voltage		4.75	5	5.25	V
V_{CC12}	Slow Blanking Control Supply Voltage		11.2	12	12.8	V

Table 2. Active Mode (All channels ON)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{DD}	Digital Supply Current	$V_{DD} = 5 V$		4.5	10	mA
I_{CCA}	Audio Supply Current	$V_{CCAO} = 12 V$, no load		9	15	mA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{CCV}	Total Video Supply Current ($V_{CC}+V_{CCB1}+V_{CCB2}+V_{CCB3}+V_{CCB4}+V_{CCB5}$)	$V_{CC} = 5\text{ V}$, no load		43	60	mA
I_{CC12}	12 V Supply Current	$V_{CC12} = 12\text{ V}$ SLB input mode SLB output mode, no load		0 2.5	1 4	mA

Table 3. Standby Mode (All channels OFF)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{DD}	Digital Supply Current	$V_{DD} = 5\text{ V}$		4.5	10	mA
I_{CCAstd}	Audio Supply Current	$V_{CCA0} = 12\text{ V}$, no load		3		mA
I_{CCVstd}	Total Video Supply Current	$V_{CC} = 5\text{ V}$		1		mA

2.3 Audio Section Characteristics

$T_{amb} = 25^{\circ}\text{C}$, $V_{CCA0} = 12\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{CC12} = 12\text{ V}$, $V_{DD} = 5\text{ V}$

$R_{GA} = 600\ \Omega$, $R_{LOUTA} = 10\text{ k}\Omega$, $R_{GV} = 50\ \Omega$, $R_{LOUTV} = 150\ \Omega$, unless otherwise specified.

Table 4. Audio Section Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SVR100	Supply Voltage Rejection	$V_{RIPPLE} = 500\text{m } V_{RMS}$ at $f = 100\text{ Hz}$, Gain = 0 dB, DECA filter cap = 47 μF DECA filter cap = 220 μF	60	70 80		dB dB
SVR1K	Supply Voltage Rejection	$V_{RIPPLE} = 500\text{m } V_{RMS}$ at $f = 1\text{ kHz}$, Gain = 0 dB	70	80		dB
V_{INDC}	Input DC Level	$V_{CCA} = 9\text{ V}$		$V_{CCA}/2$		V
V_{INAC}	Input Signal Amplitude				2	V_{RMS}
R_{IN}	Input Resistance		30	50		$\text{k}\Omega$
$R_{INmatch}$	Input Resistance Matching			± 2	± 10	%
F_{RANGE}	Bandwidth	-3 dB, 0.5 V_{RMS} , $R_{LOAD} = 10\text{ k}\Omega$, Gain = 0 dB	50			kHz
Flatness	Spread of Gain in Audio Band	-0.5 V_{RMS} , 20 Hz to 20 kHz, Gain = 0 dB			0.5	dB
CS	Channel Separation, from audio in-puts Between L & R of TV outputs	$V_{IN} = 0.5\text{ } V_{RMS}$, $f = 1\text{ kHz}$, on one in-put, $R_{LOAD} = 10\text{ k}\Omega$, Gain = 0 dB	80 70	90 74		dB dB
C_i	Channel Isolation from video inputs	$V_{IN} = 1\text{ } V_{pp}$, $f = 15\text{ kHz}$, on one point		85		dB
V_{OUT}	Output DC Level	$V_{CCA} = 9\text{ V}$		$V_{CCA}/2$		V
V_{OFF}	DC Offset Change	Switching between inputs		1	± 15	mV
R_{OUT}	Output Resistance			60	120	W
PHD	Phase Difference	$f = 1\text{ kHz}$, 1 V_{RMS} input on each input channel			3	$^{\circ}\text{ deg.}$
ASN	S/N Ratio	$f = 1\text{ kHz}$, 1 V_{RMS} input (gain = 0dB) weighted CCIR 468-4 quasi peak	70			dB
eNI	Equivalent RMS Input Voltage Noise	BW = 20 Hz, 20 kHz Flat, Gain = 0 dB		5		μV
G0	0 dB Gain	0.5 V_{RMS} , $R_{LOAD} = 10\text{ k}\Omega$, Gain = 0 dB	-0.5		+0.5	dB

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
G _{STEP}	Gain Step	-62 dB to +6 dB (see Figure 2)		2		dB
G _{MATCH1}	Gain matching between different inputs of one output	V _{IN} = 0.5 V _{RMS} , 1 kHz, Gain = 0 dB	-0.5		0.5	dB
G _{MATCH2}	Gain matching between Left/Right outputs of one input channel	V _{IN} = 0.5 V _{RMS} , 1 kHz, Gain = 0 dB	-0.5		0.5	dB
THD0 THD6 THD9	Total Harmonic Distortion ENC Input at 0 dB ENC Input at 6 dB ENC Input at 9 dB	V _{OUT} = 0.5 V _{RMS} , 1 kHz, LPF @ 80 kHz		0.01 0.01 0.01	0.1 0.1 0.1	% % %
V _{CL}	Output Clipping Level	THD = 0.2%, 1 kHz	2.1	2.3		V _{RMS}
R _L	Output Load Resistance	V _{IN} = 1 V _{RMS} , THD = 0.3%, Gain = 0 dB	2	2.25		kΩ
Mute	Mute Suppression	V _{IN} = 0.5 V _{RMS} , on one point	-90			dB

2.4 Video Section Characteristics

T_{amb} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 5. Video Section Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{DCIN}	DC Input Level	Bottom Synch Pulse		2		V
I _{CLAMP}	Clamping Current	at V _{DCIN} -400 mV	1	2		mA
I _{LEAK}	Input Leakage Current	V _{IN} = V _{DCIN} +1 V		1	10	μA
C _{IN}	Input Capacitance			2		pF
V _{IN}	Max Input Signal	V _{CC} = 5 V		1.5		V _{PP}
DYN	Dynamic Output Signal	V _{CC} = 5 V		3		V _{PP}
BW	Bandwidth at -3 dB Y/CVBS RGB Y/C Mixer (on VOUT-RF)	V _{IN} = 1 V _{PP} V _{IN} = 1 V _{PP} V _{IN} = 1 V _{PP} , V _{INC} = muted	12 12 8	15 15 10		MHz MHz MHz
Flatness	Spread of Gain in Video Band (15 kHz - 5 MHz) Y/CVBS RGB Y/C Mixer (on VOUT-RF)	V _{IN} = 1 V _{PP} V _{IN} = 1 V _{PP} V _{IN} = 1 V _{PP} , V _{INC} = muted			+/-0.5 +/-0.5 +/-1.5	dB dB dB
CTi	Crosstalk Isolation between Input Channel	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one point		60		dB
CTo	Crosstalk Isolation between Output Channel	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one point, R _{LOAD} = 150Ω		50		dB
R _{OUT}	Output Resistance			5	10	Ω
G _{RGB}	Gain at RGB outputs	V _{IN} = 1 V _{pp} , gain set to 6 dB	5.5	6	6.5	dB
G _{RGBM}	Gain matching between R, G, B	V _{IN} = 1 V _{PP} , gain set to 6 dB	-0.3	0	0.3	dB
G _{RGBSTEP}	Step of Gain	3 dB to 6 dB	0.75	1	1.25	dB
G _{YCVBS}	Gain on Y, /CVBS channels	V _{IN} = 1 V _{PP}	5.5	6	6.5	dB
G _{YCVBSM}	Gain matching between Y, CVBS inputs	V _{IN} = 1 V _{PP}	-0.5	0	0.5	dB

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
DC _{OUT}	DC Output Voltage	Bottom sync pulse		0.6		V
DC _{OUT RF}	RF Output Voltage	Bottom sync pulse		1		V
DPHI	Differential Phase	V _{IN} = 1 V _{PP} at f = 4.43 MHz		1	5	° deg.
DG	Differential Gain	V _{IN} = 1 V _{PP} at f = 4.43 MHz		1	5	%
Mute	Mute Suppression	V _{IN} = 1 V _{PP} at f = 5 MHz on one point	-55			dB
LNL	Luminance non-linearity			0.3	3	%
VSN	Video S/N Ratio	Refer to Note 1	65			dB

Note 1: S/N = 20 log (V_{OUT} Black to White = 0.7 V_{PP} / V_{Noise} (mV_{RMS}) weighted CCIR 567).

2.5 Chroma Section Characteristics

T_{amb} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 6. Chroma Section Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{DCIN}	DC Input Level			3		V
R _{IN}	Input Resistance		30	50		kΩ
C _{IN}	Input Capacitance			2		pF
V _{IN}	Max Input Signal			1.5		V _{PP}
DYN	Dynamic Output Signal			3		V _{PP}
DC _{OUT}	DC Output VCR Voltage			2.2		V
CBW	Chroma Bandwidth	C _{IN} = 1 V _{PP} at -3 db	10			MHz
CTi	Crosstalk Isolation between Input Channel	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one input		55		dB
CTo	Crosstalk Isolation between Output Channel	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one input, R _{LOAD} = 150 Ω		50		dB
R _{OUT}	Output Resistance			5	10	W
G _{OUTC}	Gain at OUTC	V _{IN} = 1 V _{pp}	5.5	6	6.5	dB
G _{CM}	Gain matching between C inputs	V _{IN} = 1 V _{PP}	-0.5	0	0.5	dB
Mute	Mute Suppression	V _{IN} = 1 V _{PP} at f = 4.43 MHz, on one input	-55			dB
CToYdel	Chroma to luma delay, source Y/C	Pin other than VOUT_RF, V _{PP} @ 4.43 MHz,			20	ns
CToYdel	Chroma to luma delay, source Y/C	Pin VOUT_RF			20	ns

2.6 Blanking Section

T_{amb} = 25 °C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600 Ω, R_{LOUTA} = 10 kΩ, R_{GV} = 50 Ω, R_{LOUTV} = 150 Ω, unless otherwise specified.

Table 7. Slow Blanking Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
INPUT MODE						
SLBlow	Input Low Level Threshold		2.5	3.25	4	V
SLBhigh	Input High Level Threshold		7.5	8.25	9	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{IN}	Input Current			50	100	μ A

OUTPUT MODE

SLB _{low}	Output Low Level (int. TV)		0	0.02	1.5	V
SLB _{med}	Output Medium Level (ext. 16/9)		5	5.75	6.5	V
SLB _{high}	Output High Level (ext. 4/3)		10	11	12	V

Table 8. Fast Blanking Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	-------

INPUT MODE

FB _{low/high}	Input Low/High Level Threshold		0.4	0.7	0.9	V
I_{IN}	Input Current			2	10	μ A

OUTPUT MODE

FB _{LOW}	Output Low Level	$R_{LOAD} = 150 \Omega$	3.0	3.4	0.5	V
FB _{HIGH}	Output High Level				3.8	V
FB _{DEL}	Fast Blanking RGB delay	At 50% on digital RGB transients, at 2 V on FB rise transient, at 1 V on FB fall, $C_{LOAD} = 10$ pF maximum		15		ns
FB _{TRANS}	FB Transitions at FB output Rise Time Fall Time	$C_{LOAD} = 10$ pF maximum between 10% and 90% between 90% and 10%		10		ns
				10		ns

Table 9. C_Gate Function Output

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_GATE-H	Pull-up Resistor Value to V_{CCB1}			20		k Ω
C_GATE-L	Output Low Level	$I_{IN} = 0$ mA $I_{IN} = 1$ mA			0.3	V
					0.7	V

Table 10. Interrupt Output (Refer to Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
IT-Leak	High Level Leakage	External pull-up to 5 V			10	μ A
IT-Low	Output Low Level (Active)	$I_{IN} = 0$ mA $I_{IN} = 1$ mA			0.3	V
					0.7	V

Table 11. Address Selection Input

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
ADDsel_L	Address Selection Low Level			0	0.2	V
ADDsel_H	Address Selection High Level		2.5		V_{DD}	V
I_{LEAK}	Leakage Current				10	μ A

Note 2: The interrupt is forced to a low level when a change is detected on slow blanking inputs. It can be used in Standby mode to wake up the microprocessor. It is released when the I²C bus register is read.

2.7 I²C Bus Characteristics

T_{amb} = 25°C, V_{CCAO} = 12 V, V_{CC} = 5 V, V_{CC12} = 12 V, V_{DD} = 5 V

R_{GA} = 600Ω, R_{LOUTA} = 10kΩ, R_{GV} = 50Ω, R_{LOUTV} = 150Ω, unless otherwise specified.

Table 12. I²C Bus Characteristics

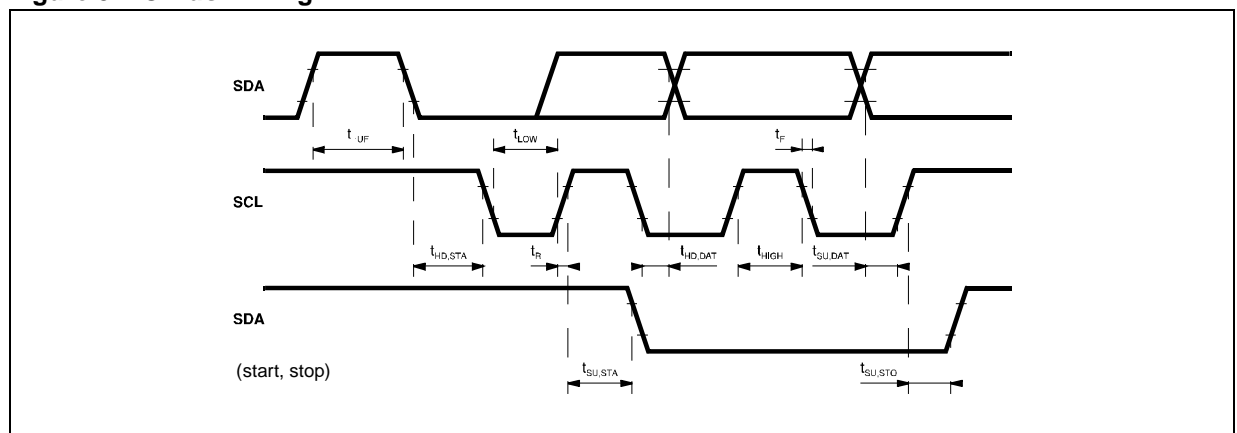
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SCL						
V _{IL}	Low Level Input Voltage		-0.3		1.5	V
V _{IH}	High Level Input Voltage		2.3		5.5	V
I _{LI}	Input Leakage Current	V _{IN} = 0 to 5.5 V	-10	0	10	μA

SDA						
V _{IL}	Low Level Input Voltage		-0.3		1.5	V
V _{IH}	High Level Input Voltage		2.3		5.5	V
I _{LI}	Input Leakage Current	V _{IN} = 0 to 5.5 V	-10	0	10	μA
C _I	Input Capacitance				10	pF
t _R	Input Rise Time	1.5 V to 3 V			1	μs
t _F	Input Fall Time	3 V to 1.5 V			300	ns
V _{OL}	Low Level Output Voltage	I _{OL} = 3 mA			0.4	V
t _F	Output Fall Time	3 V to 1.5 V			250	ns
C _L	Load Capacitance				400	pF

TIMING						
t _{LOW}	Clock Low Period		4.7			μs
t _{HIGH}	Clock High Period		4			μs
t _{SU,DAT}	Data Setup Time		250			ns
t _{HD,DAT}	Data Hold Time		0		340	ns
t _{SU,STO}	Setup Time from Clock High to Stop		4			μs
t _{BUF}	Start Setup Time following a Stop		4.7			μs
t _{HD,STA}	Start Hold Time		4			μs
t _{SU,STA}	Start Setup Time following Clock Low to High Transition		4.7			μs

Note 3: The device can also operate at 400 kHz and is capable of interfacing with +3.3 V or + 5 V logic levels.

Figure 5. I²C Bus Timing



3 I²C BUS SELECTION

Data transfers follow the usual I²C format; i.e. after the start condition (S), a 7-bit slave address is sent, followed by an eight-bit data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The IC's I²C bus decoder enables the automatic incrementation mode in write mode.

String Format

Write only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	SLAVE ADDRESS	0	A	SUB-ADDRESS	A	DATA	A	P
---	---------------	---	---	-------------	---	------	---	---

Read only mode

S	SLAVE ADDRESS	1	A	DATA	A	P
---	---------------	---	---	------	---	---

Slave Address

Address	A6	A5	A4	A3	A2	A1	A0
Value	1	0	0	1	0	1	X

Auto Increment Mode

S	SLAVE ADDRESS	0	A	SUB-ADDRESS	A	DATA0	A	DATA1	A	DATAn	A	P
				Sub-Address		Sub-Address + 1		Sub-Address + N					

3.1 I²C Bus Addresses

Write Address: 1001 01X0, Read Address: 1001 01X1

Address Selection Pin Grounded: X = 0, write address = 94(hex), read address = 95(hex)

Address Selection Pin to Supply: X = 1, write address = 96(hex), read address = 97(hex)

Table 13. Input Signal Summary (Write Mode)

Reg Addr (Hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0

AUDIO

00	TV Stereo Mono	TV 0/6 dB	TV Volume-62 dB to 0 dB - 2 dB steps				Soft Volume Mode	
01	VCR Stereo Mono	Not Used	VCR Audio Switch Control		CINCH Audio Gain	TV/CINCH Audio Switch Control		

VIDEO

02	VCR Chroma muted	VCR Video and Chroma Switch Control			TV Chroma muted	TV Video and Chroma Switch Control		
03	RGB and FB Tri-state	RGB Gain			RGB Switch Control		Fast Blanking Mode/Input Selection	

MISCELLANEOUS

04	IT Enable	SLB Mode	Not Used	VCR-C Output Control	VCR-C Gate Control	RF Trap Filter Control	RF Adder Control	TV R or C Output Selection
05	VCR Slow Blanking		TV Slow Blanking		ENC Audio Input Gain 0/6/9 dB		VCR R/C sub Clamp	ENC R/C sub Clamp

STB-BY

06	RF Outputs	TV Outputs	CINCH Outputs	VCR Outputs	AUX Inputs	TV Inputs	VCR Inputs	ENC Inputs
----	------------	------------	---------------	-------------	------------	-----------	------------	------------

Note 4: Unused data must be set to "0".

Table 14. TV Audio Output

Reg. Addr (Hex)	Description	Bits	Data								Comments	
			d7	d6	d5	d4	d3	d2	d1	d0		
00	Soft Volume Change	1	X	X	X	X	X	X	X	X	0 1	Active Disabled
	Level Adjustment	5	X	X	0	0	0	0	0	X	0 dB -62 dB (-2 dB/step)	
	6 dB Extra Gain	1	X	0	X	X	X	X	X	X	0 dB +6 dB	
	TV Stereo or Mono Mode	1	0	X	X	X	X	X	X	X	0 = Stereo 1 = Mono	

Table 15. Audio Selection & VCR Audio Output

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
01	TV & CINCH Audio Output Selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	Encoder L/R selected
			X	X	X	X	X	0	1	0	VCR L/R selected
			X	X	X	X	X	0	1	1	AUX L/R selected
			X	X	X	X	X	1	0	0	TV L/R selected
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
	CINCH Audio Gain	1	X	X	X	X	0	X	X	X	0 dB
			X	X	X	X	1	X	X	X	Follow TV Gain
	VCR Audio Output Selection	2	X	X	0	0	X	X	X	X	Muted
X			X	0	1	X	X	X	X	Encoder L/R selected	
X			X	1	0	X	X	X	X	TV L/R selected	
VCR Stereo or Mono Mode	1	0	X	X	X	X	X	X	X	0 = Stereo	
		1	X	X	X	X	X	X	X	1 = Mono	

Table 16. TV & VCR Video Selection

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
02	TV Video Output Selection	3	X	X	X	X	X	0	0	0	Y/CVBS muted & Chroma muted
			X	X	X	X	X	0	0	1	Y/CVBS_ENC & R/C_ENC
			X	X	X	X	X	0	1	0	Y_ENC & C_ENC
			X	X	X	X	X	0	1	1	Y/CVBS_VCR & R/C_VCR
			X	X	X	X	X	1	0	0	CVBS_AUX & Chroma muted
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
	TV Chroma Output Control	1	X	X	X	X	0	X	X	X	Chroma defined by d2d1d0
			X	X	X	X	1	X	X	X	Chroma force to mute
	VCR Video Output Selection	3	X	0	0	0	X	X	X	X	Y/CVBS muted & Chroma muted
			X	0	0	1	X	X	X	X	Y/CVBS_ENC & R/C_ENC
			X	0	1	0	X	X	X	X	Y_ENC & C_ENC
X			0	1	1	X	X	X	X	CVBS_TV & Chroma muted	
X			1	0	0	X	X	X	X	CVBS_AUX & Chroma muted	
X			1	0	1	X	X	X	X	Not allowed	
X			1	1	0	X	X	X	X	Not allowed	
VCR Chroma Output Control	1	0	X	X	X	X	X	X	X	Chroma defined by d6d5d4	
		1	X	X	X	X	X	X	X	Chroma force to mute	

Table 17. RGB & Fast Blanking Outputs

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
03	Fast Blanking Control	2	X	X	X	X	X	X	0	0	FB forced to low level
			X	X	X	X	X	X	0	1	FB forced to high level
			X	X	X	X	X	X	1	0	FB from Encoder
			X	X	X	X	X	X	1	1	FB from VCR
	RGB Selection	2	X	X	X	X	0	0	X	X	Muted
			X	X	X	X	0	1	X	X	RGB_ENC selected
			X	X	X	X	1	0	X	X	RGB_VCR selected
			X	X	X	X	1	1	X	X	Not allowed
	RGB Gain	2	X	X	0	0	X	X	X	X	+6 dB gain
			X	X	0	1	X	X	X	X	+5 dB gain
			X	X	1	0	X	X	X	X	+4 dB gain
			X	X	1	1	X	X	X	X	+3 dB gain
RGB and Fast Blanking Control	1	X	0	X	X	X	X	X	X	+0 dB extra gain	
		X	1	X	X	X	X	X	X	+3 dB for weak input signals	
RGB and Fast Blanking Control	1	0	X	X	X	X	X	X	X	RGB and FB outputs high impedance state	
		1	X	X	X	X	X	X	X	RGB and FB outputs active	

Table 18. RF & Miscellaneous Control

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
04	R/C TV Output Selection	1	X	X	X	X	X	X	X	0	Red signal selected
			X	X	X	X	X	X	X	1	Chroma signal selected
	RF Output: Adder control and chroma sub-carrier filter selection	2	X	X	X	X	X	X	0	X	CVBS to RF output
			X	X	X	X	X	X	1	X	Y + C to RF output
			X	X	X	X	X	0	X	X	Filter not active
			X	X	X	X	X	1	X	X	Filter active
C_Gate Output Control	1	X	X	X	X	0	X	X	X	High level	
		X	X	X	X	1	X	X	X	Low level	
C_VCR Output Control	1	X	X	X	0	X	X	X	X	Tri-state mode (high impedance)	
		X	X	X	1	X	X	X	X	Active	
Slow Blanking Mode	1	X	0	X	X	X	X	X	X	Normal Mode	
		X	1	X	X	X	X	X	X	SLB TV is driven by SLB VCR	
IT Enable	1	0	X	X	X	X	X	X	X	No interrupt flag	
		1	X	X	X	X	X	X	X	IT enable	

Table 19. Slow Blanking & Inputs Control

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
05	Encoder R/Csub Clamp	1	X	X	X	X	X	X	X	0	Bottom level clamp
			X	X	X	X	X	X	X	1	Average level clamp
	VCR R/Csub Clamp	1	X	X	X	X	X	X	0	X	Bottom level clamp
			X	X	X	X	X	X	1	X	Average level clamp
	Encoder Input Level Adjustment	2	X	X	X	X	0	0	X	X	0 dB for normal audio inputs
			X	X	X	X	0	1	X	X	+6 dB for weak audio inputs
			X	X	X	X	1	0	X	X	+9 dB for weak audio inputs
	Slow Blanking TV SCART	2	X	X	0	0	X	X	X	X	Input mode only
			X	X	0	1	X	X	X	X	Output < 2 V
			X	X	1	0	X	X	X	X	Output 16/9 format
		X	X	1	1	X	X	X	X	Output 4/3 format	
Slow Blanking VCR SCART	2	0	0	X	X	X	X	X	X	Input mode only	
		0	1	X	X	X	X	X	X	Output < 2 V	
		1	0	X	X	X	X	X	X	Output 16/9 format	
		1	1	X	X	X	X	X	X	Output 4/3 format	

Table 20. Standby Modes

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
06	ENC Inputs	1	X	X	X	X	X	X	X	0	Inputs active
			X	X	X	X	X	X	X	1	Inputs disabled
	VCR Inputs	1	X	X	X	X	X	X	0	X	Inputs active
			X	X	X	X	X	X	1	X	Inputs disabled
	TV Inputs	1	X	X	X	X	X	0	X	X	Inputs active
			X	X	X	X	X	1	X	X	Inputs disabled
	AUX Inputs	1	X	X	X	X	0	X	X	X	Inputs active
			X	X	X	X	1	X	X	X	Inputs disabled
	VCR Outputs	1	X	X	X	0	X	X	X	X	Audio & Video Outputs ON
X			X	X	1	X	X	X	X	Audio & Video Outputs OFF	
CINCH Outputs	1	X	X	0	X	X	X	X	X	Audio & Video Outputs ON	
		X	X	1	X	X	X	X	X	Audio & Video Outputs OFF	
TV Outputs	1	X	0	X	X	X	X	X	X	Audio & Video Outputs ON	
		X	1	X	X	X	X	X	X	Audio & Video Outputs OFF	
RFmod Outputs	1	0	X	X	X	X	X	X	X	Audio & Video Outputs ON	
		1	X	X	X	X	X	X	X	Audio & Video Outputs OFF	
Full Stop		1	1	1	1	1	1	1	1	Only I ² C bus and slow blanking detection parts are supplied.	

Table 21. Output Signals (Read Mode)

Reg. Addr (Hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
	Slow Blanking TV SCART	2	X	X	X	X	X	X	0	1	Input <2 V
			X	X	X	X	X	X	1	0	Input 16/9 format
			X	X	X	X	X	X	1	1	Input 4/3 format
	Slow Blanking VCR SCART	2	X	X	X	X	0	1	X	X	Input <2 V
			X	X	X	X	1	0	X	X	Input 16/9 format
			X	X	X	X	1	1	X	X	Input 4/3 format
	Interrupt Flag	1	X	X	X	0	X	X	X	X	No change since read One change has been detected (refer to Note 5)

Note 5: The Interrupt Flag will be cleared when this register is read. To prepare for a new interrupt, a "1" must be re-written in the IT Enable bit (Reg. 04, d7).

3.2 Power-on Reset — Bus Register Initial Conditions

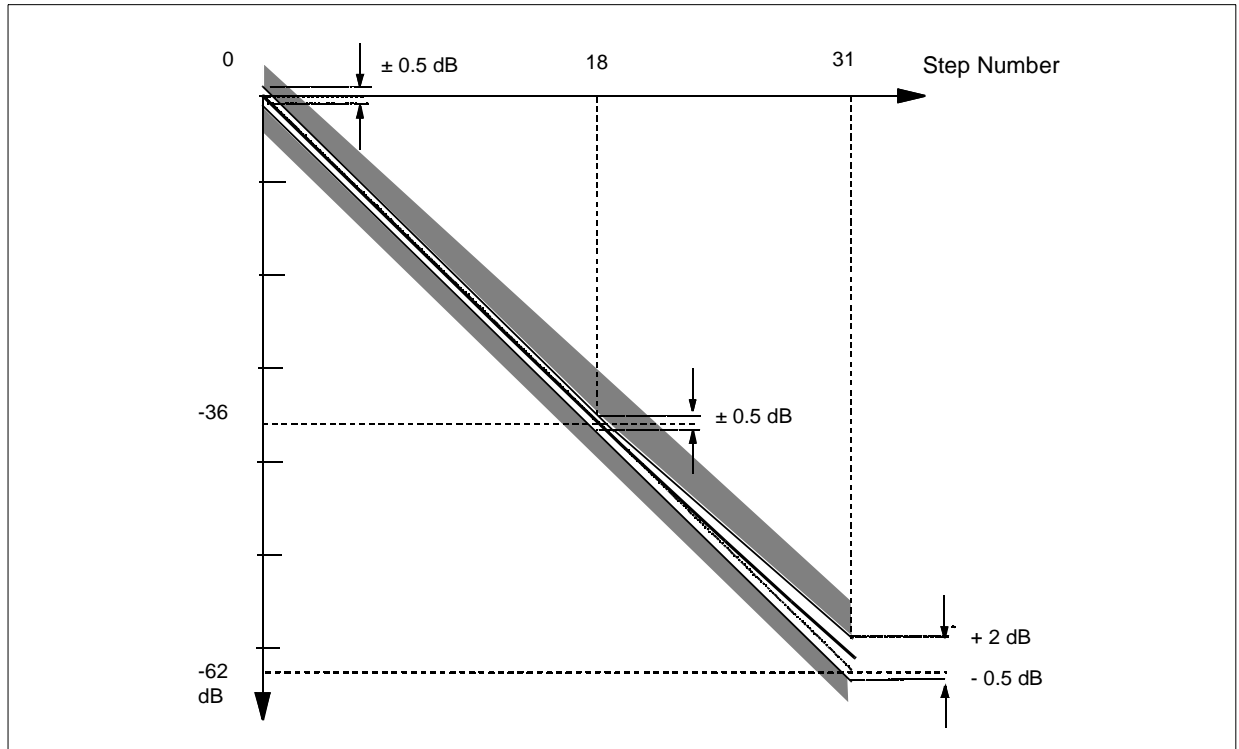
Power-on Reset is active when the supply V_{DD} is less than 3.5 volts.

Non-significant bits (X) are pre-set to "0".

Reg. Addr (Hex)	Data								Comments
	d7	d6	d5	d4	d3	d2	d1	d0	
00	0	0	0	0	0	0	0	0	Audio TV and Cinch outputs are in Stereo Mode, 0 dB Gain Adjustment.
01	0	0	0	0	0	0	0	0	TV, Cinch and VCR audio outputs are muted. VCR output is in Stereo Mode.
02	0	0	0	0	0	0	0	0	VCR, TV and RFmod video outputs are muted.
03	0	0	0	0	0	0	0	0	Fast Blanking is forced to '0'. RGB outputs are muted and in high impedance.
04	0	0	0	0	0	0	0	0	C_GATE is high. C_VCR is high impedance.

Reg. Addr (Hex)	Data								Comments
	d7	d6	d5	d4	d3	d2	d1	d0	
05	0	0	0	0	0	0	0	0	Encoder and VCR R/Csub Bottom Level Clamp, RGB outputs 6 dB Gain, and Slow Blanking parts are in read mode.
06	0	0	0	0	0	0	0	0	All internal blocks are ON.

Figure 6. Volume Control Characteristics



4 INPUT/OUTPUT GROUPS

Figure 7. Bottom Clamped Video Inputs (Pins 2, 4, 6, 12, 14, 18, 21, 62, 64)

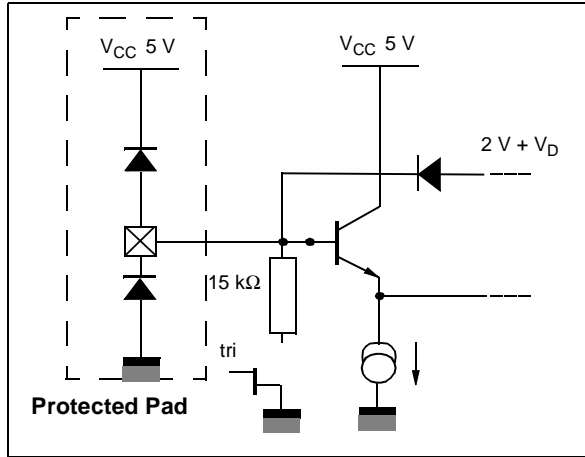


Figure 8. R/C Clamped Video Inputs (Pins 10, 60)

R/C inputs may be configured either as a bottom clamped input or as an average clamped input. In either case, the simplified input schematic is very close to one of the graphics shown above.

Figure 9. Fast Blanking Inputs (Pins 50, 51)

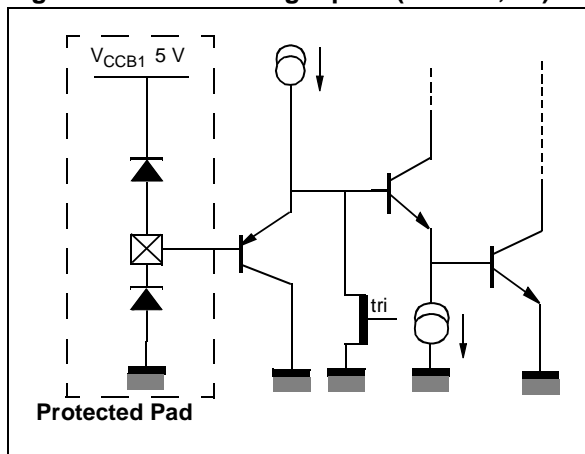


Figure 10. Average Clamped Video Inputs (Pin8)

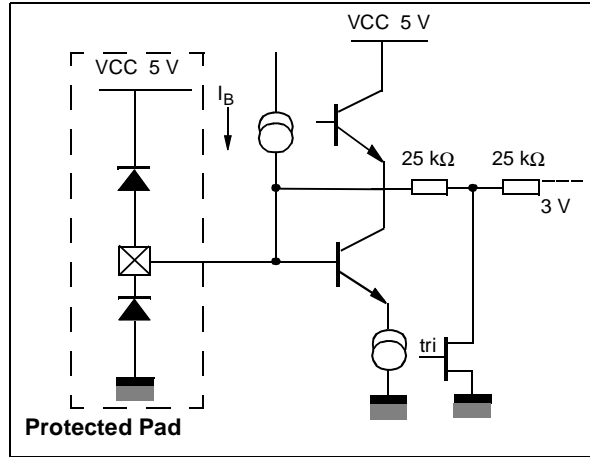


Figure 11. Cgate Logical Output (Pin 52)

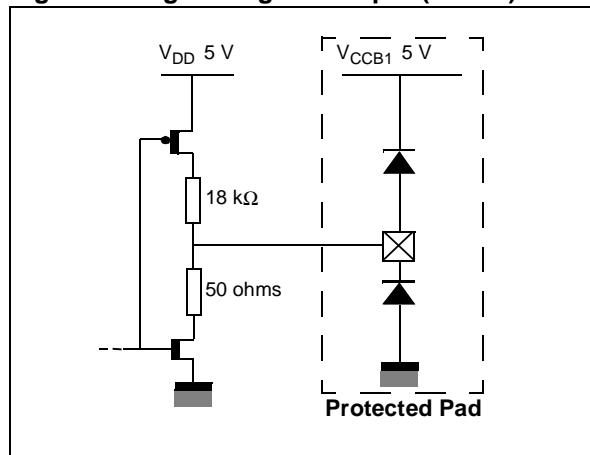


Figure 12. Fast Blanking Output (Pin 49)

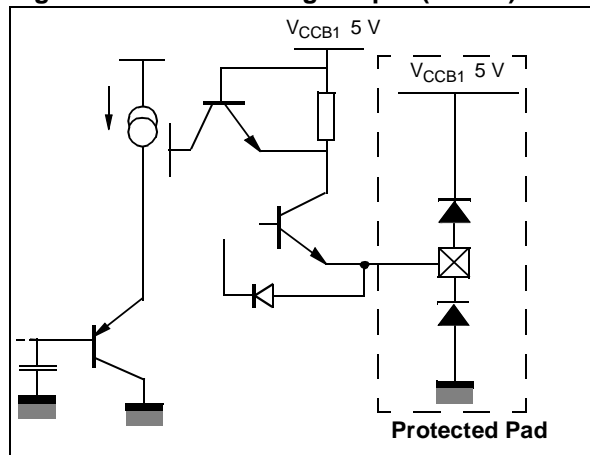


Figure 13. Video Outputs (Pins 38, 40, 42, 44, 46, 48)

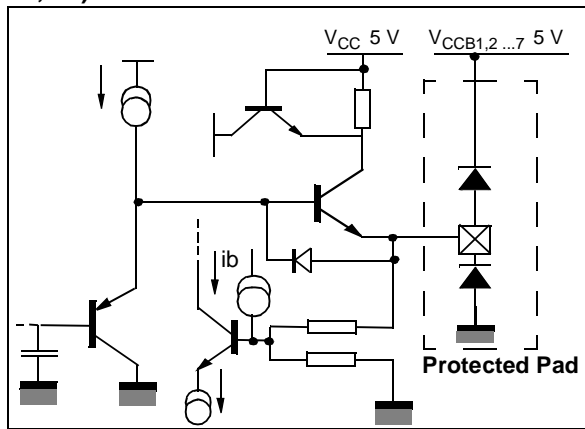


Figure 16. Trap Filter (Pin 34)

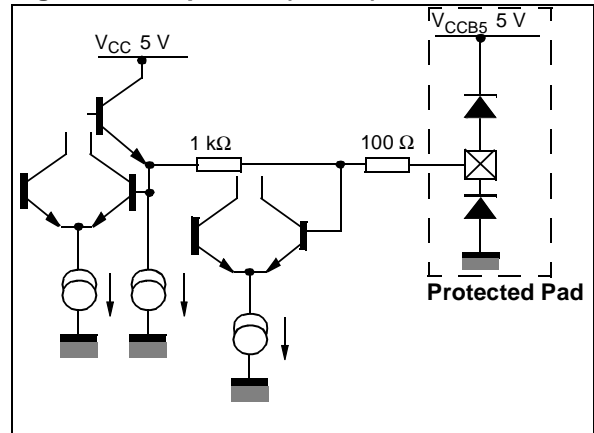


Figure 14. Audio Inputs (Pins 7, 9 11, 13, 19, 20, 22, 23)

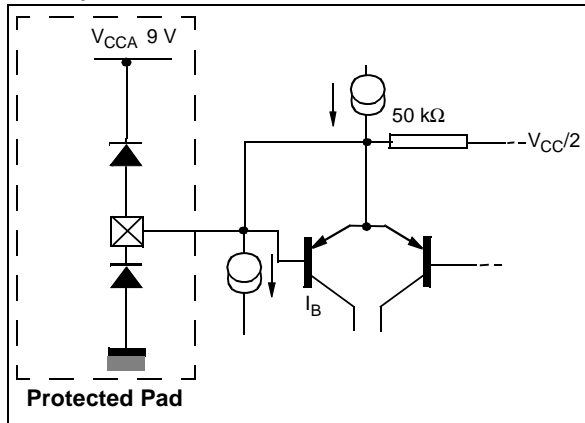


Figure 17. Audio Outputs (Pins 27, 28, 29, 30, 32, 33,35)

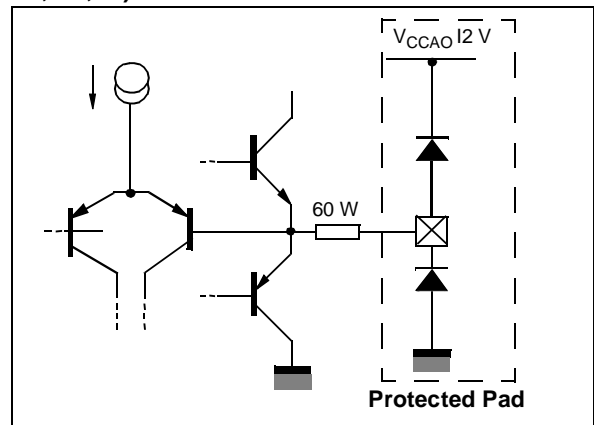


Figure 15. Slow Blanking I/O (Pins 59, 61)

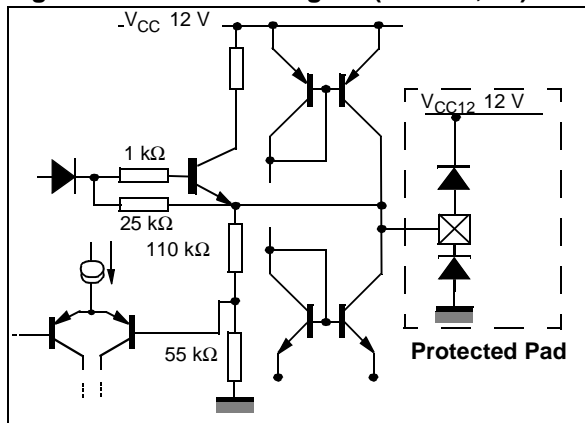


Figure 18. Interrupt Output (Pin 58)

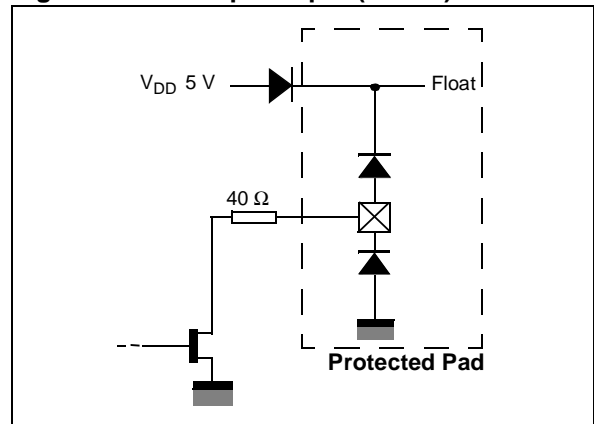


Figure 19. I²C Bus (SDA) (Pin 56)

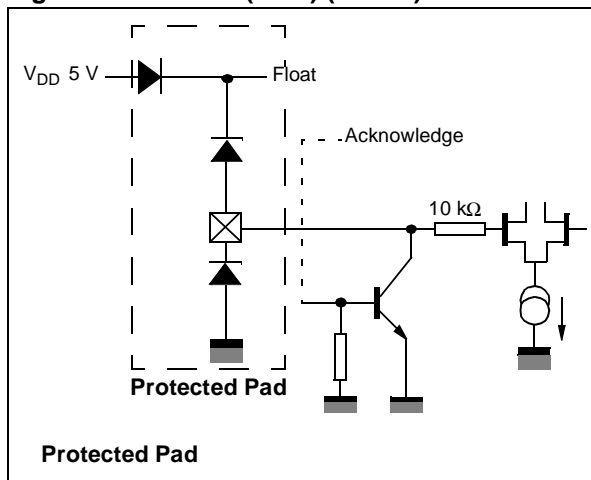


Figure 21. I²C Bus (SCL) (Pin 55)

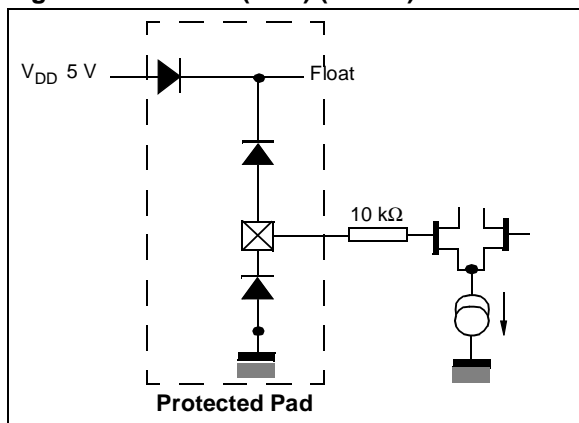


Figure 20. I²C Bus (ADD) (Pin 54)

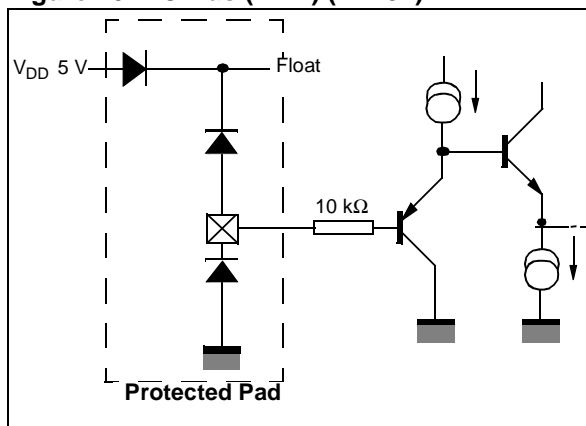
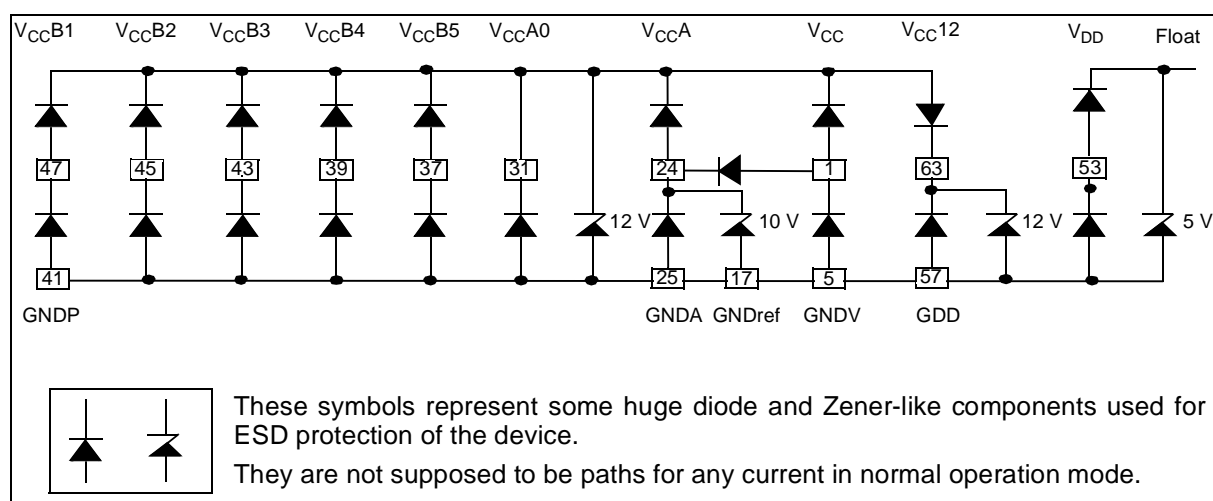
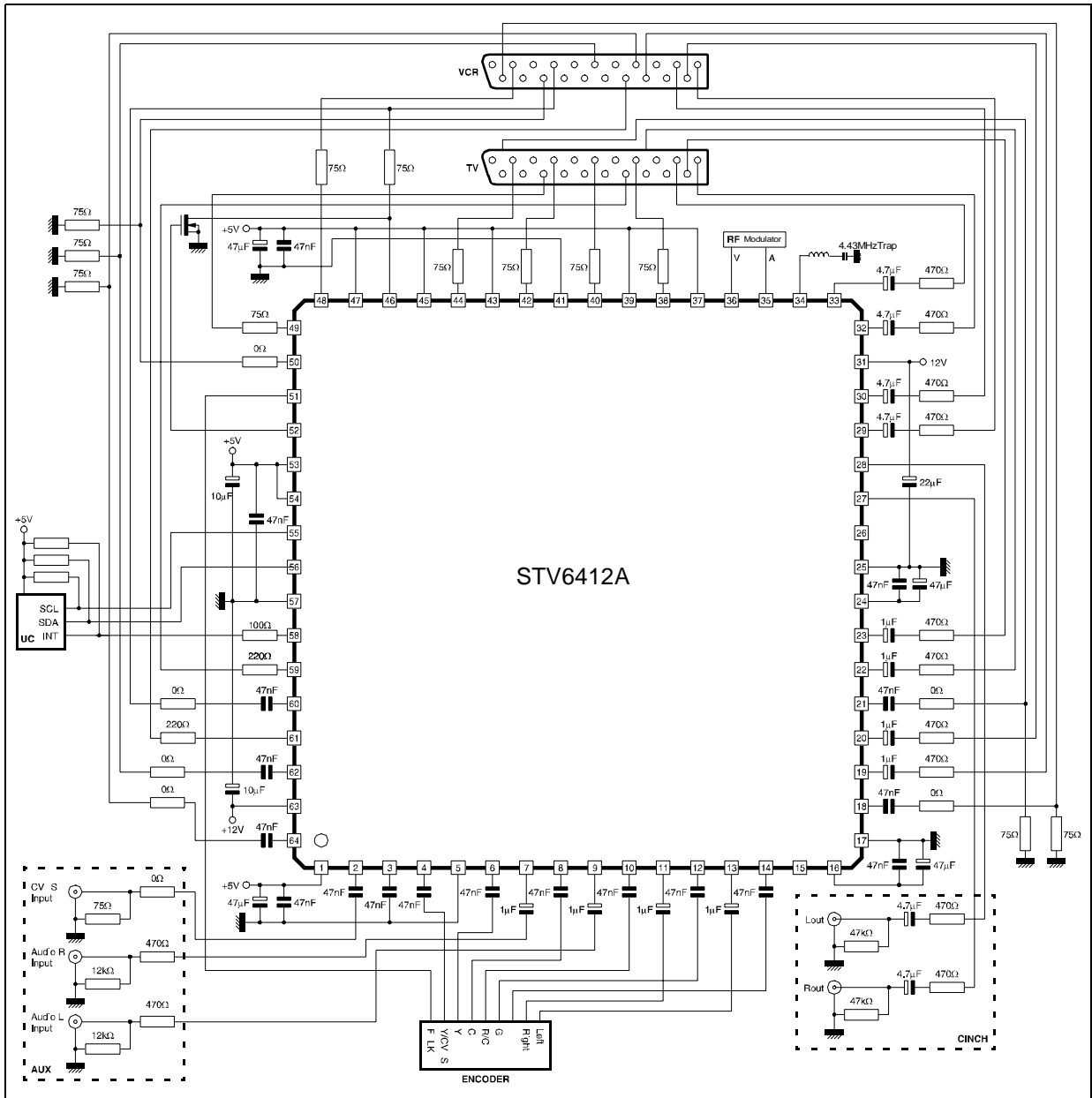


Figure 22. Power Supply Connection



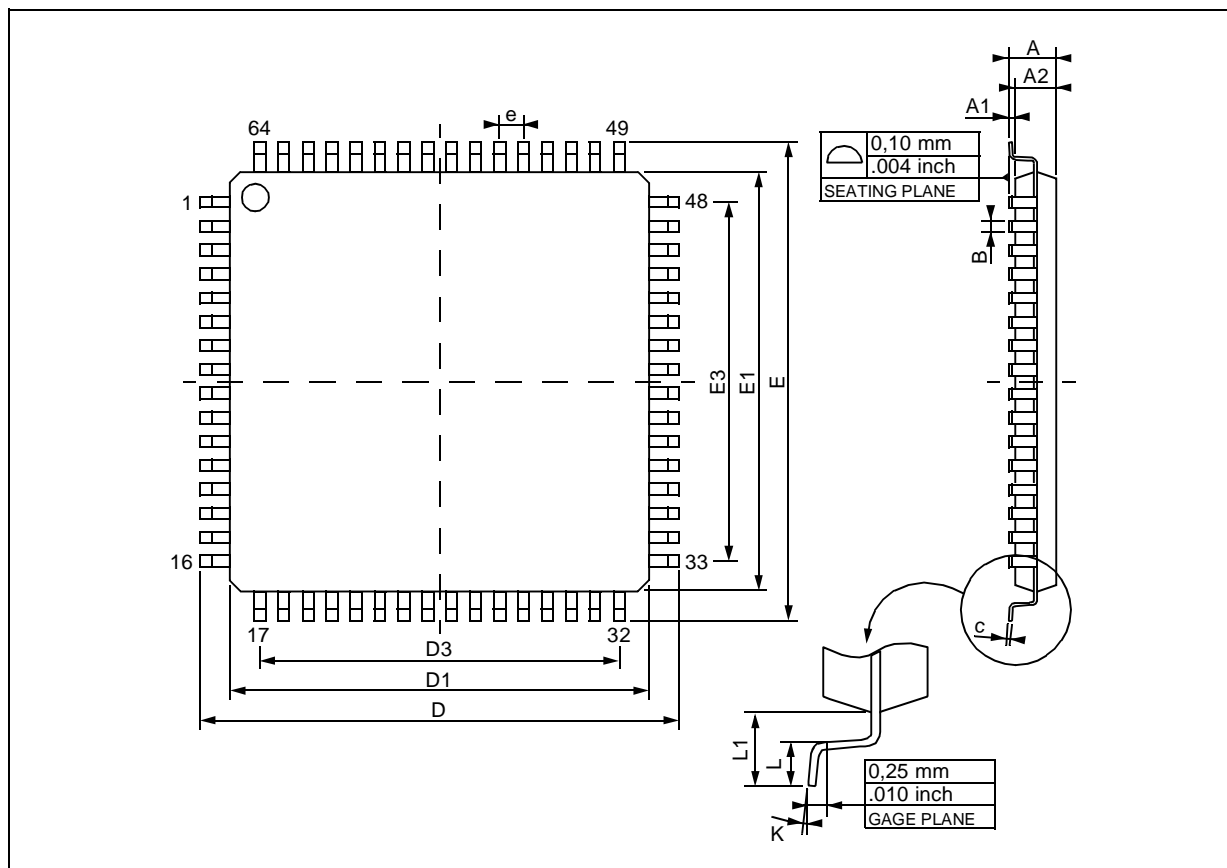
5 APPLICATION DIAGRAM



For more details refer to STV6412 Application Note.

6 PACKAGE MECHANICAL DATA

Figure 23. 64 Pins — Thin Full Plastic Quad Flat Pack (TQFP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.0118	0.0146	0.0177
C	0.09		0.20	0.0035		0.0079
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.80			0.0315	
E		16.00			0.630	
E1		14.00	1		0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (Min.), 7° (Max.)					

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without the express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

©2003 STMicroelectronics - All Rights Reserved.

Purchase of I²C Components by STMicroelectronics conveys a license under the Philips I²C Patent. Rights to use these components in an I²C system is granted provided that the system conforms to the I²C Standard Specification as defined by Philips.

STMicroelectronics Group of Companies

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>