TMP61 Small Silicon-Based Linear Thermistor for Temperature Sensing

1 Features

- Silicon-based thermistor with a Positive Temperature Coefficient (PTC)
- Linear resistance change with temperature
  - Simplifies resistance-to-temperature conversion
  - Decrease accuracy spread compared to non-linear Negative Temperature Coefficient (NTC) thermistor-based circuits across a wide temperature range
- 10-kΩ nominal resistance at 25°C (R25)
  - ±1% maximum (0°C to 70°C)
- Consistent sensitivity across temperature
  - 6400 ppm/°C TCR (25°C)
  - 0.2% typical TCR tolerance across temperature (–40°C to 125°C)
- Wide operating temperature:
  - –65°C to +150°C
- Fast thermal response time:
  - 0.6 second for DEC package
- Long lifetime and robust performance
  - Ultra low power consumption compared to traditional NTCs that lower errors due to self heating
  - Built-in fail-safe in case of short-circuit failures
  - <1% maximum drift after high temperature and high humidity stress tests
- Available package options:
  - X1SON (DEC/0402 footprint)
  - TO-92S (LPG)
  - SOT-5X3 (DYA) (contact representative for availability)

2 Applications

- Temperature Measurement and Monitoring
- Thermal Compensation
- Thermal Protection (With Comparator)

3 Description

The TMP61 series of small silicon linear thermistors are designed for temperature measurement, protection, compensation, and control systems. Compared to traditional NTC thermistors, the TMP61 device offers enhanced linearity and consistent sensitivity across the full temperature range. The TMP61 offers robust performance due to device immunity to environmental variation and built-in fail-safe behaviors at high temperatures. This device is currently available in a 2-pin, surface-mount, 0402 footprint-compatible X1SON package and a 2-pin, through-hole, mini-sized transistor-outline TO-92S package, and a low profile 2-pin SOT-5X3 package.

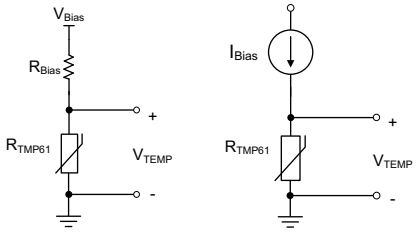
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP61	X1SON (2)	0.60 mm × 1.00 mm
	TO-92S (2)	4.00 mm × 3.15 mm
	SOT-5X3 (2)(2)	0.80 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) This package is in preview

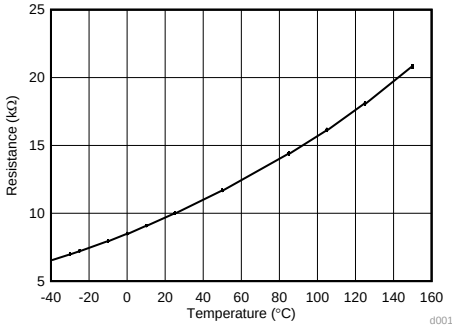
Typical Implementation Circuits



$V_{Temp} = V_{Bias} \times \frac{R_{TMP61}}{R_{Bias} + R_{TMP61}}$

$V_{Temp} = I_{Bias} \times R_{TMP61}$

Typical Resistances vs Ambient Temperature



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2019) to Revision C — **Page**

- Added preview SOT-5X3 package ... 1

Changes from Revision A (June 2019) to Revision B — **Page**

- Changed *Application* bullets ... 1
- Increased ESD CDM Rating ... 4
- Added Thermal Information for LPG Package ... 4
- Added 'Long Term Drift' spec for LPG package ... 5
- Changed polynomial equation ... 8
- Added equations for both DEC package and LPG packages ... 8
- Added transfer tables for the LPG package ... 9
- Changed *Layout Example* section ... 22

Changes from Original (December 2018) to Revision A — **Page**

- Changed data sheet status from Production Mixed to Production Data ... 1

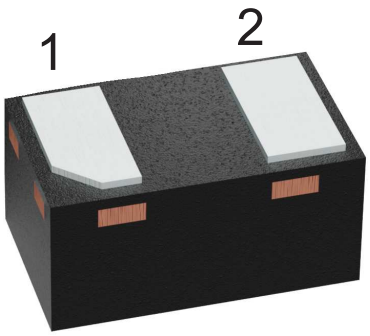
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5 Device Comparison Table

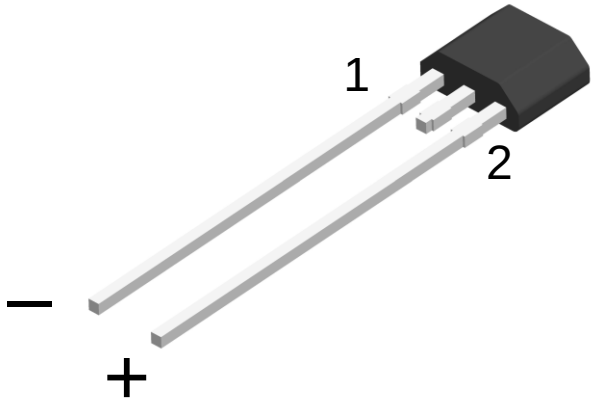
PART NUMBER	RATING	R25 TYP	R25 %TOL	PACKAGE	T_A
TMP61DEC	Catalog	10k	1%	X1SON / DEC (0402)	–40°C to 150°C
TMP61LPG				TO92S / LPG	–40°C to 150°C
TMP61DYA				SOT-5X3 / DYA	–40°C to 125°C

6 Pin Configuration and Functions

DEC Package
2-Pin X1SON
Top View (Angled)



LPG Package
2-Pin TO-92S
Top View (Angled)



DYA Package
2-Pin SOT-5X3
Bottom View (Angled)



(1) This package is in preview

Pin Functions

PIN				TYPE	DESCRIPTION
NAME	X1SON (DEC)	TO-92S (LPG)	SOT-5X3 (DYA)		
–	1	1	1	—	Thermistor (–) and (+) terminals. For proper operation, ensure a positive bias where the + terminal is at a higher voltage potential than the – terminal.
+	2	2	2		

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage across the device		6	V
Junction temperature (T_J)	-40	150	°C
Current through the device		450	µA
Storage temperature (T_{stg})	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) per JESD22-A114 (1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{Sns}	Voltage Across Pins 2 (+) and 1 (–)	0		5.5	V
I_{Sns}	Current passing through the device	0		400	µA
T_A	Operating free-air temperature (specified performance) (X1SON/DEC Package)	–40		125	°C
T_A	Operating free-air temperature (specified performance) (TO-92S/LPG Package)	–40		150	°C
T_A	Operating free-air temperature (specified performance) (SOT-5X3/DYA Package)	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)(2)		TMP61			UNIT
		DEC (X1SON)	LPG (TO-92)	DYA (SOT-5X3)	
		2 PINS	2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (3)(4)	443.4	215	742.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	195.7	99.9	315.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	254.6	191.7	506.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	35.1	109.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	254.5	191.7	500.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) For information on self-heating and thermal response time see Layout Guidelines section.
(3) The junction to ambient thermal resistance ($R\theta_{JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(4) Changes in output due to self heating can be computed by multiplying the internal dissipation by the thermal resistance.

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7.5 Electrical Characteristics

T_A = -40°C to 125°C, I_{Sns} = 200 µA (unless otherwise noted)

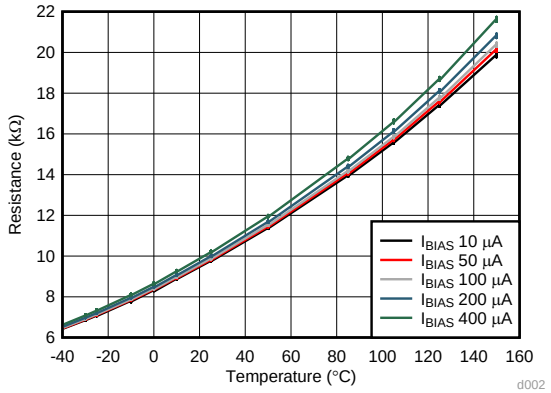
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{25}	Thermistor Resistance at 25°C (1)	T_A = 25°C	9.9	10	10.1	kΩ
R_{TOL}	Resistance Tolerance (1)	T_A = 25°C	–1		+1	%
		T_A = 0°C to 70°C	–1		+1	
		T_A = -40°C to 125°C	–1.5		+1.5	
TCR_{-35}	Temperature Coefficient of Resistance	T1 = -40°C, T2 = -30°C		+6220		ppm/°C
TCR_{25}		T1 = 20°C, T2 = 30°C		+6400		
TCR_{85}		T1 = 80°C, T2 = 90°C		+5910		
TCR_{-35} %	Temperature Coefficient of Resistance Tolerance	T1 = -40°C, T2 = -30°C		±0.4		%
TCR_{25} %		T1 = 20°C, T2 = 30°C		±0.2		
TCR_{85} %		T1 = 80°C, T2 = 90°C		±0.3		
ΔR	Sensor Long Term Drift (Reliability)	96 hours continuous operation RH=85%, T_A = 130°C, V_{Bias} = 5.5V	0.1		0.8	%
	Sensor Long Term Drift (Reliability)	600 hours continuous operation T_A = 150°C, V_{Bias} = 5.5V, DEC Package	0.1		1	
	Sensor Long Term Drift (Reliability)	1000 hours continuous operation T_A = 150°C, V_{Bias} = 5.5V, LPG Package	0.1		1.1	%
$t_{RES\ (stirred\ liquid)}$	Thermal response to 63%	T1=25°C in Still Air to T2=125°C in Stirred Liquid		0.6		s
$t_{RES\ (still\ air)}$	Thermal response to 63%	T1=25°C to T2=70°C in Still Air		3.2		s

(1) Limits defined based on 4th order equation

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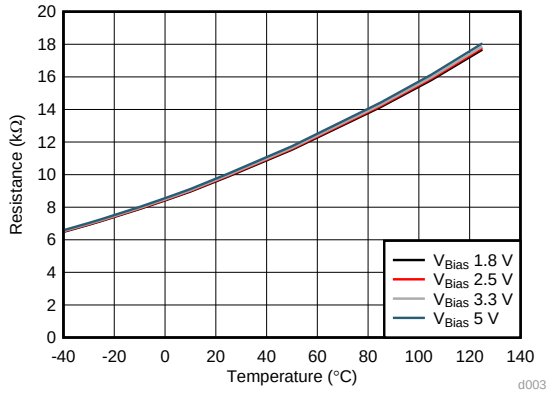
7.6 Typical Characteristics

at T_A = 25°C, (unless otherwise noted)



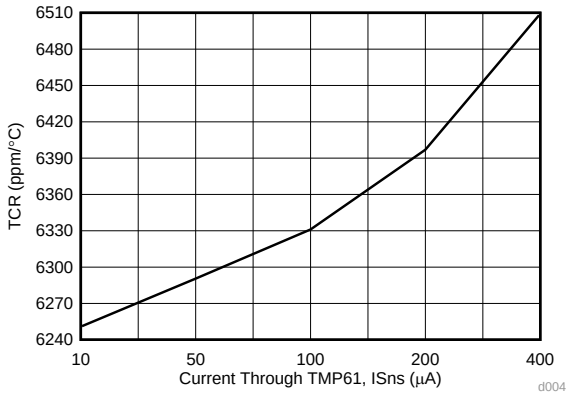
TMP61: I_{Bias} = 10, 100, 200, and 400 µA

Figure 1. Resistance vs. Ambient Temperature Using Multiple Bias Currents



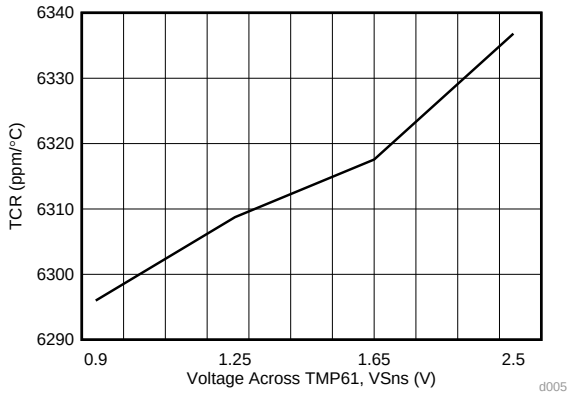
TMP61: V_{Bias} = 1.8, 2.5, 3.3, and 5.0 V, R_{Bias} = 10 kΩ with ±0.01% Tolerance

Figure 2. Resistance vs. Ambient Temperature Using Multiple Bias Voltages



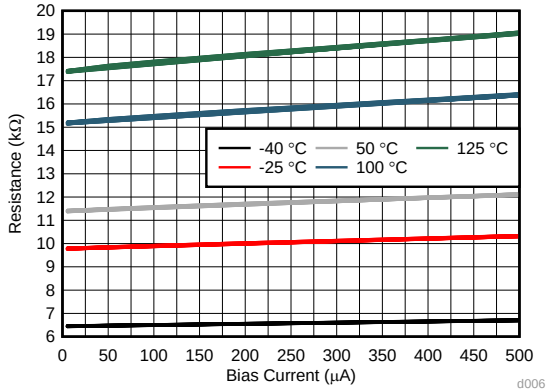
TMP61: I_{Sns} = 10, 100, 200, and 400 µA

Figure 3. TCR as a Function of Sense Currents I_{Sns}



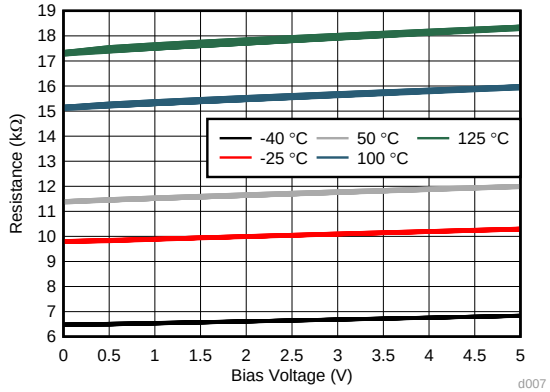
TMP61: V_{Sns} = 1.8, 2.5, 3.3, and 5.0 V, R_{Bias} = 10 kΩ with ±0.01% Tolerance

Figure 4. TCR as a Function of Sense Voltages, V_{Sns}



TMP61: T_A = –40°C, 25°C, 50°C, 100°C, and 125°C

Figure 5. Supply Dependence R vs. I_{Bias}



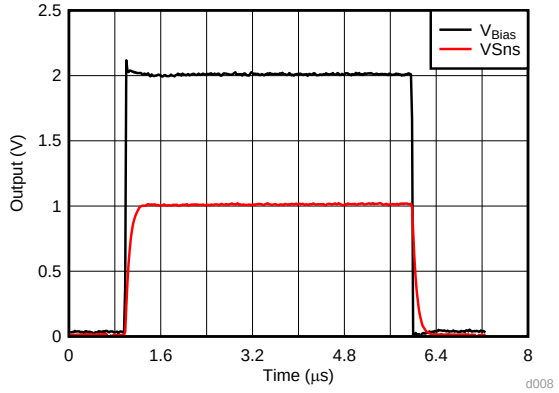
TMP61: T_A = –40°C, 25°C, 50°C, 100°C, and 125°C, R_{Bias} = 10 kΩ with ±0.01% Tolerance

Figure 6. Supply Dependence R vs. V_{Bias}

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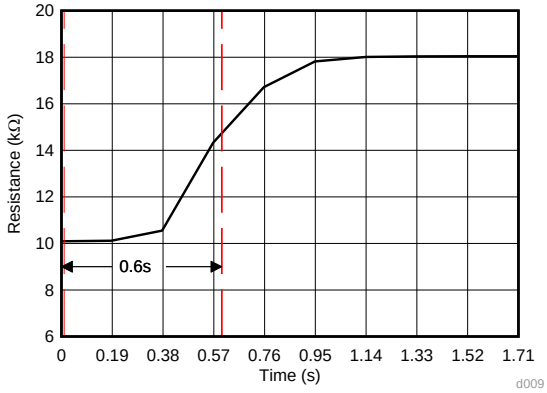
Typical Characteristics (continued)

at T_A = 25°C, (unless otherwise noted)



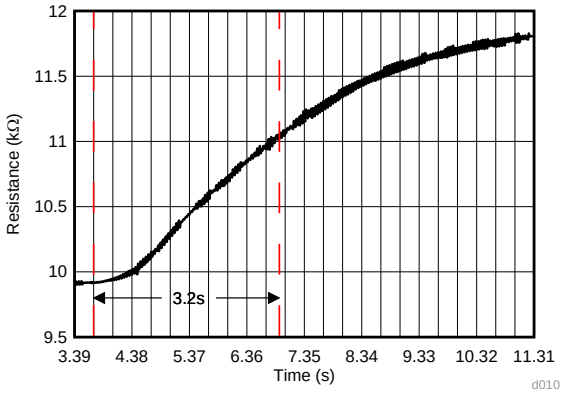
TMP61: V_{SNS} = 1 V

Figure 7. Step Response



TMP61: Stirred Liquid

Figure 8. Thermal Response Time



TMP61: Still Air

Figure 9. Thermal Response Time

8 Detailed Description

8.1 Overview

The TMP61 series of silicon linear thermistors has a linear positive temperature coefficient (PTC) that results in a uniform and consistent temperature coefficient resistance (TCR) across a wide operating temperature range.

8.2 Functional Block Diagram

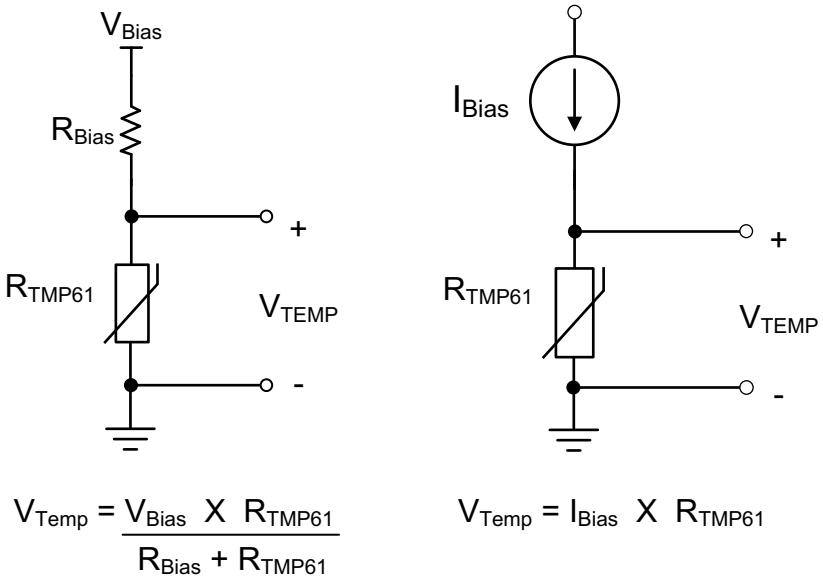


Figure 10. Typical Implementation Circuits

8.3 Feature Description

As shown in Figure 1 and Figure 2, the TMP61 has good linear behaviour across the whole temperature range, but a small non-linearity can be observed, as well as supply dependence, as shown in Figure 3 and Figure 4. To fabricate the TMP61, the engineer can use a special silicon process where the device key characteristics—the temperature coefficient resistance (TCR) and nominal resistance (R25)—are controlled by the doping level and active region area. Note that the TMP61 has an active area and a substrate due to the polarized terminals of the device. The positive terminal should be connected to the highest potential, while the negative terminal (which is tied to the substrate internally) should be connected to the lowest potential. and Equation 1 can help the user approximate the device resistance and TCR. Table 1, Table 2, Table 4, and Table 5 show the typical resistance, resistance spread, and maximum expected error across temperature using a direct ideal bias current or an ideal voltage bias in a divider circuit.

DEC Package: $R\ (\Omega) \approx 8490.69 + 55.24\ T + 0.1541\ T^2 - 1.224E\text{-}4\ T^3 + 1.465E\text{-}6\ T^4$

LPG Package: $R\ (\Omega) \approx 8535.76 + 54.79454\ T + 0.14982\ T^2 - 2.06739E\text{-}5\ T^3 + 9.94E\text{-}7\ T^4$

DYA Package: $R\ (\Omega) \approx 8485.75 + 53.65\ T + 0.145\ T^2 + 1.18E\text{-}4\ T^3 + 5.71E\text{-}8\ T^4$

where

- T is the temperature of interest

$$TCR\ (ppm/°C) = (R_{T2} - R_{T1}) / ((T_2 - T_1) \times R_{(T2+T1)/2}) \quad (1)$$

Below are the definitions of the key terms used throughout this document:

- I_{Sns}: Current flowing through the TMP61.
- V_{Sns}: Voltage across the two TMP61 terminals.
- I_{Bias}: Current supplied by the biasing circuit.
- V_{Bias}: Voltage supplied by the biasing circuit.
- V_{Temp}: Output voltage that corresponds to the measured temperature. Note that this is different from V_{Sns}. In a

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Feature Description (continued)

case of a voltage divider circuit with the TMP61 in the high side, V_{Temp} is taken across R_{Bias}.

Table 1. TMP61 Transfer Table Using an Ideal I_{Bias} of 200 µA [DEC Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(1)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(2)(1) (°C)
	MIN	TYP	MAX		
–40	6445	6543	6641	42	2.32
–35	6657	6759	6860	44	2.30
–30	6879	6983	7088	46	2.29
–25	7109	7217	7325	48	2.28
–20	7347	7459	7571	49	2.27
–15	7594	7710	7825	51	2.27
–10	7849	7968	8088	53	2.27
–5	8112	8235	8359	54	2.28
0	8425	8510	8595	56	1.53
5	8704	8792	8880	57	1.53
10	8992	9083	9173	59	1.54
15	9287	9381	9475	60	1.55
20	9590	9687	9783	62	1.56
25	9900	10000	10100	63	1.58
30	10218	10321	10424	65	1.59
35	10544	10650	10757	67	1.60
40	10877	10987	11097	68	1.61
45	11218	11332	11445	70	1.62
50	11568	11685	11801	71	1.64
55	11925	12045	12166	73	1.65
60	12291	12415	12539	75	1.66
65	12665	12792	12920	76	1.67
70	13047	13179	13311	78	1.69
75	13371	13574	13778	80	2.55
80	13769	13979	14188	82	2.56
85	14177	14393	14608	84	2.58
90	14594	14816	15038	86	2.59
95	15021	15250	15479	88	2.61
100	15458	15694	15929	90	2.62
105	15906	16148	16391	92	2.63
110	16365	16614	16863	94	2.64
115	16835	17091	17348	97	2.65
120	17317	17581	17844	99	2.66
125	17811	18082	18353	102	2.67

(1) Table defined based on 4th order equation:
(2) Assuming ideal current source

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Table 2. TMP61 Transfer Table Using an Ideal I_{Bias} of 200 µA [LPG Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(1)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(2)(1) (°C)
	MIN	TYP	MAX		
–40	6486	6585	6684	43	2.32
–35	6700	6802	6904	44	2.31
–30	6922	7027	7132	46	2.30
–25	7151	7260	7368	47	2.30
–20	7387	7500	7612	49	2.31
–15	7631	7748	7864	50	2.31
–10	7883	8003	8123	52	2.32
–5	8142	8266	8390	53	2.33
0	8450	8536	8621	55	1.56
5	8725	8813	8902	56	1.57
10	9008	9099	9190	58	1.57
15	9298	9392	9485	59	1.58
20	9595	9692	9789	61	1.59
25	9900	10000	10100	62	1.60
30	10213	10316	10419	64	1.61
35	10533	10639	10746	66	1.62
40	10861	10971	11081	67	1.63
45	11198	11311	11424	69	1.64
50	11542	11659	11775	70	1.66
55	11895	12015	12135	72	1.67
60	12256	12380	12504	74	1.68
65	12626	12754	12881	76	1.69
70	13005	13136	13268	77	1.70
75	13325	13528	13731	79	2.56
80	13721	13929	14138	81	2.57
85	14125	14340	14555	83	2.59
90	14540	14761	14983	85	2.60
95	14964	15192	15420	87	2.61
100	15399	15633	15868	89	2.62
105	15844	16086	16327	92	2.64
110	16301	16549	16797	94	2.65
115	16768	17024	17279	96	2.66
120	17248	17510	17773	99	2.67
125	17739	18009	18279	101	2.68

(1) Table defined based on 4th order equation:
(2) Assuming ideal current source

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Table 3. TMP61 Transfer Table Using an Ideal I_{Bias} of 200 µA [DYA Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(1)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(2)(1) (°C)
	MIN	TYP	MAX		
–40	6497	6596	6695	42	2.36
–35	6707	6809	6911	44	2.35
–30	6926	7031	7136	45	2.33
–25	7152	7261	7370	47	2.33
–20	7387	7499	7612	48	2.32
–15	7629	7746	7862	50	2.32
–10	7880	8000	8120	52	2.32
–5	8138	8262	8386	53	2.33
0	8447	8532	8618	55	1.56
5	8722	8810	8898	56	1.56
10	9005	9096	9187	58	1.57
15	9296	9390	9484	60	1.58
20	9594	9691	9788	61	1.59
25	9900	10000	10100	63	1.60
30	10214	10318	10421	64	1.61
35	10536	10643	10749	66	1.62
40	10866	10976	11086	67	1.63
45	11204	11317	11430	69	1.64
50	11549	11666	11783	71	1.65
55	11903	12024	12144	72	1.66
60	12265	12389	12513	74	1.67
65	12636	12763	12891	76	1.69
70	13015	13146	13278	77	1.70
75	13335	13538	13741	79	2.56
80	13729	13938	14147	81	2.58
85	14132	14347	14563	83	2.60
90	14545	14766	14988	85	2.62
95	14966	15194	15422	87	2.63
100	15397	15632	15866	89	2.65
105	15838	16079	16320	90	2.67
110	16289	16537	16785	93	2.68
115	16749	17004	17260	95	2.70
120	17221	17483	17745	97	2.71
125	17703	17972	18242	99	2.72

(1) Table defined based on 4th order equation:
(2) Assuming ideal current source

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Table 4. TMP61 Transfer Table Using a Voltage Divider With an Ideal V_{Bias} of 2.5 V and R_{Bias} of 10 kΩ With ±0.01% Tolerance [DEC Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(1)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(2) (°C)
	MIN	TYP	MAX		
–40	6411	6508	6606	41	2.39
–35	6617	6717	6818	43	2.35
–30	6833	6937	7041	45	2.32
–25	7058	7165	7273	47	2.30
–20	7293	7404	7515	49	2.29
–15	7536	7651	7765	50	2.28
–10	7788	7906	8025	52	2.28
–5	8048	8170	8293	54	2.29
0	8358	8442	8527	55	1.53
5	8635	8722	8809	57	1.54
10	8920	9010	9100	58	1.55
15	9212	9305	9398	60	1.56
20	9511	9607	9703	61	1.57
25	9817	9916	10016	63	1.58
30	10131	10233	10335	64	1.60
35	10451	10557	10662	65	1.61
40	10779	10888	10997	67	1.63
45	11113	11226	11338	68	1.64
50	11455	11571	11687	70	1.66
55	11804	11923	12043	71	1.67
60	12161	12283	12406	73	1.69
65	12524	12651	12777	74	1.70
70	12896	13026	13156	76	1.72
75	13208	13409	13610	77	2.60
80	13593	13800	14007	79	2.62
85	13987	14200	14413	81	2.64
90	14390	14609	14828	83	2.65
95	14801	15026	15252	84	2.67
100	15222	15453	15685	86	2.68
105	15652	15890	16129	88	2.70
110	16093	16338	16583	91	2.71
115	16544	16796	17048	93	2.72
120	17006	17265	17524	95	2.73
125	17480	17746	18012	97	2.73

(1) Table defined based on 4th order equation:
(2) Assuming ideal voltage source, 10 kΩ with ±0.01% R_{Bias}

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Table 5. TMP61 Transfer Table Using a Voltage Divider With an Ideal V_{Bias} of 2.5 V and R_{Bias} of 10 kΩ With ±0.01% Tolerance [LPG Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(1)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(2) (°C)
	MIN	TYP	MAX		
–40	6460	6559	6657	42	2.32
–35	6673	6774	6876	44	2.32
–30	6892	6997	7102	45	2.32
–25	7119	7227	7336	47	2.32
–20	7353	7465	7576	48	2.33
–15	7593	7709	7824	50	2.33
–10	7841	7960	8079	51	2.34
–5	8095	8218	8342	52	2.35
0	8399	8484	8569	54	1.58
5	8669	8756	8844	55	1.59
10	8946	9036	9126	57	1.60
15	9230	9323	9416	58	1.61
20	9521	9617	9713	60	1.62
25	9819	9918	10017	61	1.63
30	10124	10227	10329	62	1.64
35	10437	10543	10648	64	1.65
40	10758	10866	10975	65	1.66
45	11086	11198	11310	67	1.67
50	11421	11536	11652	69	1.68
55	11764	11883	12002	70	1.69
60	12115	12238	12360	72	1.71
65	12475	12601	12727	73	1.72
70	12842	12972	13101	75	1.73
75	13151	13351	13551	77	2.61
80	13533	13739	13945	78	2.63
85	13923	14136	14348	80	2.64
90	14323	14541	14759	82	2.66
95	14731	14956	15180	84	2.68
100	15149	15380	15610	86	2.69
105	15576	15813	16050	88	2.71
110	16013	16256	16500	90	2.72
115	16459	16710	16960	92	2.73
120	16915	17173	17430	94	2.75
125	17382	17647	17911	96	2.76

(1) Table defined based on 4th order equation:
(2) Assuming ideal voltage source, 10 kΩ with ±0.01% R_{Bias}

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Table 6. TMP61 Transfer Table Using a Voltage Divider With an Ideal V_{Bias} of 2.5 V and R_{Bias} of 10 kΩ With ±0.01% Tolerance [DYA Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(1)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(2) (°C)
	MIN	TYP	MAX		
–40	6466	6564	6663	43	2.31
–35	6679	6781	6882	44	2.32
–30	6899	7004	7109	45	2.32
–25	7125	7233	7342	47	2.33
–20	7358	7470	7582	48	2.33
–15	7598	7713	7829	49	2.34
–10	7844	7964	8083	51	2.35
–5	8098	8221	8344	52	2.36
0	8401	8486	8571	54	1.58
5	8670	8758	8845	55	1.59
10	8946	9037	9127	57	1.60
15	9230	9324	9417	58	1.61
20	9522	9618	9714	60	1.61
25	9820	9919	10019	61	1.62
30	10127	10229	10331	63	1.63
35	10441	10546	10652	64	1.64
40	10763	10871	10980	66	1.65
45	11093	11205	11317	67	1.66
50	11430	11546	11661	69	1.67
55	11776	11895	12014	71	1.68
60	12130	12253	12376	72	1.69
65	12493	12619	12745	74	1.70
70	12864	12994	13124	76	1.72
75	13176	13377	13577	77	2.59
80	13562	13769	13975	79	2.61
85	13957	14169	14382	81	2.62
90	14360	14579	14797	83	2.64
95	14772	14997	15222	85	2.66
100	15193	15424	15656	86	2.68
105	15623	15861	16099	88	2.70
110	16063	16307	16552	90	2.71
115	16511	16763	17014	92	2.73
120	16969	17227	17486	94	2.75
125	17437	17702	17968	96	2.77

(1) Table defined based on 4th order equation:
(2) Assuming ideal voltage source, 10 kΩ with ±0.01% R_{Bias}

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMP61 is a positive temperature coefficient (PTC) linear silicon thermistor. The device behaves like a temperature-dependent resistor, and may be configured in a variety of ways to monitor temperature based on the system-level requirements. The TMP61 has a nominal resistance at 25°C (R25) of 10 kΩ with ±1% maximum tolerance, a maximum operating voltage of 5.5 V (V_{Sns}), and maximum supply current of 400 µA (I_{Sns}). This device may be used in a variety of applications to monitor temperature close to a heat source with the very small DEC package option compatible with the typical 0402 (inch) footprint. Some of the factors that influence the total measurement error include the ADC resolution (if applicable), the tolerance of the bias current or voltage, the tolerance of the bias resistance in the case of a voltage divider configuration, and the location of the sensor with respect to the heat source.

9.2 Typical Application

9.2.1 Thermistor Biasing Circuits

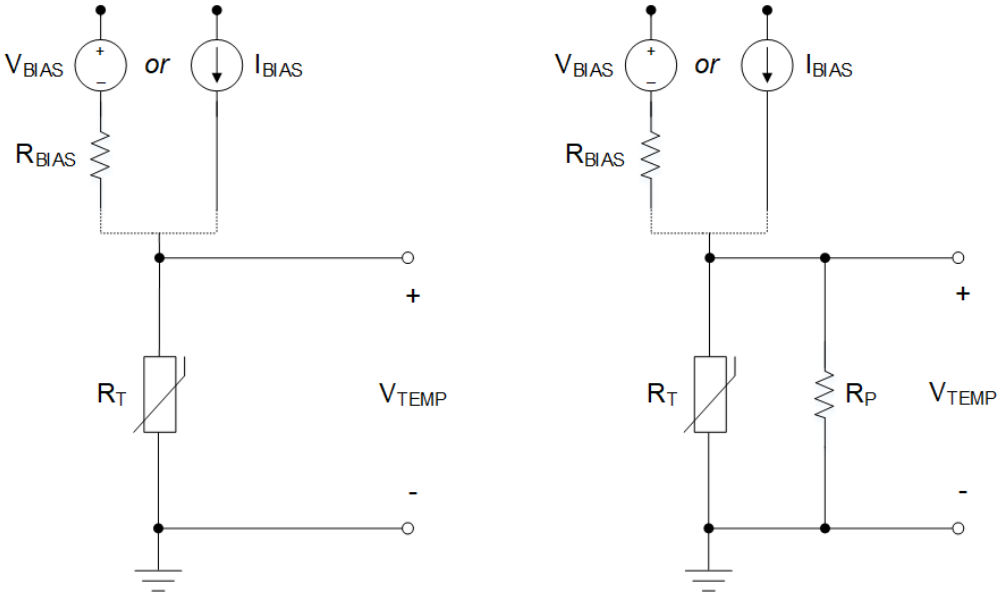


Figure 11. Biasing Circuit Implementations With Linear Thermistor (Left) vs. Non-Linear Thermistor (Right)

9.2.1.1 Design Requirements

Existing thermistors, in general, have a non-linear temperature vs. resistance curve. To linearize the thermistor response, the engineer can use a voltage linearization circuit with a voltage divider configuration, or a resistance linearization circuit by adding another resistance in parallel with the thermistor, R_P. Figure 11 highlights the two implementations, where R_T is the thermistor resistance. To generate an output voltage across the thermistor, the engineer can use either a voltage divider circuit with the thermistor placed at either the high side (close to supply) or low side (close to ground), depending on the desired voltage response (negative or positive). Additionally, the resistor can be biased directly using a precision current source (yielding the highest accuracy and voltage gain).

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Typical Application (continued)

It is common to use a voltage divider with thermistors because of its simple implementation and lower cost. The TMP61, on the other hand, has a linear positive temperature coefficient (PTC) of resistance such that the voltage measured across it increases linearly with temperature. As such, the need for linearization circuits is no longer a requirement, and a simple current source or a voltage divider circuit can be used to generate the temperature voltage.

This output voltage can be interpreted using a comparator against a voltage reference to trigger a temperature trip point that is either tied directly to an ADC to monitor temperature across a wider range or used as feedback input for an active feedback control circuit.

The voltage across the TMP61 can be translated to temperature using either a lookup table method (LUT) or a fitting polynomial, V(T), as described in Equation 2. The temperature voltage must first be digitized using an ADC. The necessary resolution of this ADC is dependent on the biasing method used. Additionally, for best accuracy, the bias voltage (V_{BIAS}) should be tied to the reference voltage of the ADC to create a measurement where the difference in tolerance between the bias voltage and the reference voltage cancels out. The engineer can also implement a low-pass filter to reject system level noise, and the user should place the filter as close to the ADC input as possible.

9.2.1.2 Detailed Design Procedure

The resistive circuit divider method produces an output voltage (V_{TEMP}) scaled according to the bias voltage (V_{BIAS}). When V_{BIAS} is also used as the reference voltage of the ADC, any fluctuations or tolerance error due to the voltage supply will be canceled and will not affect the temperature accuracy. This type of configuration is shown in Figure 12. Equation 2 describes the output voltage (V_{TEMP}) based on the variable resistance of the TMP61 (R_{TMP61}) and bias resistor (R_{BIAS}). The ADC code that corresponds to that output voltage, ADC full-scale range, and ADC resolution is given in Equation 3.

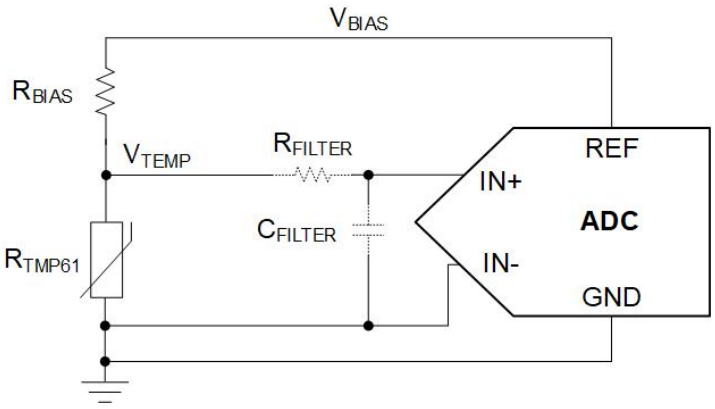


Figure 12. TMP61 Voltage Divider With an ADC

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}} \right) \quad (2)$$

$$ADC\ Code = \frac{V_{TEMP}}{FSR} 2^n \quad (3)$$

where

- FSR is the full-scale range of the ADC, which is the voltage at REF to GND (V_{REF})
- n is the resolution of the ADC

Equation 4 shows whenever $V_{REF} = V_{BIAS}$, V_{BIAS} cancels out.

$$ADC\ Code = \frac{V_{BIAS} \times \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}} \right)}{V_{BIAS}} 2^n = \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}} \right) 2^n \quad (4)$$

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Typical Application (continued)

The engineer can use a polynomial equation or a LUT to extract the temperature reading based on the ADC code read in the microcontroller.

The cancellation of V_{BIAS} is one benefit to using a voltage-divider (ratiometric approach), but the sensitivity of the output voltage of the divider circuit cannot increase much. Therefore, not all of the ADC codes will be used due to the small voltage output range compared to the FSR. This application is very common, however, and is simple to implement.

The engineer can use a current source-based circuit, like the one shown in Figure 13, to have better control over the sensitivity of the output voltage and achieve higher accuracy. In this case, the output voltage is simply V = I × R. For example, if a current source of 400 µA is used with the TMP61, the output voltage will span approximately 5.5 V and will have a gain up to 40 mV/°C. Having control over the voltage range and sensitivity allows for full utilization of the ADC codes and full-scale range. Based on the bias current, the temperature voltage is shown in Figure 14. Similar to the ratiometric approach above, if the ADC has a built-in current source that shares the same bias as the reference voltage of the ADC, the tolerance of the supply current cancels out. In this case, a precision ADC is not required. This method yields the best accuracy, but can increase the system implementation cost.

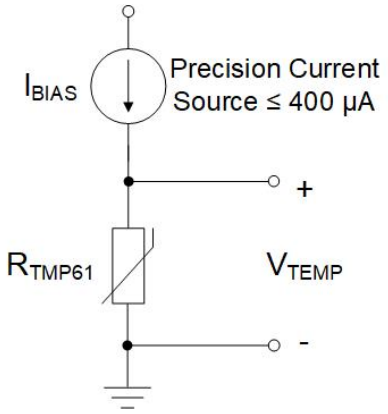


Figure 13. TMP61 Biasing Circuit With Current Source

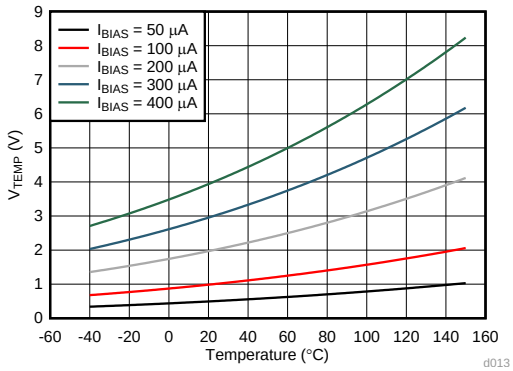


Figure 14. TMP61 Temperature Voltage With Varying Current Sources

In comparison to the non-linear NTC thermistor in a voltage divider, the TMP61 has an enhanced linear output characteristic. The two voltage divider circuits with and without a linearization parallel resistor, R_P, is shown in Figure 15. For example, consider an example where V_{BIAS} = 5 V, R_{BIAS} = 10 kΩ, and a parallel resistor (R_P) is used with the NTC thermistor (R_{NTC}) to linearize the output voltage with an additional 10-kΩ resistor. The output characteristics of the voltage dividers are shown in Figure 16. The TMP61 produces a linear curve across the entire temperature range while the NTC curve is only linear across a small temperature region. When the parallel resistor (R_P) is added to the NTC circuit, the added resistor makes the curve much more linear, but greatly affects the output voltage range.

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Typical Application (continued)

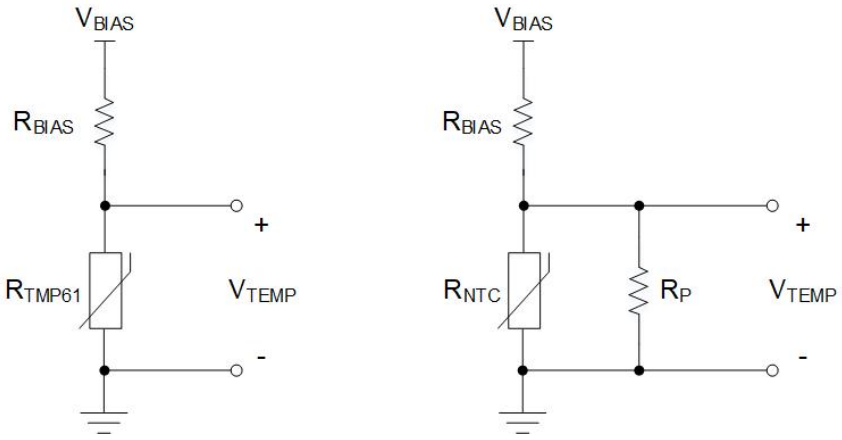


Figure 15. TMP61 vs. NTC With Linearization Resistor (R_P) Voltage Divider Circuits

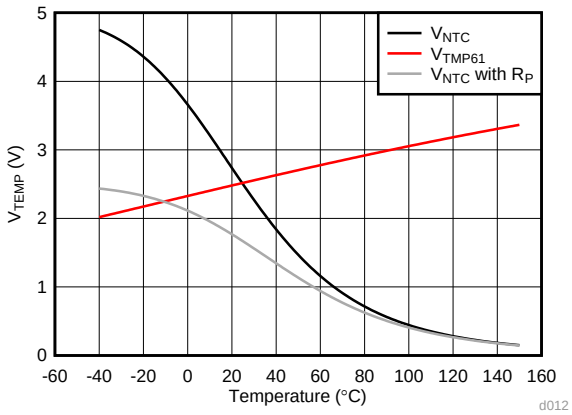


Figure 16. NTC With and Without a Linearization Resistor vs. TMP61 Temperature Voltages

9.2.1.2.1 Thermal Compensation

The TMP61 can be used to compensate for components within systems whose characteristics vary over temperature. For example, resistors will change with temperature based on their specified temperature coefficient. In certain systems where these resistors are included in the feedback loop, the performance over temperature may be greatly affected by the changes in resistance. Examples include components like those in control systems within the feedback loop, linear dropout regulators with feedback resistors, and solenoids or coils with varying impedance. One implementation is to put the TMP61 in a feedback loop to compensate for temperature drift, along with other resistive components to better control the temperature coefficient (α) of the compensation circuit.

Equation 5 can describe this type of circuit:

$$R(T) = R(T_0) \times (1 + \alpha \Delta T) \quad (5)$$

where

- $R(T_0)$ is the resistance
- the temperature coefficient, α, is specified (25°C)
- the change in temperature, ΔT, is the temperature of interest, T, minus T_0 (25°C)

This circuit is shown in Figure 17.

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Typical Application (continued)

$$R_{total} = R_S + \frac{R_{TMP61} \times R_P}{R_{TMP61} \times R_P} \quad (6)$$

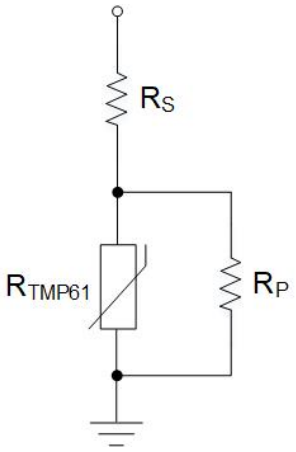


Figure 17. TMP61 Thermal Compensation Circuit

9.2.1.2.2 Thermal Protection With Comparator

The engineer can use the TMP61, a voltage reference, and a comparator to program the thermal protection. As shown in Figure 18, the output of the comparator will remain low until the voltage of the thermistor divider, with R_{BIAS} and R_{TMP61}, rises above the threshold voltage, set by R_1 and R_2. When the output goes high, the comparator signals an overtemperature warning signal. The engineer can also program the hysteresis to prevent the output from continuously toggling around the temperature threshold when the output returns low. Either a comparator with built-in hysteresis or feedback resistors may be used.

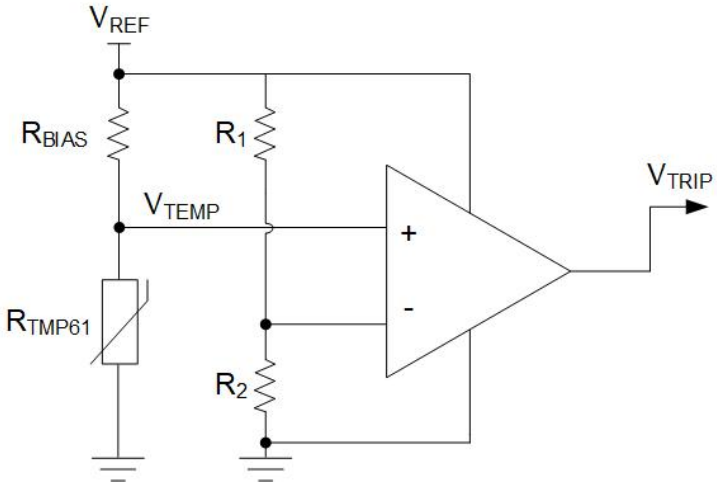


Figure 18. Temperature Switch Using TMP61 Voltage Divider and a Comparator

9.2.1.2.3 Thermal Foldback

One application that uses the output voltage of the TMP61 in an active control circuit is thermal foldback. This is performed to reduce, or fold back, the current driving a string of LEDs, for example. At high temperatures, the LEDs begin to heat up due to environmental conditions and self-heating. Thus, at a certain temperature threshold based on the LED's safe operating area, the driving current must be reduced to cool down the LEDs and prevent thermal runaway. The TMP61 voltage output increases with temperature when the output is in the lower position of the voltage divider, and can provides a response used to fold back the current. Typically, the current is held at a specified level until a high temperature is reached, known as the knee point, where the current must be rapidly

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Typical Application (continued)

reduced. To better control the temperature/voltage sensitivity of the TMP61, a rail-to-rail operational amplifier is used. In the example shown in Figure 19, the temperature "knee" where the foldback begins is set by the reference voltage (2.5 V) at the positive input, and the feedback resistors set the response of the foldback curve. The foldback knee point may be chosen based on the output of the voltage divider and the corresponding temperature from Equation 7 (like 110°C, for example). A buffer is used in-between the voltage divider with R_{TMP61} and the input to the op amp to prevent loading and variations in V_{TEMP}.

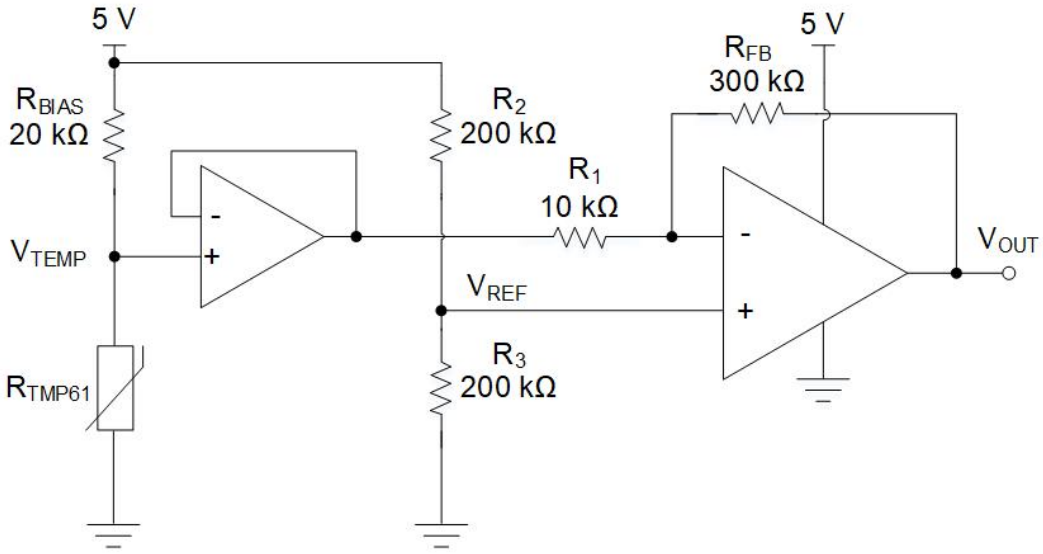


Figure 19. Thermal Foldback Using TMP61 Voltage Divider and a Rail-to-Rail Op Amp

The op amp will remain high as long as the voltage output is below V_{Ref}. When the temperature goes above 110°C, then the output will swing low to the 0-V rail of the op amp. The rate at which the foldback occurs is dependent on the feedback network, R_{FB} and R_1, which varies the gain of the op amp, G, given by Equation 8. This in return controls the voltage/temperature sensitivity of the circuit. This voltage output is fed into a LED driver IC that will adjust output current accordingly. The final output voltage used for thermal foldback is V_{OUT}, and is given in Equation 9. In this example where the knee point is set at 110°C, the output voltage curve is as shown in Figure 20.

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}} \right) \tag{7}$$

$$G = \frac{R_{FB}}{R_1} \tag{8}$$

$$V_{OUT} = -G \times V_{TEMP} + (1 + G) \times V_{REF} \tag{9}$$

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Typical Application (continued)

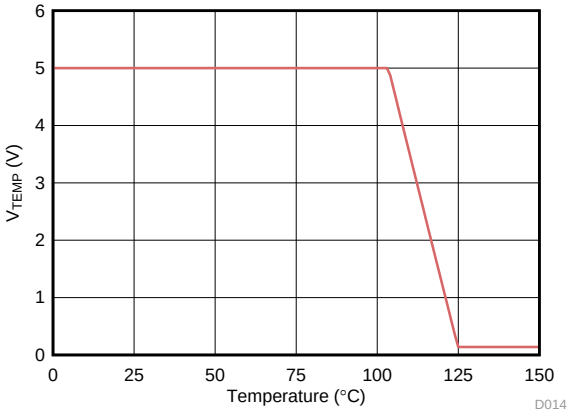


Figure 20. Thermal Foldback Voltage Output Curve

9.2.1.3 Application Curve

The TMP61 accuracy varies depending on the selected biasing circuit. This variation can be seen in Figure 21. V_{TEMP} is shown with either V_{BIAS} at 2 V in a resistor divider circuit (R_{BIAS} = 10 kΩ ±1%), or I_{BIAS} at 200 µA. Supply sources used are assumed to be ideal. The best accuracy is achieved using a direct current bias method.

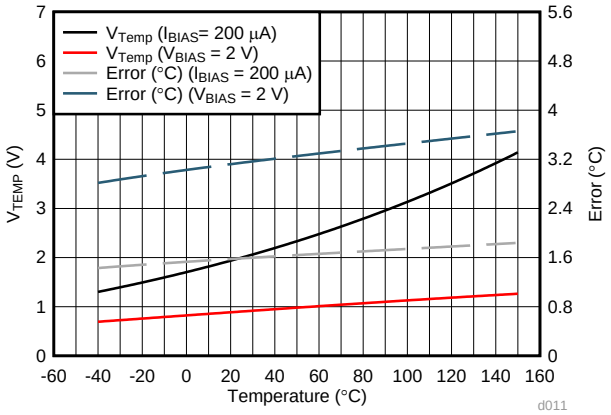


Figure 21. TMP61 Voltage Output and Temperature Error Based on the Bias Method

10 Power Supply Recommendations

The maximum recommended operating voltage of the TMP61 is 5.5 V (V_{Sns}), and the maximum current through the device is 400 µA (I_{Sns}).

11 Layout

11.1 Layout Guidelines

The layout of the TMP61 is similar to that of a passive component. If the device is biased with a current source, the positive pin 2 is connected to the source, while the negative pin 1 is connected to ground. If the circuit is biased with a voltage source, and the device is placed on the lower side of the resistor divider, V– is connected to ground and V+ is connected to the output, V_{TEMP}. If the device is placed on the upper side of the divider, V+ is connected to the voltage source and V– is connected to the output voltage, V_{TEMP}. Figure 22 shows the device layout.

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11.2 Layout Example

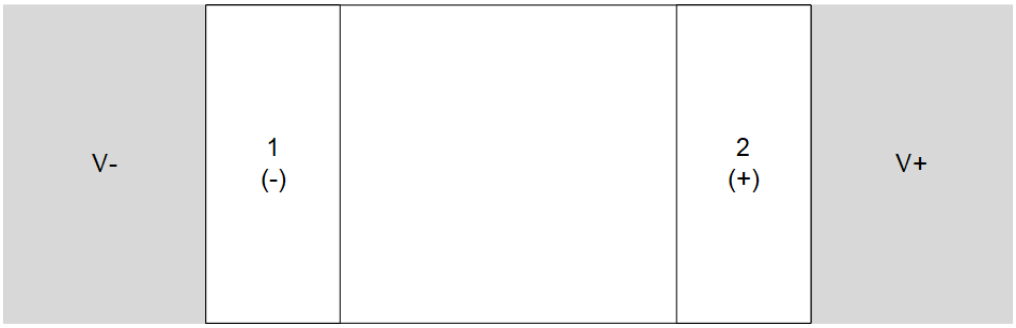


Figure 22. Recommended Layout: DEC Package

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

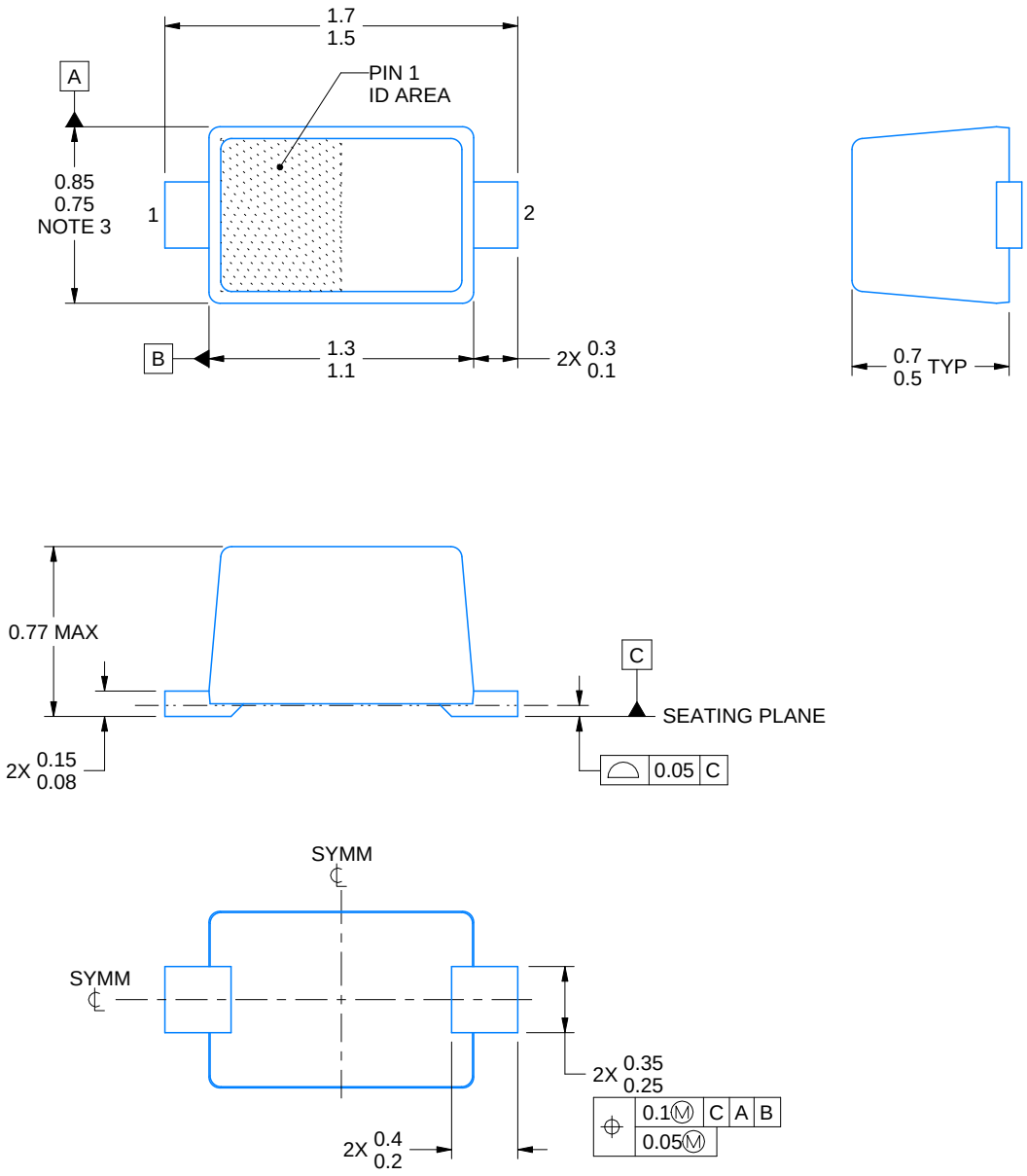
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PACKAGE OUTLINE

DYA0002A

SOT - 0.77 mm max height

PLASTIC SMALL OUTLINE



4224978/A 04/2019

NOTES:

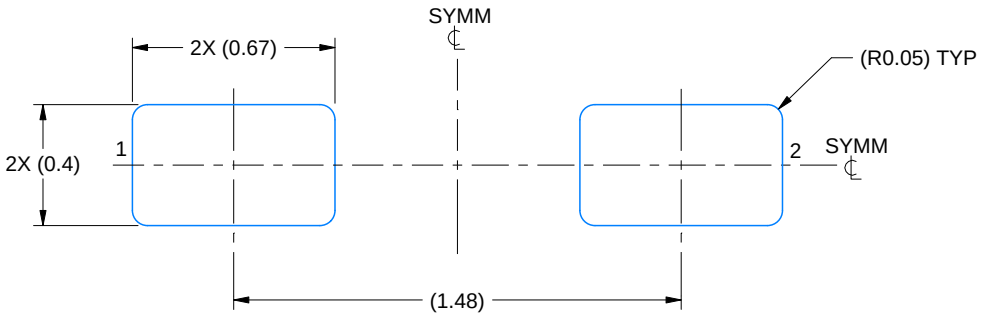
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

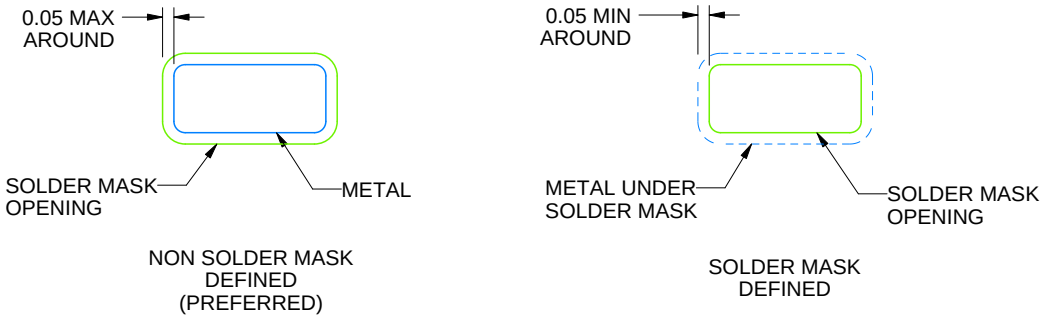
DYA0002A

SOT - 0.77 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

4224978/A 04/2019

NOTES: (continued)

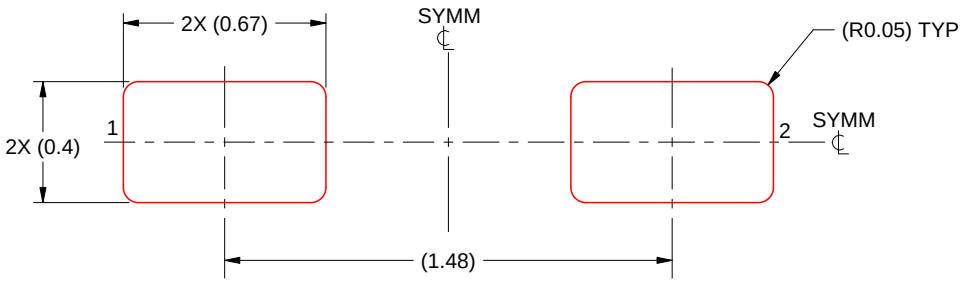
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT - 0.77 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMP6131DYAT	ACTIVE	SOT-5X3	DYA	2	250	TBD	Call TI	Call TI	-65 to 150		Samples
PTMP6131LPGM	ACTIVE	TO-92	LPG	2	3000	TBD	Call TI	Call TI	-65 to 150		Samples
TMP6131DECR	ACTIVE	X1SON	DEC	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-65 to 150	EL	Samples
TMP6131DECT	ACTIVE	X1SON	DEC	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-65 to 150	EL	Samples
TMP6131LPGM	ACTIVE	TO-92	LPG	2	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-65 to 150	TMP61	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TMP61 :

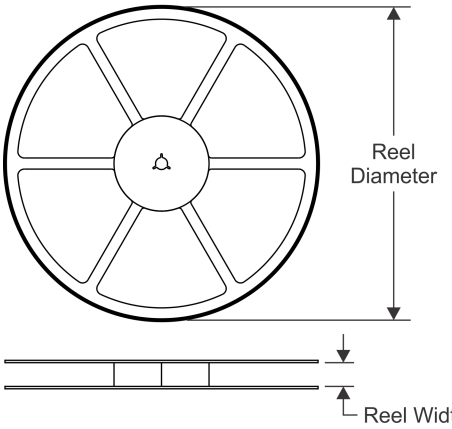
- Automotive: TMP61-Q1

NOTE: Qualified Version Definitions:

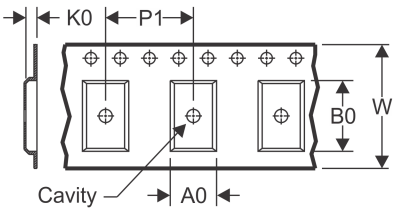
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

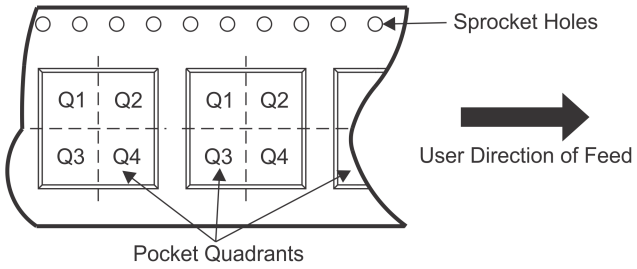


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

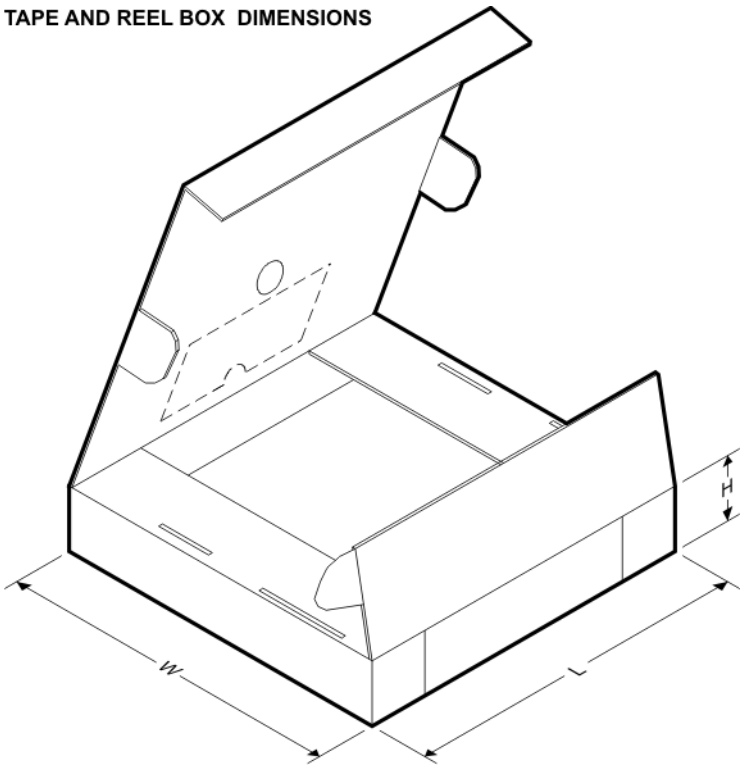
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP6131DECR	X1SON	DEC	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TMP6131DECT	X1SON	DEC	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

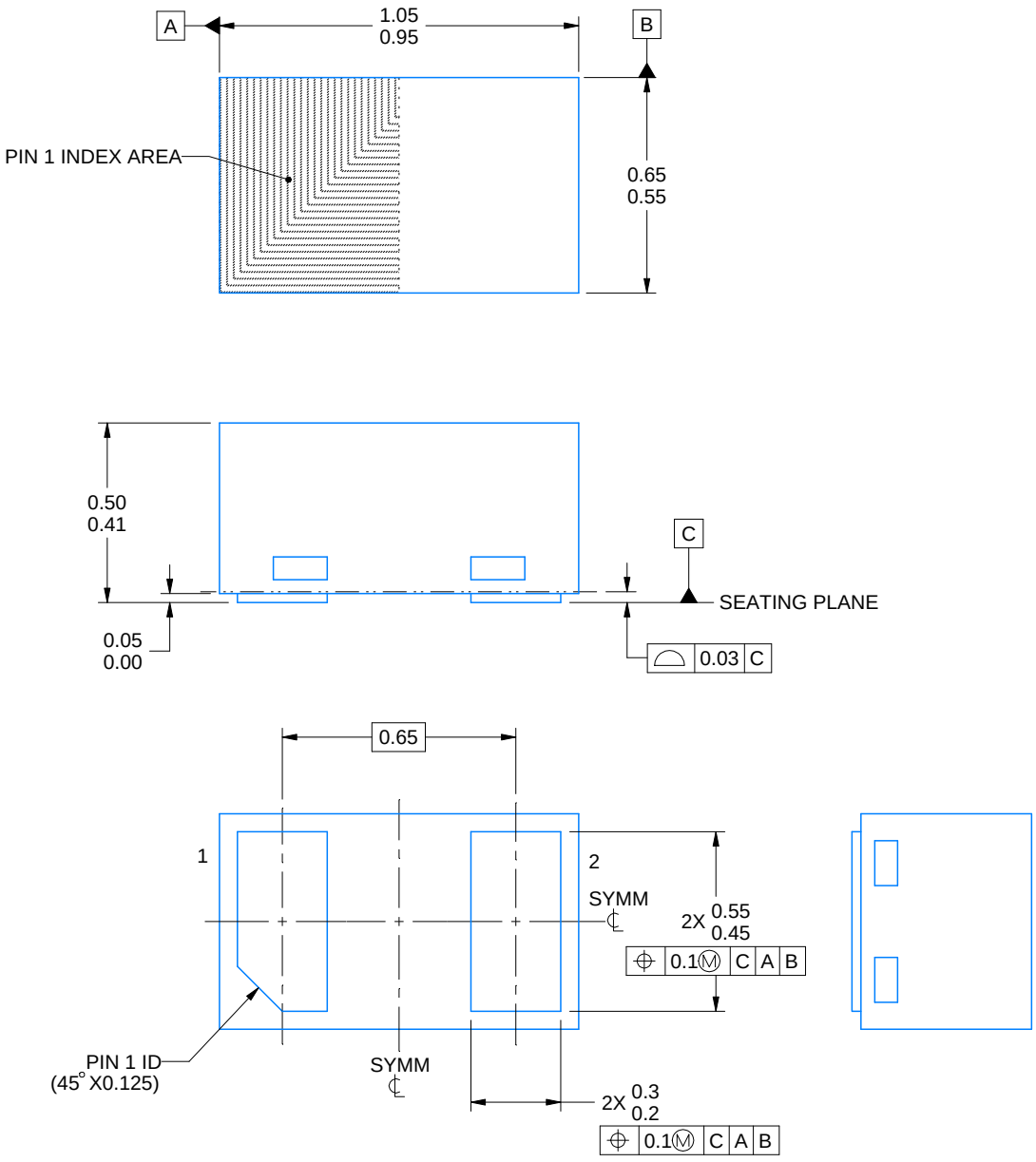
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP6131DECR	X1SON	DEC	2	10000	205.0	200.0	33.0
TMP6131DECT	X1SON	DEC	2	250	205.0	200.0	33.0

PACKAGE OUTLINE

DEC0002A

X1SON - 0.5 mm max height

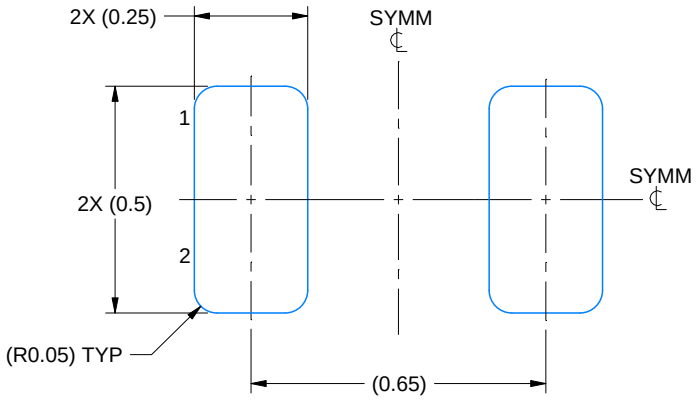
PLASTIC SMALL OUTLINE - NO LEAD



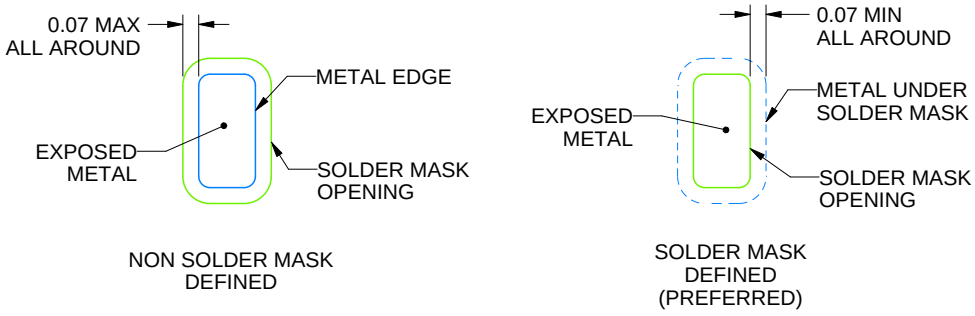
4224506/A 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

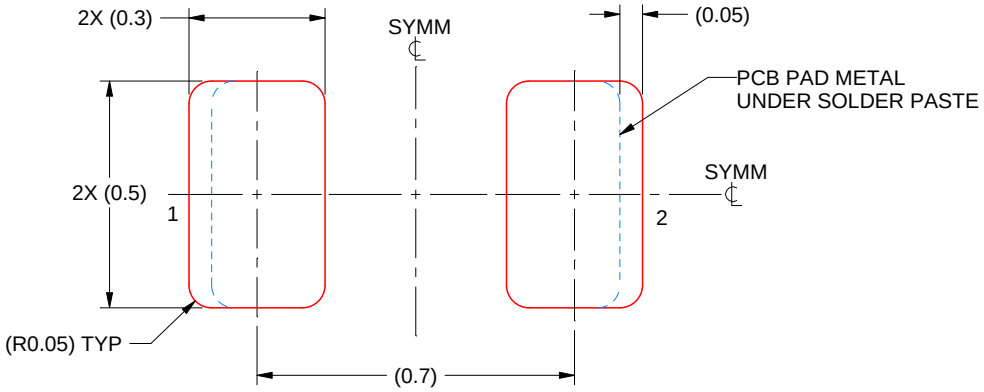


SOLDER MASK DETAILS

4224506/A 08/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224506/A 08/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

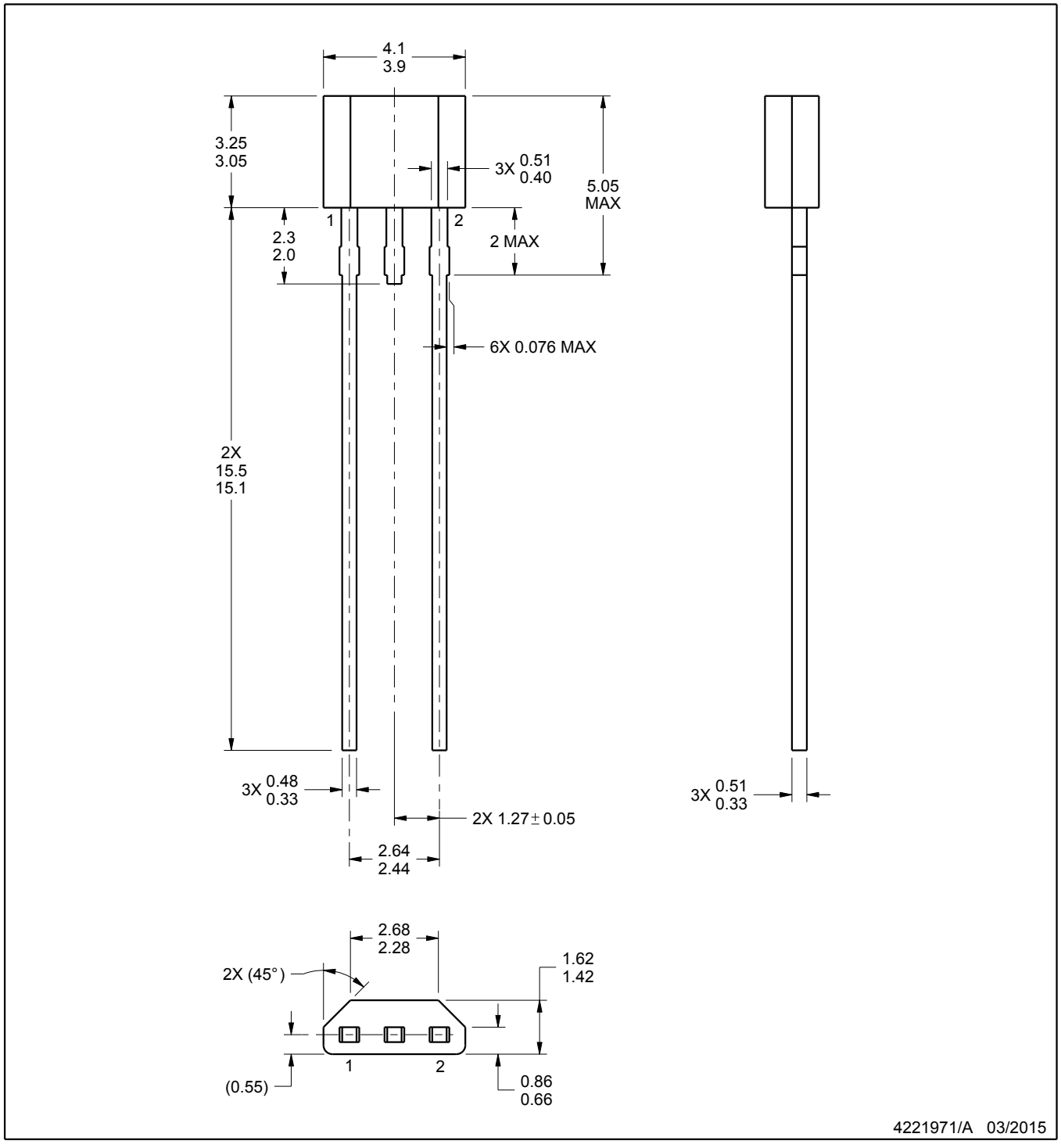


PACKAGE OUTLINE

LPG0002A

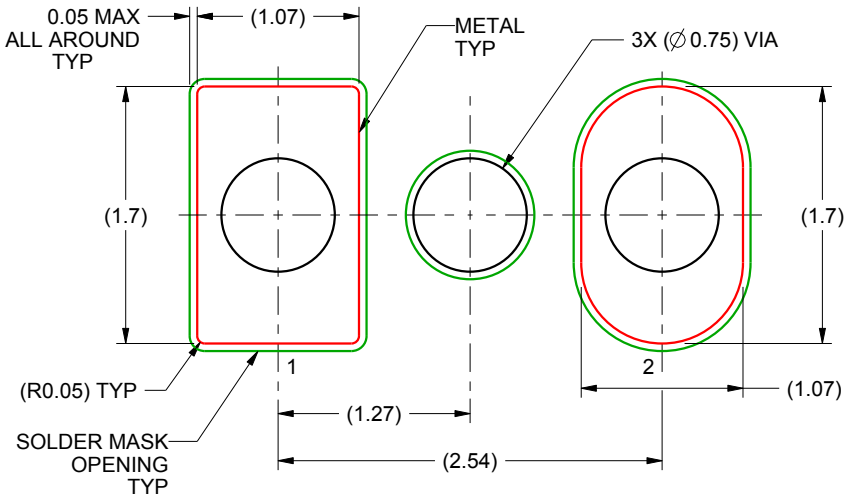
TO-92 - 5.05 mm max height

TO-92



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

4221971/A 03/2015

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