MPQ2918

4V - 40V Input, Current Mode, Synchronous, Step-Down Controller AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ2918 is a high-voltage, synchronous, step-down controller that steps down voltages directly from up to 40V. The MPQ2918 uses pulse-width modulation (PWM) current control architecture with accurate cycle-by-cycle current limiting and is capable of driving dual N-channel MOSFETs.

Advanced asynchronous mode (AAM) enables non-synchronous operation to optimize light-load efficiency.

The operating frequency of the MPQ2918 can be programmed by an external resistor or synchronized to an external clock for noise-sensitive applications. Full protection features include precision output over-voltage protection (OVP), output over-current protection (OCP), and thermal shutdown.

The MPQ2918 is available in TSSOP20-EP and QFN-20 (3mmx4mm) packages.

FEATURES

- Wide 4V to 40V Operating Input Range
- Dual N-Channel MOSFET Driver
- 0.8V Voltage Reference with ±1.5% Accuracy Over Temperature
- Low Dropout Operation: Maximum Duty Cycle at 99.5%
- Programmable Frequency Range: 100kHz - 1000kHz
- External Sync Clock Range: 100kHz - 1000kHz
- 180° Out-of-Phase SYNCO Pin
- Programmable Soft Start (SS)
- Power Good (PG) Output Voltage Monitor
- Selectable Cycle-by-Cycle Current Limit
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP)
- Internal LDO with External Power Supply Option
- Programmable Forced CCM and AAM
- Available in TSSOP20-EP and QFN-20 (3mmx4mm) Packages
- AEC-Q100 Grade-1

APPLICATIONS

- Automotive
- Industrial Control Systems

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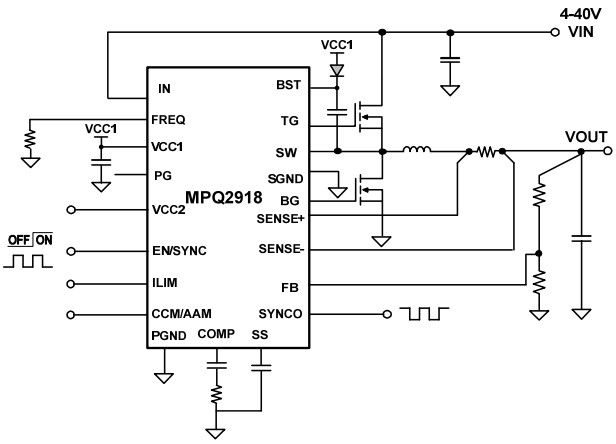
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ2918GF*	TSSOP-20 EP	*See Below*
MPQ2918GL	QFN-20 (3mmx4mm)	*See Below*
MPQ2918GF-AEC1	TSSOP-20 EP	*See Below*
MPQ2918GL-AEC1	QFN-20 (3mmx4mm)	*See Below*
MPQ2918GLE-AEC1	QFN-20 (3mmx4mm)	*See Below*

*For Tape & Reel, add suffix –Z (e.g. MPQ2918GF–Z)

TOP MARKING (MPQ2918GF & MPQ2918GF-AEC1)

MPSYYWW
MP2918
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2918: Product code of MPQ2918GF & MPQ2918GF-AEC1
LLLLLLLLL: Lot number

TOP MARKING (MPQ2918GL & MPQ2918GL-AEC1)

MPYW
2918
LLL

MP: MPS prefix
Y: Year code
W: Week code
2918: Product code of MPQ2918GL & MPQ2918GL-AEC1
LLL: Lot number

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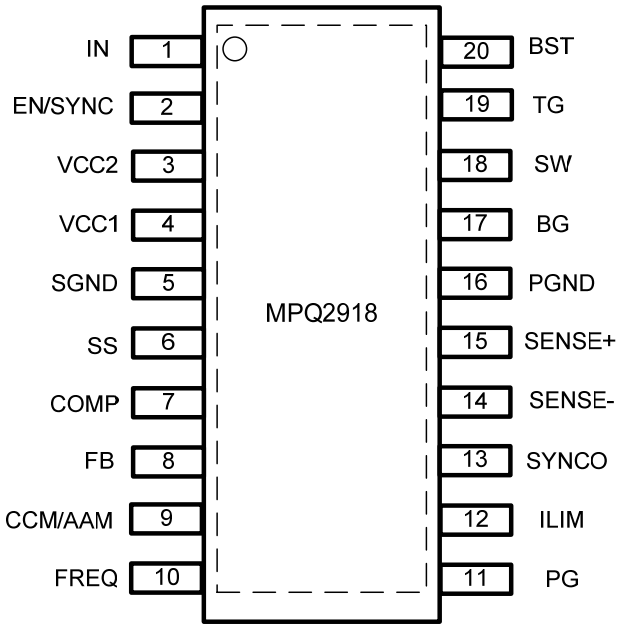
TOP MARKING (MPQ2918GLE-AEC1)

MPYW
2918
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
2918: Product code of MPQ2918GLE-AEC1
LLL: Lot number
E: Wettable lead flank

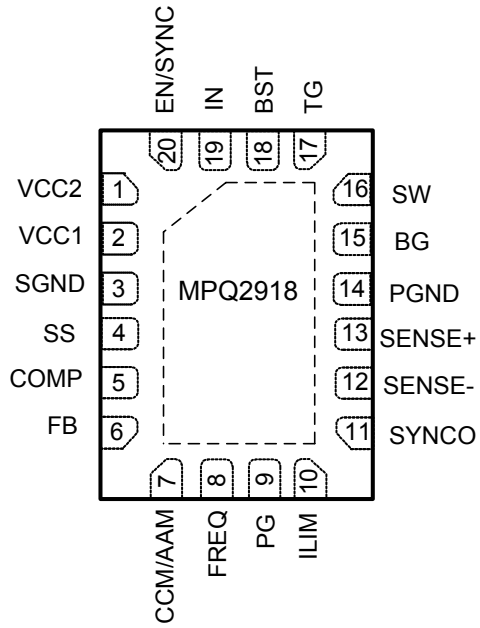
PACKAGE REFERENCE

TOP VIEW



TSSOP-20 EP

TOP VIEW



QFN-20 (3mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN}) 65V
BST supply voltage (V_{BST}) ..... V_{IN} + 6.5V
SW ..... -0.3V to 65V
EN/SYNC 55V
BST - SW 6.5V
Supply voltage (VCC1) 6.5V
External supply voltage (VCC2) 15V
SENSE + / - 28V
Differential sense (SENSE+ to SENSE-) ..... -0.7V to +0.7V
TG ..... V_{SW} - 0.3V to V_{BST} + 0.3V
BG ..... -0.3V to VCC1 + 0.3V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2)
TSSOP-20 EP 3.1W
QFN-20 (3mmx4mm) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +175°C

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 4V to 40V
Output voltage (V_{OUT}) ..... ≤25V
Supply voltage for (VCC2) ..... 4.7V to 12V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
TSSOP-20 EP	40	8	°C/W
QFN-20 (3mmx4mm)	48	10	°C/W

NOTES:

1) Absolute maximum are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, EN/SYNC = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} UVLO threshold (rising)	IN_{UV_RISING}		4	4.5	5	V
V_{IN} UVLO threshold (falling)	$IN_{UV_FALLING}$		3.2	3.7	3.95	V
V_{IN} UVLO hysteresis	IN_{UV_HYS}			800		mV
V_{IN} supply current with VCC2 bias	I_{Q_VCC2}	VCC2 = 12V, external bias, V_{AAM} = 5V, V_{FB} = 0.84V, SENSE+ = SENSE- = 0V, no switching		25	40	µA
V_{IN} supply current without VCC2 bias	I_Q	VCC2 = 0V, V_{FB} = 0.84V, V_{AAM} = 5V, SENSE+ = SENSE- = 0V, no switching		750	1000	µA
V_{IN} AAM current	I_{Q_AAM}	VCC2 = 0V, V_{AAM} = 0.6V, V_{FB} = 0.84V, SENSE+ = SENSE- = 12V, no switching		250	350	µA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V		0.5	5	µA
VCC Regulator						
VCC1 regulator output voltage from V_{IN}	$VCC1_{_VIN}$	VIN > 6V, load = 0 to 50mA	4.5	5	5.5	V
VCC1 regulator load regulation from V_{IN}		Load = 0 to 50mA, VCC2 floating or connected to SGND		1	3	%
VCC1 regulator output voltage from VCC2	$VCC1_{_VCC2}$	VCC2 > 6V		5		V
VCC1 regulator load regulation from VCC2		Load = 0 to 50mA, VCC2 = 12V		1	3	%
VCC2 UVLO threshold (rising)	$VCC2_{\ RISING}$		4.3	4.7	4.92	V
VCC2 UVLO threshold (falling)	$VCC2_{\ FALLING}$		4.05	4.45	4.75	V
VCC2 threshold hysteresis	$VCC2_{\ HYS}$			250		mV
VCC2 supply current	I_{VCC2}	V_{AAM} = 5V, V_{FB} = 0.84V, SENSE+ = SENSE- = 12V, VCC2 = 12V, no switching		800	1100	µA
		V_{AAM} = 0.6V, V_{FB} = 0.84V, SENSE+ = SENSE- =12V, VCC2 = 12V, no switching		200	300	µA
Feedback (FB)						
Feedback voltage	V_{FB}	$4V \le V_{IN} \le 40V$	0.788	0.800	0.812	V
Feedback current	I_{FB}	V_{FB} = 0.8V		10		nA
Enable (EN/SYNC)						
Enable threshold (rising)	$V_{EN\ RISING}$		1.16	1.22	1.28	V
Enable threshold (falling)	$V_{EN\ FALLING}$		1.03	1.09	1.15	V
Enable threshold hysteresis	$V_{EN\ TH}$			130		mV
Enable input current	I_{EN}	$V_{EN/SYNC}$ = 2V		2	5	µA
Enable turn-off delay	t_{OFF}		10	20	40	µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, EN/SYNC = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Oscillator and Sync						
Operating frequency	F_{SW}	R_{FREQ} = 45.3kΩ	340	430	520	kHz
Foldback operating frequency	$F_{SW_FOLDBACK}$	V_{FB} = 0.1V		50%		F_{SW}
Maximum programmable frequency	F_{SWH}		1000			kHz
Minimum programmable frequency	F_{SWL}				100	kHz
EN/SYNC frequency range	F_{SYNC}		100		1000	kHz
EN/SYNC voltage rising threshold	V_{SYNC_RISING}		2			V
EN/SYNC voltage falling threshold	$V_{SYNC_FALLING}$				0.35	V
Current Sense						
Current sense common mode voltage range	$V_{SENSE+/-}$		0		25	V
Current limit sense voltage	V_{ILIMIT}	ILIM = SGND, V_{SENSE+} = 3.3V	15	25	35	mV
		ILIM = VCC1, V_{SENSE+} = 3.3V	40	50	60	mV
		ILIM = float, V_{SENSE+} = 3.3V	65	75	85	mV
Reverse current limit sense voltage	V_{REV_ILIMIT}	ILIM = SGND, V_{SENSE+} = 3.3V		8		mV
		ILIM = VCC1, V_{SENSE+} = 3.3V		17		
		ILIM = float, V_{SENSE+} = 3.3V		24		
Valley current limit	V_{VAL_ILIMIT}	ILIM = SGND, V_{SENSE+} = 3.3V		22.5		mV
		ILIM = VCC1, V_{SENSE+} = 3.3V		47.5		
		ILIM = float, V_{SENSE+} = 3.3V		72.5		
Input current of sensor	I_{SENSE}	$V_{SENSE+/-(CM)}$ = 0V	-70	-45	-20	µA
		$V_{SENSE+/-(CM)}$ = 3.3V	80	115	160	µA
		$V_{SENSE+/-(CM)}$ > 5V	105	150	205	µA
Soft Start (SS)						
Soft-start source current	I_{SS}	SS = 0.5V	2	4	6	µA
Error Amplifier (EA)						
Error amp transconductance (4)	G_m	ΔV = 5mV		500		µS
Error amp open loop DC gain (4)	A_O			70		dB
Error amp sink/source current	I_{EA}	FB = 0.7/0.9V		±30		µA
Protection						
Over-voltage threshold	V_{OV}		110%	115%	120%	V_{FB}
Over-voltage hysteresis	V_{OV_HYS}			10%		V_{FB}
Thermal shutdown (5)				170		°C
Thermal shutdown hysteresis (5)				20		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, EN/SYNC = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
TG pull-up resistor	R_{TG_PULLUP}			2		Ω
TG pull-down resistor	R_{TG_PULLDN}			1		Ω
BG pull-up resistor	R_{BG_PULLUP}			3		Ω
BG pull-down resistor	R_{BG_PULLDN}			1		Ω
Dead time	t_{dead}	C_{Load} = 3.3nF		60		ns
TG maximum duty cycle	D_{max}	V_{FB} = 0.7V	98	99.5		%
TG minimum on time (5)	$t_{ON_MIN_TG}$			92		ns
BG minimum on time	$t_{ON_MIN_BG}$			175	250	ns
Power Good (PG)						
Power good low	V_{PG_Low}	I_{load} = 4mA		0.1	0.3	V
PG rising threshold	PG_{Vth_RSING}	V_{OUT} rising	85%	90%	96.5%	V_{FB}
		V_{OUT} falling	101%	107%	112.5%	
PG falling threshold	$PG_{Vth_FALLING}$	V_{OUT} falling	81%	87%	92.5%	V_{FB}
		V_{OUT} rising	105%	110%	116.5%	
PG threshold hysteresis	PG_{Vth_HYS}			3%		V_{FB}
Power good leakage	I_{PG_LK}	PG = 5V			2	µA
Power good delay	t_{PG_delay}	Rising		28		µs
		Falling		28		
AAM/CCM						
AAM output current	I_{AAM}	R_{FREQ} = 45.3kΩ		13.2		µA
CCM required AAM threshold voltage	V_{CCM_TH}		2.3			V

NOTES:

4) Not tested in production, guaranteed by design.
5) Not tested in production, derived from bench characterization.

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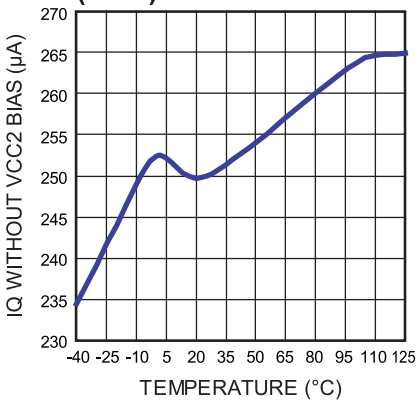
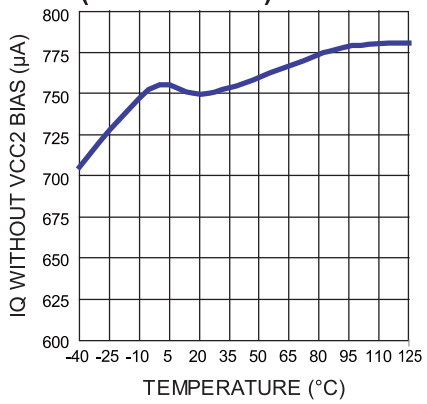
TYPICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

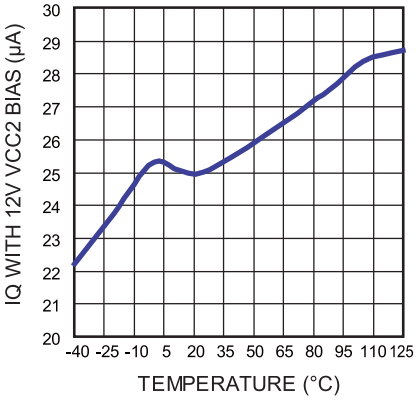
Quiescent Current without VCC2 Bias vs. Temperature (AAM)



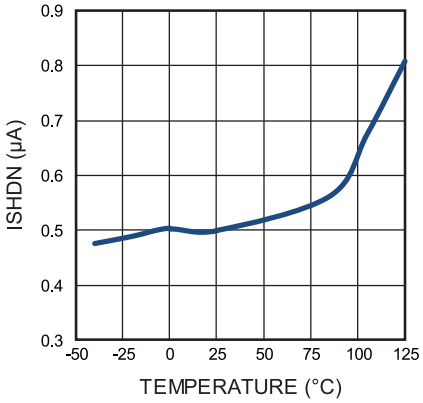
Quiescent Current without VCC2 Bias vs. Temperature (Forced CCM)



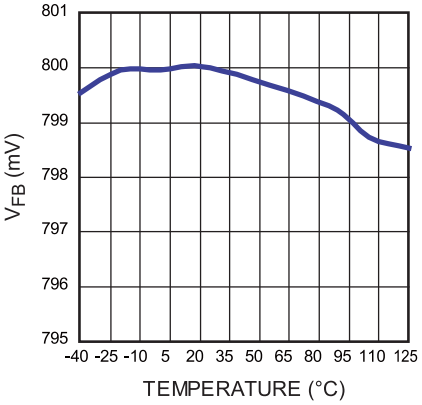
Quiescent Current with 12V VCC2 Bias vs. Temperature



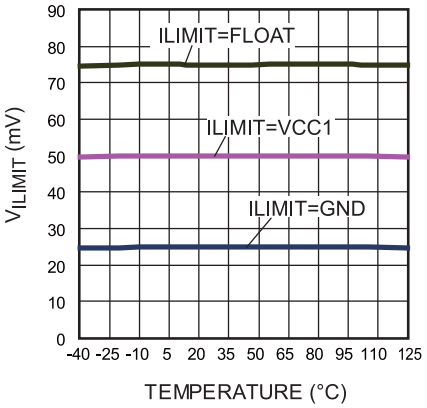
Shutdown Current vs. Temperature



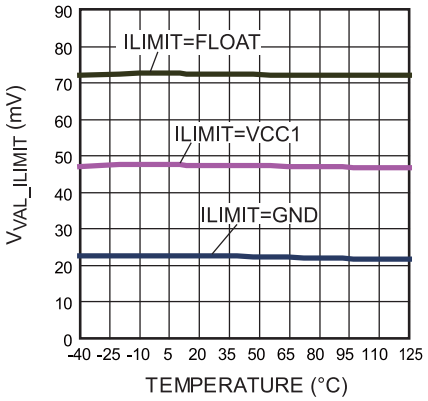
Feedback Reference vs. Temperature



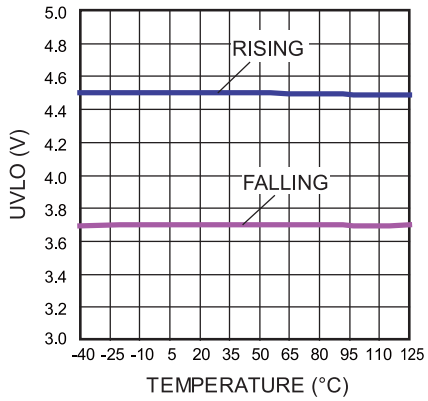
Current Limit Sense Voltage vs. Temperature



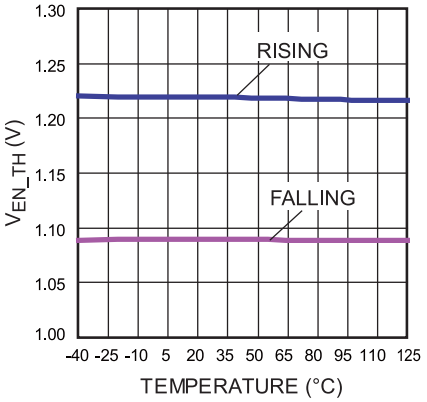
Valley Current Limit Sense Voltage vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



EN/SYNC Threshold vs. Temperature



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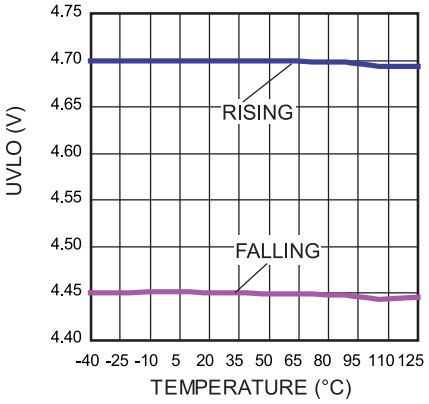
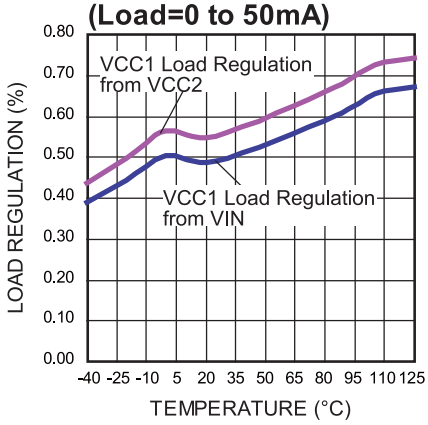
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

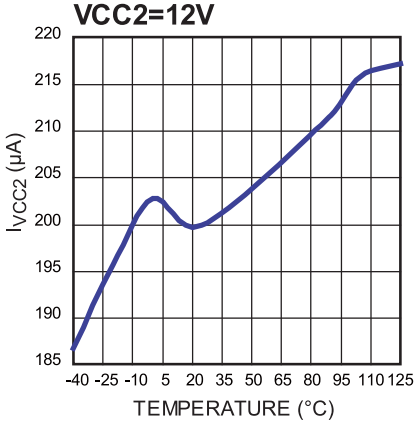
VCC2 UVLO Threshold vs. Temperature



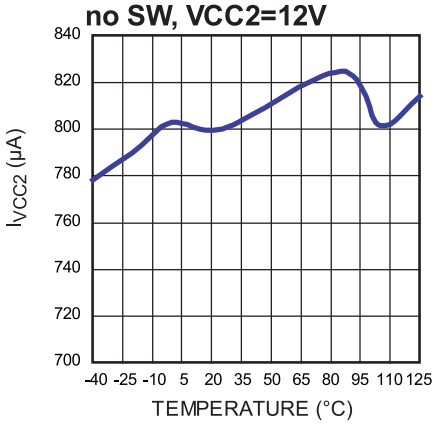
VCC1 Load Regulation vs. Temperature (Load=0 to 50mA)



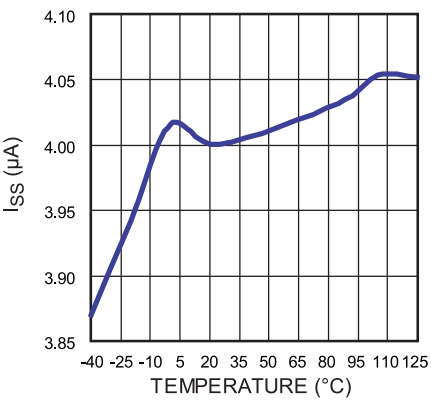
VCC2 Supply Current vs. Temperature, AAM, no SW, VCC2=12V



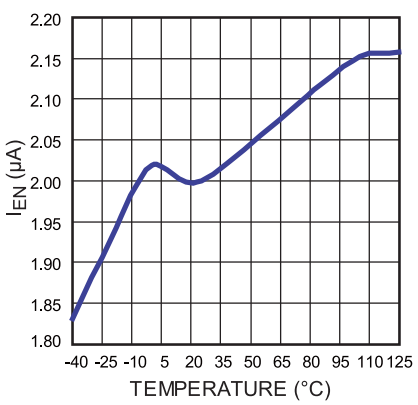
VCC2 Supply Current vs. Temperature, Forced CCM, no SW, VCC2=12V



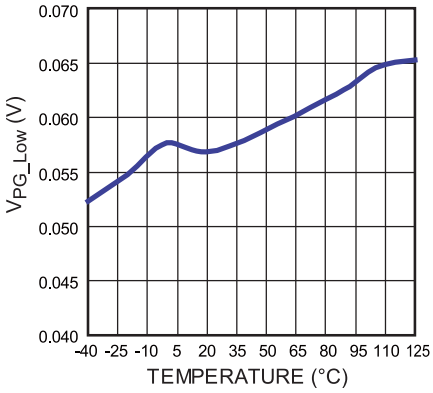
Soft-Start Source Current vs. Temperature



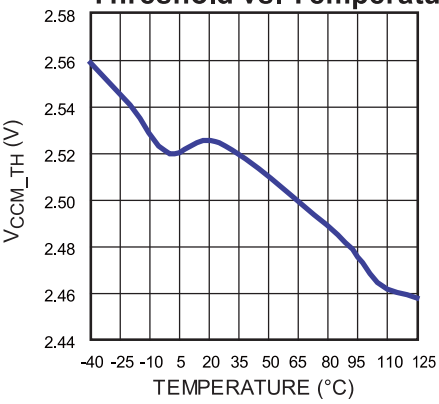
EN/SYNC Input Current vs. Temperature



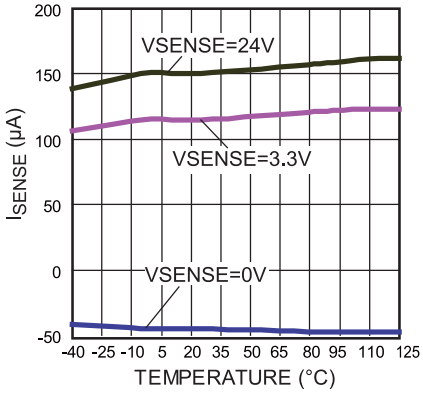
Power Good Low Voltage vs. Temperature



CCM Required AAM Threshold vs. Temperature



Input Current of Sensor vs. Temperature



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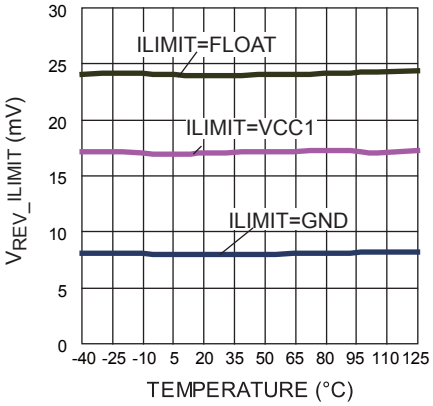
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

Reverse Current Limit Sense Voltage vs. Temperature



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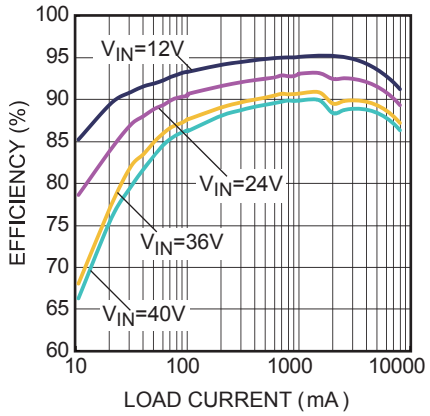
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, AAM, F_{SW} = 500kHz, T_A = +25°C, unless otherwise noted.

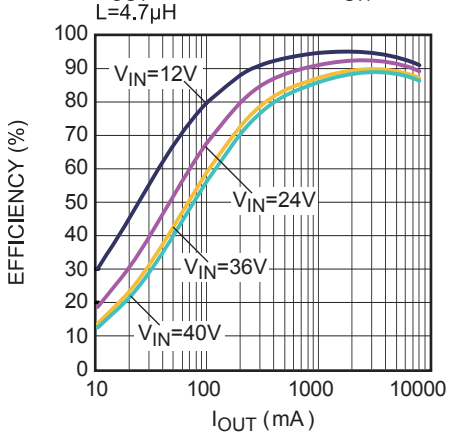
Efficiency vs. Load Current

V_{OUT}=5V, AAM, F_{SW}=500kHz, L=4.7µH

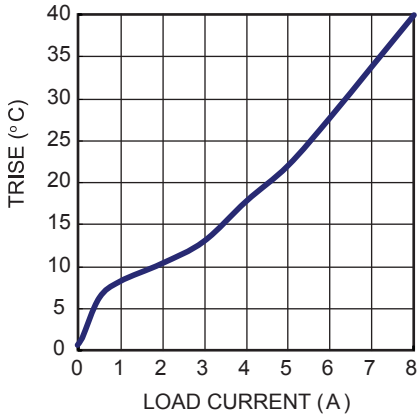


Efficiency vs. Load Current

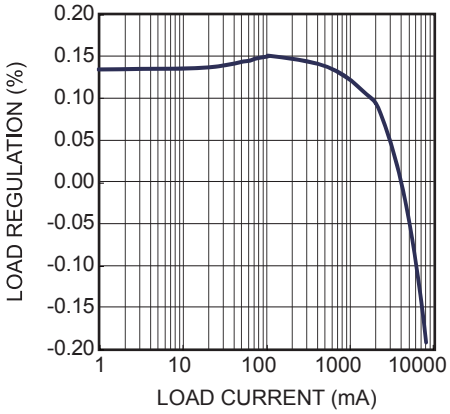
V_{OUT}=5V, Forced CCM, F_{SW}=500kHz, L=4.7µH



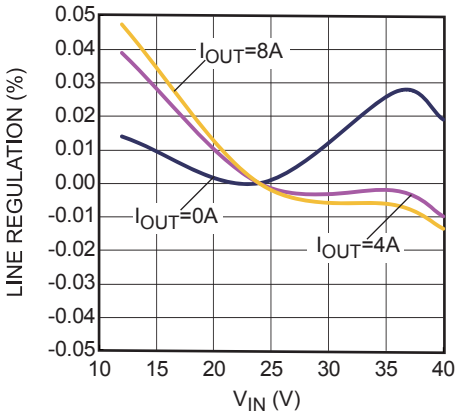
Case Temperature Rise vs. Load Current



Load Regulation



Line Regulation



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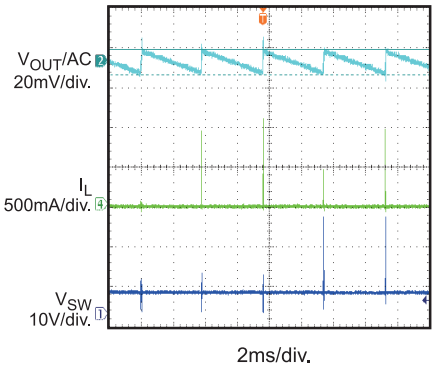
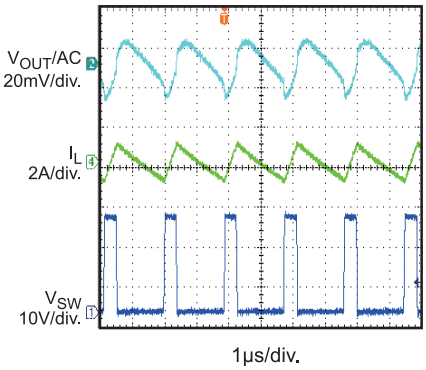
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, AAM, F_{SW} = 500kHz, T_A = +25°C, unless otherwise noted.

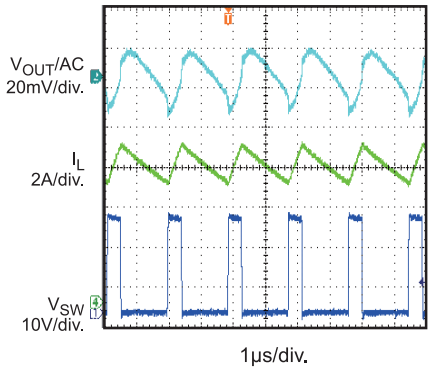
Steady State
I_{OUT}=0A, AAM Mode



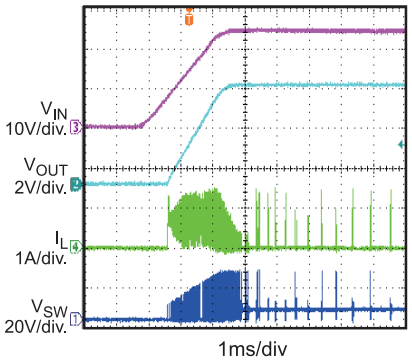
Steady State
I_{OUT}=0A, Forced CCM Mode



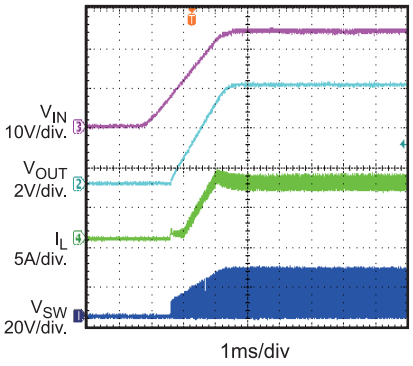
Steady State
I_{OUT}=7A



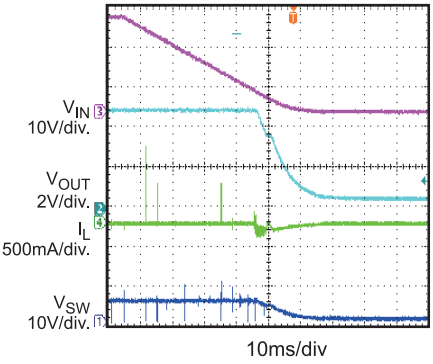
Start-Up Through V_{IN}
I_{OUT}=0A



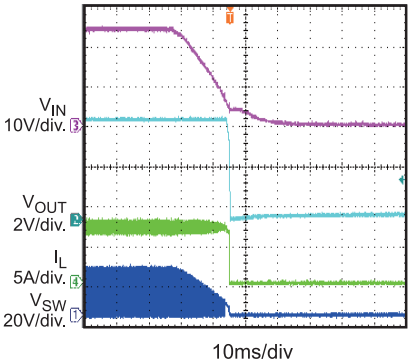
Start-Up Through V_{IN}
I_{OUT}=7A



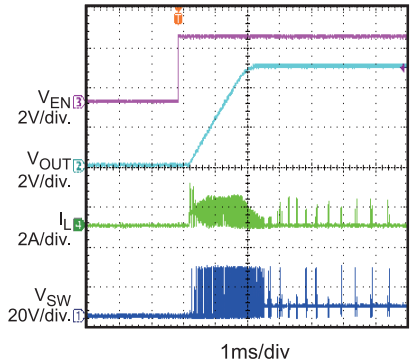
Shutdown Through V_{IN}
I_{OUT}=0A



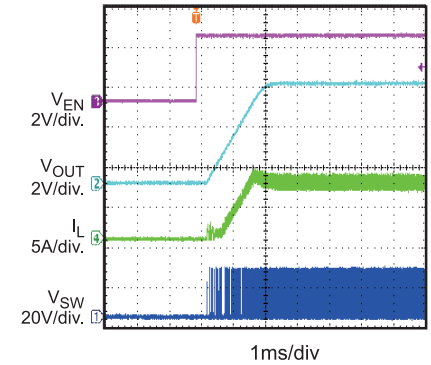
Shutdown Through V_{IN}
I_{OUT}=7A



Start-Up Through EN/SYNC
I_{OUT}=0A



Start-Up Through EN/SYNC
I_{OUT}=7A



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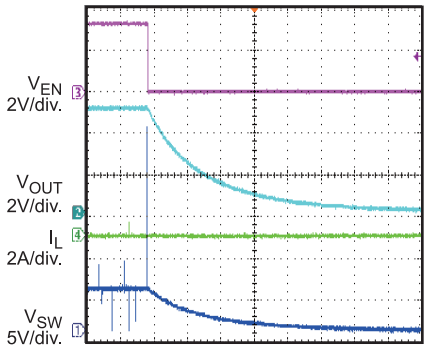
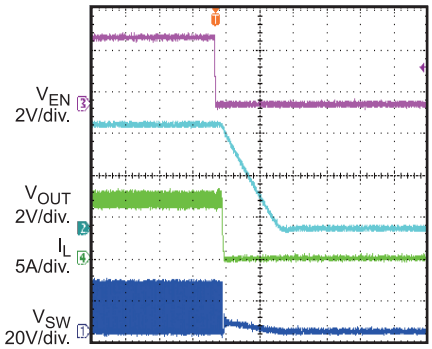
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, AAM, F_{SW} = 500kHz, T_A = +25°C, unless otherwise noted.

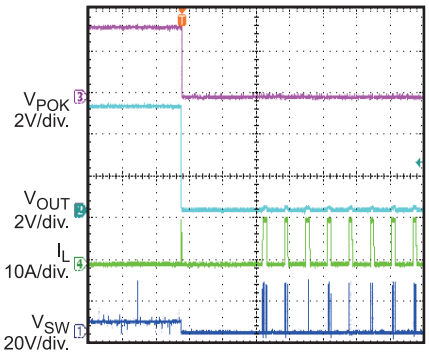
Shutdown Through EN/SYNC
I_{OUT}=0A



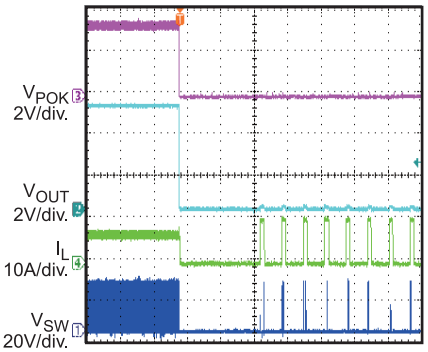
Shutdown Through EN/SYNC
I_{OUT}=7A



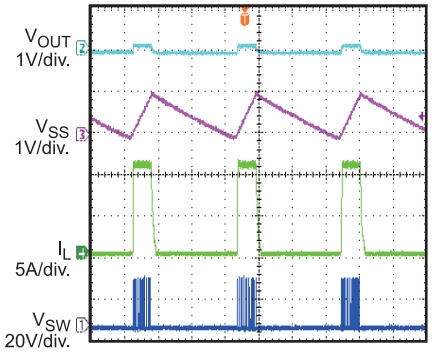
SCP Entry
I_{OUT}=0A to short circuit



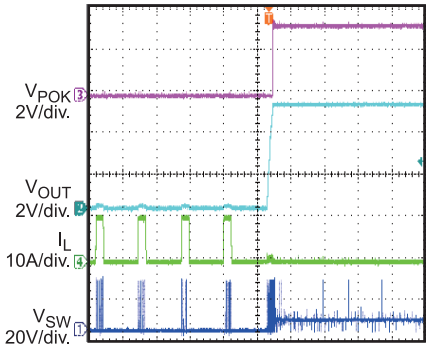
SCP Entry
I_{OUT}=7A to short circuit



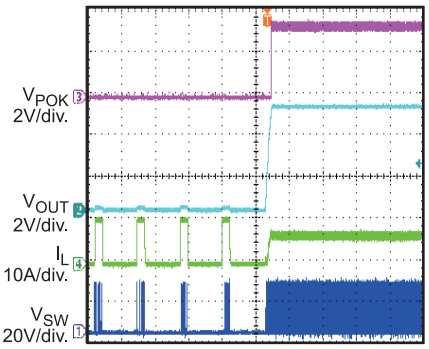
SCP Steady State



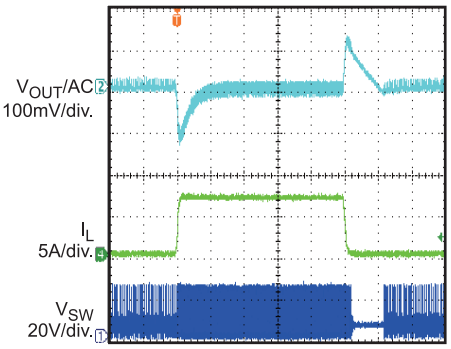
SCP Recovery
short circuit to I_{OUT}=0A



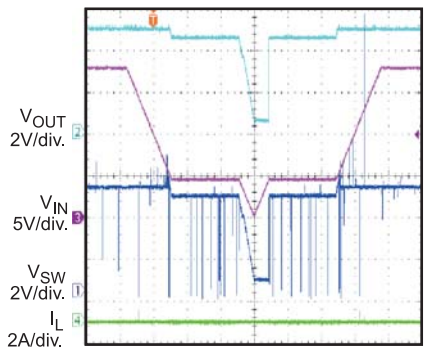
SCP Recovery
short circuit to I_{OUT}=7A



Load Transient
I_{OUT}=0.2A<->7A, 1.6A/µs



Test Pulse, Slow Ramp Up/Down
I_{OUT}=0A,AAM mode



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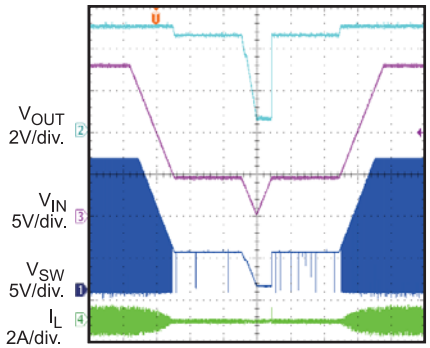
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, AAM, F_{SW} = 500kHz, T_A = +25°C, unless otherwise noted.

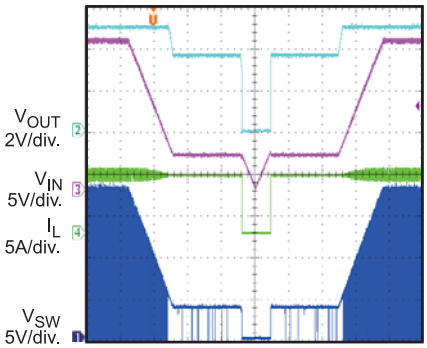
Test Pulse, Slow Ramp Up/Down

I_{OUT}=0A,AAM mode



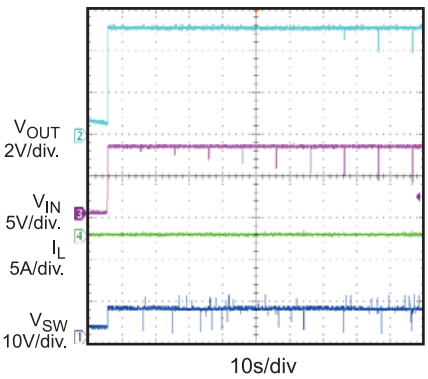
Test Pulse, Slow Ramp Up/Down

I_{OUT}=7A



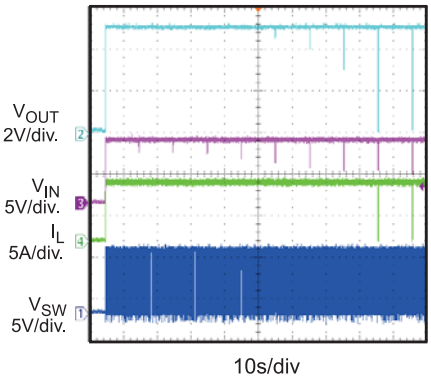
Test Pulse, Reset

V_{IN}=8V,I_{OUT}=0A,AAM mode



Test Pulse, Reset

V_{IN}=8V,I_{OUT}=7A



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PIN FUNCTIONS

TSSOP-20 Pin #	QFN-20 Pin #	Name	Description
1	19	IN	**Input supply.** The MPQ2918 operates on a 4V to 40V input range. A ceramic capacitor is needed to prevent large voltage spikes at the input.
2	20	EN/SYNC	**Enable input.** The EN/SYNC threshold is 1.22V with 130mV of hysteresis. EN/SYNC is used to implement an input under-voltage lockout (UVLO) function externally. If an external sync clock is applied to EN/SYNC, the internal clock follows the sync frequency.
3	1	VCC2	**External power supply for the internal VCC1 regulator.** VCC2 disables the power from V_{IN} for as long as VCC2 is higher than 4.7V. Do not connect a power supply greater than 12V to VCC2. Connect VCC2 to an external power supply to reduce power dissipation and increase efficiency.
4	2	VCC1	**Internal bias supply.** A ≥1μF decoupling capacitor is required between VCC1 and PGND.
5	3	SGND	**Low-noise ground reference.** SGND should be connected to the V_{OUT} side of the output capacitors.
6	4	SS	**Soft-start control input.** SS is used to program the soft-start period with an external capacitor between SS and SGND.
7	5	COMP	**Regulation control loop compensation.** Connect an R-C network from COMP to SGND to compensate for the regulation control loop.
8	6	FB	**Feedback.** FB is the input of the error amplifier. An external resistive divider connected between the output and SGND is compared to the internal +0.8V reference to set the regulation voltage.
9	7	CCM/AAM	**Continuous conduction mode/advanced asynchronous mode.** Floating CCM/AAM or connecting CCM/AAM to VCC1 makes the part operate in CCM. Connecting an appropriate external resistor from CCM/AAM to SGND (so AAM is at a low level) makes the part operate in AAM. The AAM voltage should be no less than 480mV.
10	8	FREQ	**Frequency.** Connect a resistor between FREQ and SGND to set the switching frequency.
11	9	PG	**Power good output.** The output of PG is an open drain.
12	10	ILIM	**Sense voltage limit set.** The voltage at ILIM sets the nominal sense voltage at the maximum output current. There are three fixed options: float, VCC1, and SGND.
13	11	SYNCO	**Frequency synchronous out.** SYNCO outputs a 180° out-of-phase clock when the part works in CCM for dual-channel operation.
14	12	SENSE-	**Negative input for the current sense.** The sensed inductor current limit threshold is determined by the status of ILIM.
15	13	SENSE+	**Positive input for the current sense.** The sensed inductor current limit threshold is determined by the status of ILIM.
16	14	PGND	**High-current ground reference for the internal low-side switch driver and the VCC1 regulator circuit.** Connect PGND to the negative terminal of the VCC1 decoupling capacitor directly.

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PIN FUNCTIONS *(continued)*

TSSOP-20 Pin #	QFN-20 Pin #	Name	Description
17	15	BG	**Bottom gate driver output.** Connect BG to the gate of the synchronous N-channel MOSFET.
18	16	SW	**Switch node.** SW is the reference for the V_{BST} supply and high-current returns for the bootstrapped switch.
19	17	TG	**Top gate drive.** TG drives the gate of the top N-channel synchronous MOSFET. The TG driver draws power from the BST capacitor and returns to SW, providing a true floating drive to the top N-channel MOSFET.
20	18	BST	**Bootstrap.** BST is the positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BST and SW. A diode from VCC1 to BST charges the BST capacitor when the low-side switch is off.
		Exposed pad	**Exposed pad.** The exposed pad is on the bottom side of the device. It is not connected to SGND or PGND electrically. Connect the exposed pad to SGND and PGND during PCB layout for better thermal performance.

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BLOCK DIAGRAM

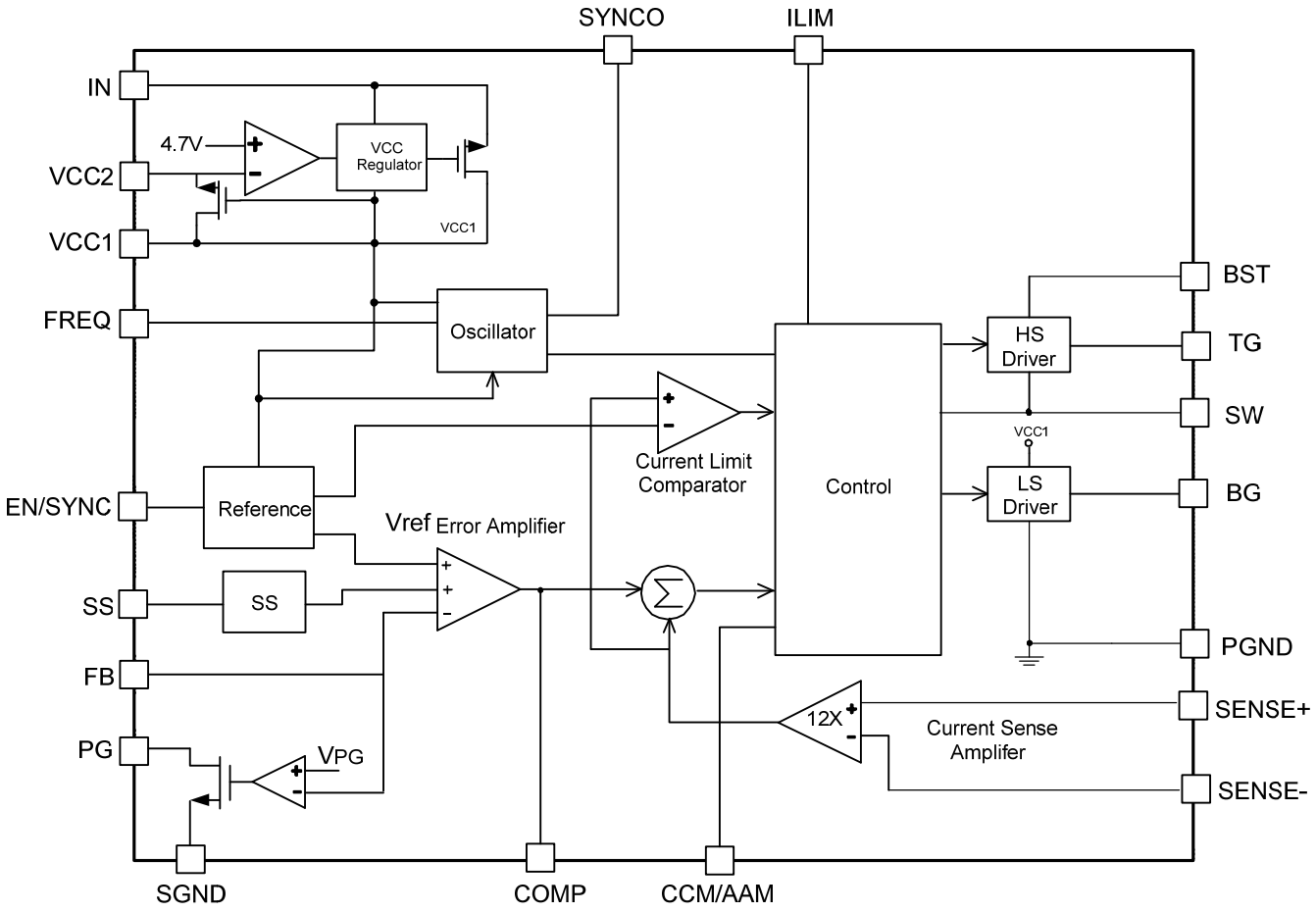

Figure 1: Functional Block Diagram

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TIMING SEQUENCE

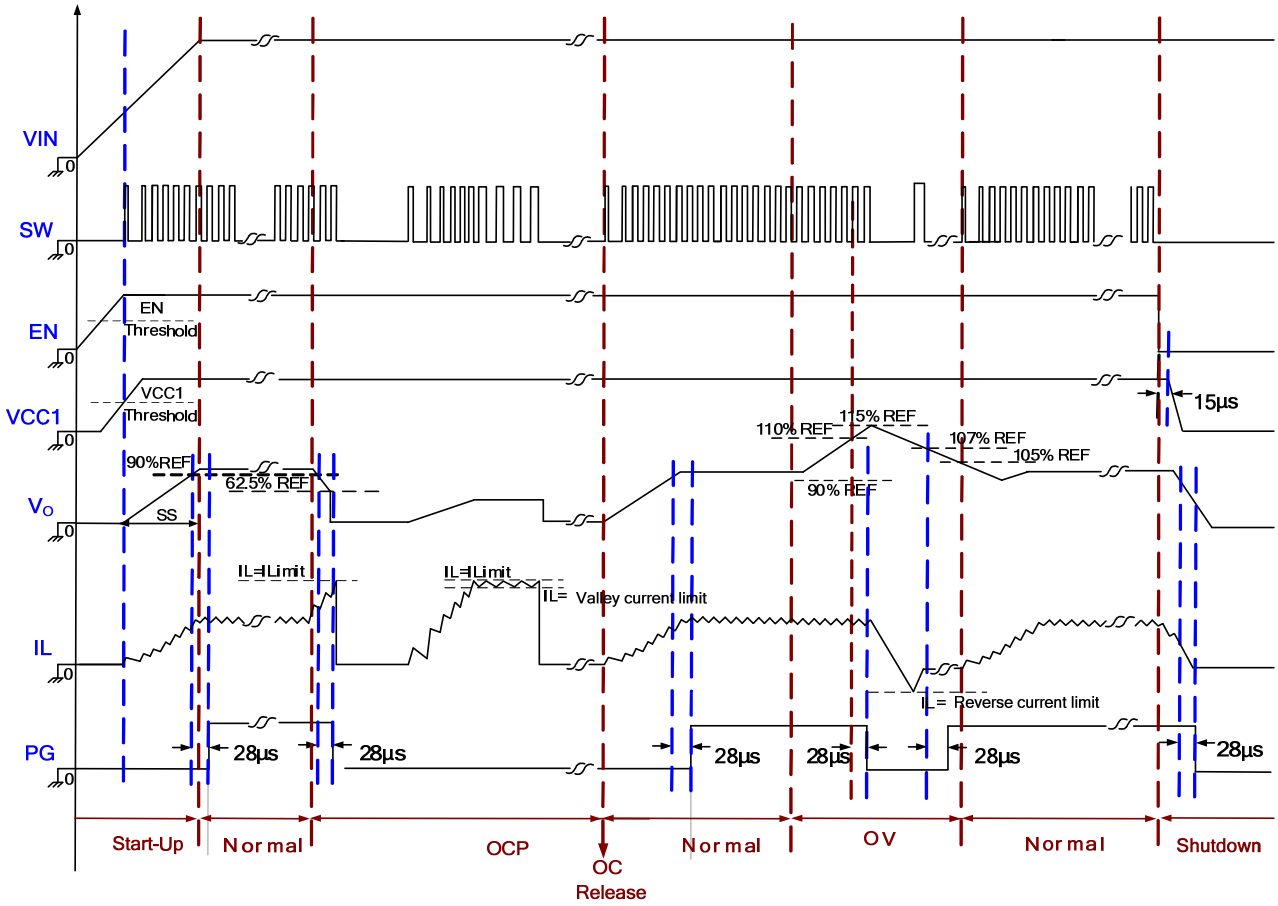

Figure 2: Time Sequence

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OPERATION

The MPQ2918 is a high-performance, step-down, synchronous, DC/DC controller IC with a wide input voltage range. It implements current-mode control and programmable switching frequency control architecture to regulate the output voltage with external N-channel MOSFETs.

The MPQ2918 senses the voltage at FB. The difference between the FB voltage (V_{FB}) and an internal 0.8V reference (V_{REF}) is amplified to generate an error voltage on COMP. This is used as the threshold for the current-sense comparator with a slope compensation ramp.

Under normal-load conditions, the controller operates in full pulse-width modulation (PWM) mode (see Figure 3). At the beginning of each oscillator cycle, the top gate driver is enabled. The top gate turns on for a period determined by the duty cycle. When the top gate turns off, the bottom gate turns on after a dead time and remains on until the next clock cycle begins.

There is an optional power-save mode for light-load or no-load condition.

Advanced Asynchronous Mode (AAM)

The MPQ2918 employs advanced asynchronous mode (AAM) functionality to optimize efficiency during light-load or no-load condition (see Figure 3). AAM is enabled when CCM/AAM is at a low level by connecting an appropriate resistor to SGND to ensure that the AAM voltage (V_{AAM}) is no less than 480mV. See Equation (1):

$$V_{AAM}\,(mV) = I_{AAM}\,(\mu A) \times R_{AAM}\,(k\Omega) \qquad (1)$$

Where I_{AAM} is the CCM/AAM output current.

AAM is disabled when CCM/AAM is floating or connected to VCC1. Calculate the CCM/AAM output current (I_{AAM}) with Equation (2):

$$I_{AAM}\,(\mu A) = 600\,(mV) / R_{FREQ}\,(k\Omega) \qquad (2)$$

If AAM is enabled, the MPQ2918 first enters non-synchronous operation for as long as the inductor current approaches zero at light load. If the load decreases further to make the COMP voltage (V_{COMP}) drop below the CCM/AAM voltage (V_{AAM}), the MPQ2918 enters AAM. In AAM, the internal clock resets whenever V_{COMP} crosses over V_{AAM}. The crossover time is taken as the benchmark for the next clock cycle. When the load increases and the DC value of V_{COMP} is higher than V_{AAM}, the operation mode is discontinuous conduction mode (DCM) or continuous conduction mode (CCM), which have a constant switching frequency.

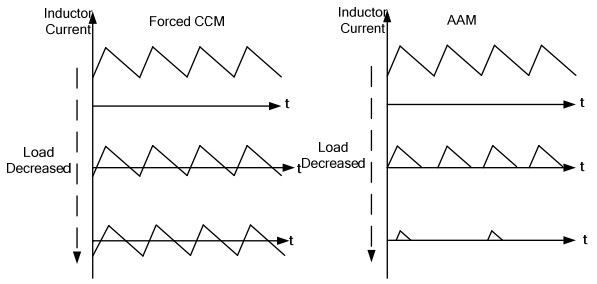

Figure 3: Forced CCM and AAM

Floating Driver and Bootstrap Charging

The floating top gate driver is powered by an external bootstrap capacitor (C_{BST}), which is refreshed when the high-side MOSFET (HS-FET) turns off, typically. This floating driver has its own under-voltage lockout (UVLO) protection. This UVLO's rising threshold is 3.05V with a hysteresis of 170mV.

If the BST voltage is lower than the bootstrap UVLO, the MPQ2918 enters constant-off-time mode to ensure that the BST capacitor is high enough to drive the HS-FET.

VCC1 Regulator and VCC2 Power Supply

Both the top and bottom MOSFET drivers and most of the internal circuitries are powered by the VCC1 regulator. An internal, low dropout, linear regulator supplies VCC1 power from V_{IN}. Connect a ≥1μF ceramic capacitor from VCC1 to PGND.

If VCC2 is left open or connected to a voltage less than 4.7V, an internal 5V regulator supplies power to VCC1 from V_{IN}. If VCC2 is greater than 4.7V, the internal regulator that supplies power to VCC1 from VCC2 is triggered. If VCC2 is between 4.7V and 5V, the 5V regulator is in dropout, and VCC1 approximately equals VCC2. Using the VCC2 power supply allows the VCC1 power to be derived from a high-efficiency external source, such as one of the MPQ2918's switching regulator outputs.

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Error Amplifier (EA)

The error amplifier (EA) compares V_{FB} with the internal 0.8V reference and outputs a current proportional to the difference between the two input voltages. This output current is used to charge or discharge the external compensation network to form V_{COMP}, which is used to control the power MOSFET current. Adjusting the compensation network from COMP to SGND optimizes the control loop for good stability or fast transient response.

Current Limit Function

The MPQ2918 has three fixed current limit options: 25mV, when ILIM is connected to SGND; 50mV, when ILIM is connected to VCC1; and 75mV, when ILIM is floating.

When the peak value of the inductor current exceeds the set current-limit threshold, the output voltage begins dropping until FB is 37.5% below the reference. The MPQ2918 enters hiccup mode to restart the part periodically. The frequency is lowered when FB is below 0.4V. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues. The MPQ2918 exits hiccup mode once the over-current condition is removed.

Low Dropout Operation

In low dropout mode, the MPQ2918 is designed to operate in high-side fully on mode for as long as the voltage difference across BST - SW is greater than 3.05V, improving dropout. When the voltage from BST to SW drops below 3.05V, a UVLO circuit turns off the HS-FET. At the same time, the low-side MOSFET (LS-FET) turns on to refresh the charge on the BST capacitor. After the BST capacitor voltage is re-charged, the HS-FET turns on again to regulate the output. Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the BST capacitor, increasing the effective duty cycle of the switching regulator. Low dropout operation makes the MPQ2918 suitable for automotive cold-crank applications.

Power Good (PG) Function

The MPQ2918 includes an open-drain power good (PG) output that indicates whether the regulator's output is within ±10% of its nominal value. When the output voltage falls outside of this range, the PG output is pulled low. PG should be connected to a voltage source no more than 5V through a resistor (e.g.: 100kΩ). The PG delay time is 28μs.

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to 1.2V. When it is lower than REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

An external capacitor connected from SS to SGND is charged from an internal 4μA current source, producing a ramped voltage. The soft-start time (t_{SS}) is set by the external SS capacitor and can be calculated by Equation (3):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (3)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.8V), and I_{SS} is the 4μA SS charge current. There is no internal SS capacitor. SS is reset when a fault protection other than over-voltage protection (OVP) occurs.

Output Over-Voltage Protection (OVP)

The output over-voltage is monitored by V_{FB}. If V_{FB} is typically 15% higher than the reference, the MPQ2918 enters discharge mode. The HS-FET turns off, and the LS-FET turns on. The LS-FET remains on until the reverse current limit is triggered. The LS-FET then turns off, and the inductor current increases to 0. The LS-FET is turned on again after ZCD is triggered. The MPQ2918 works in discharge mode until the over-voltage condition is cleared.

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EN/SYNC Control

The MPQ2918 has a dedicated enable (EN/SYNC) control that uses a bandgap-generated precision threshold of 1.22V. By pulling EN/SYNC high or low, the IC can be enabled or disabled. To disable the part, EN/SYNC must be pulled low for at least 40μs.

Tie EN/SYNC to V_{IN} through a resistor divider (R16 and R17) to program the V_{IN} start-up threshold (see Figure 4). The EN/SYNC threshold is 1.09V (falling edge), so the V_{IN} UVLO threshold is 1.09V x (1 + R16/R17).

Otherwise, if V_{IN} ≤ 52V, EN/SYNC can be connected to V_{IN} directly. If V_{IN} ≥ 52V, a ≥50kΩ pull-up resistor is needed to prevent EN/SYNC from breaking down.

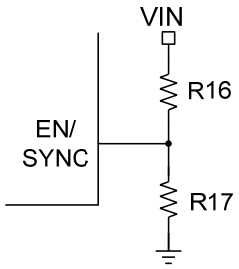

Figure 4: EN/SYNC Resistor Divider

Synchronize

The MPQ2918 can be synchronized to an external clock ranging from 100kHz up to 1000kHz through EN/SYNC. The internal clock rising edge is synchronized to the external clock rising edge. The pulse width (both on and off) of the external clock signal should be no less than 100ns.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at an insufficient input supply voltage. The MPQ2918 UVLO rising threshold is about 4.5V, while its falling threshold is a consistent 3.7V.

Thermal Protection

Thermal protection prevents damage to the IC from excessive temperatures. The die temperature is monitored internally until the thermal limit is reached. When the silicon die temperature is higher than 170°C, the entire chip shuts down. When the temperature is lower than its lower threshold (typically 20°C), the chip is enabled again.

Start-Up and Shutdown

If both V_{IN} and EN/SYNC are higher than their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents. The internal regulator is then enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN/SYNC low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signal path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Pre-Bias Start-Up

If SS is less than FB at start-up, the output has a pre-bias voltage, and neither TG nor BG is turned on until SS is greater than FB.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Figure 5).

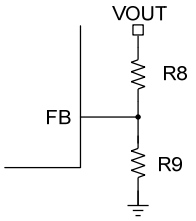

Figure 5: External Resistor Divider

If R8 is known, then R9 can be calculated with Equation (4):

$$R_9 = \frac{R_8}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R8 (kΩ)	R9 (kΩ)
3.3	37.4 (1%)	12 (1%)
5	63.4 (1%)	12 (1%)
12	169 (1%)	12 (1%)

Setting Current Sensing

The MPQ2918 has three fixed current limit options: 25mV, when ILIM is connected to SGND; 50mV, when ILIM is connected to VCC1; and 75mV, when ILIM is floating. Ensure that the application can deliver a full load of current over the full operating temperature range when setting ILIM.

The current sense resistor (R_{SENSE}) monitors the inductor current. Its value is chosen based on the current limit threshold. The relationship between the peak inductor current (I_{pk}) and R_{SENSE} can be calculated with Equation (5):

$$R_{SENSE} = \frac{V_{ILIMIT}}{Ipk} \quad (5)$$

A higher R_{SENSE} value increases the power loss across it. Considering the output current, efficiency, and ILIM threshold, the recommended value for R_{SENSE} is between 7mΩ and 50mΩ.

Programmable Switching Frequency

Consider different variables when choosing the switching frequency. A high frequency increases switching losses and gate charge losses, while a low frequency requires more inductance and capacitance, resulting in larger real estate and higher cost. Setting the switching frequency is a trade-off between power loss and passive component size. In noise-sensitive applications, the switching frequency should be out of a sensitive frequency band.

The MPQ2918's frequency can be programmed from 100kHz to 1000kHz with a resistor from FREQ to SGND (see Table 2). The value of R_{FREQ} for a given operating frequency can be calculated with Equation (6):

$$R_{FREQ}(k\Omega) = \frac{20000}{f_s(kHz)} - 1 \quad (6)$$

Table 2: Frequency vs. Resistor

Resistor (kΩ)	Frequency (kHz)
65	300
45.3	430
39	500
19	1000

VCC Regulator Connection

VCC1 can be powered from both V_{IN} and VCC2. If connecting VCC2 to an external power supply to improve the overall efficiency, VCC2 should be larger than 4.7V but smaller than 12V (see Figure 6).

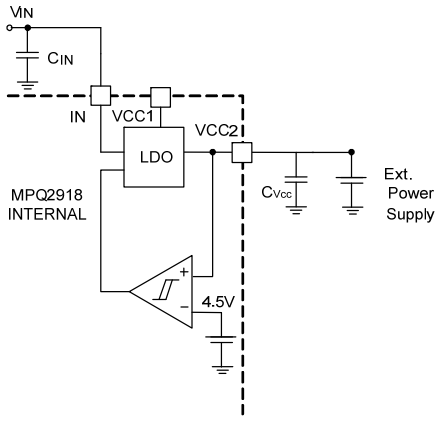

Figure 6: Internal Circuitry of VCC2

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If V_{OUT} is higher than 4.7V but less than 12V, VCC2 can be connected to V_{OUT} directly (see Figure 7).

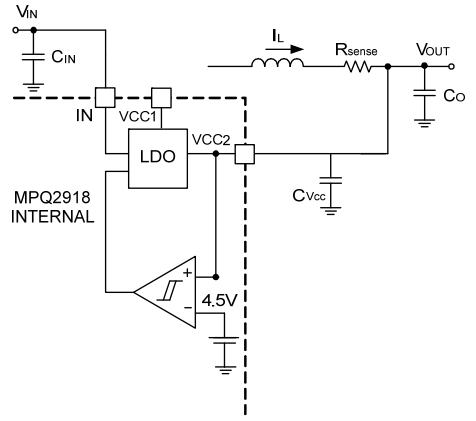

Figure 7: Configuration of VCC2 Connecting to V_{OUT}

Selecting the Inductor

An inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, the larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current. Choose the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (7):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S} \quad (7)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the 300kHz switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

The maximum inductor peak current can be calculated with Equation (8):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (8)$$

Where I_{LOAD} is the load current.

Selecting the Input Capacitor

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The selection of the input capacitor is based mainly on its maximum ripple current capability. The RMS value of the ripple current flowing through the input capacitor can be calculated with Equation (9):

$$I_{RMS} = I_{LOAD} \sqrt{\frac{V_{OUT}}{V_{IN}} (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (10):

$$I_{RMS} = I_{LOAD}/2 \quad (10)$$

The input capacitor must be capable of handling this ripple current.

Output Capacitor Selection

The output capacitor impedance should be low at the switching frequency. The output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right) \quad (11)$$

Where C_O is the output capacitance value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For tantalum or electrolytic capacitor applications, the ESR dominates the impedance at the switching frequency. The output voltage ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

Power MOSFET Selection

Two N-channel MOSFETs must be selected for the controller: one for the high-side switch, and one for the low-side switch.

The driver level of the HS-FET and LS-FET is 5V, so the threshold voltage (V_{th}) of the selected MOSFETs must be no higher than this value.

The input voltage (V_{DS}), continuous drain current (I_D), on resistance ($R_{DS(ON)}$), total gate charge (Qg), and thermal-related parameters should be considered when choosing the power MOSFETs.

V_{DS} of the chosen MOSFETs should exceed the maximum applied voltage between the drain and source in the application, which is $V_{IN(MAX)}$ plus additional rings on the switch node.

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The MOSFET's power dissipations can be calculated with Equation (13) and Equation (14):

$$P_{HS}=I_{OUT}^{2}\times R_{ON\text{-}HS}\times\frac{V_{OUT}}{V_{IN}}+\frac{1}{2}\times V_{IN}\times I_{OUT}\times(t_r+t_f)\times f_{SW}+Q_{g\text{-}HS}\times f_{SW}\times V_{driver} \quad (13)$$

$$P_{LS}=I_{OUT}^{2}\times R_{ON\text{-}LS}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)+Q_{g\text{-}LS}\times f_{SW}\times V_{driver}+V_{DROP}\times I_{OUT}\times(t_{dead1}+t_{dead2})\times f_{SW} \quad (14)$$

Where $R_{ON\text{-}HS}$ and $R_{ON\text{-}LS}$ are the on resistance of the HS-FET and LS-FET, t_r and t_f are the rising and falling time of the switch, $Q_{g\text{-}HS}$ and $Q_{g\text{-}LS}$ are the total gate charge of the HS-FET and LS-FET, V_{driver} is the gate driver voltage (which is provided by VCC1), V_{DROP} is the LS-FET body diode forward voltage, t_{dead1} is the dead time between the HS-FET turning off and the LS-FET turning on, and t_{dead2} is the dead time between the LS-FET turning off and the HS-FET turning on.

Ensure that the thermal caused by the power loss on the MOSFETs does not exceed the allowed maximum thermal of the selected MOSFETs.

Schottky Selection

The diode between SW and PGND (shown as D2 in Figure 12) is used to absorb spikes, store charges during dead time, and protect the body diode of the LS-FET. Considering the size and power loss during the dead time, a 1 - 3A Schottky diode is recommended.

BST Charge Diode and Resistor Selection

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC1 or V_{OUT} is recommended to be this power supply in the circuit (see Figure 8).

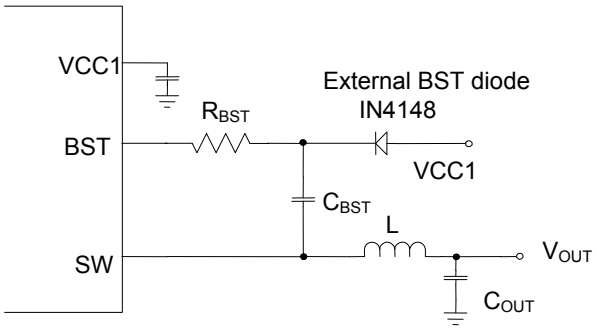

Figure 8: External Bootstrap Diode and Resistor

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1µF to 1µF.

A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at a high V_{IN}. A higher resistance is better for SW spike reduction but compromises efficiency. To make a tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

Compensation Components

The MPQ2918 employs current-mode control for easy compensation and fast transient response. COMP is the output of the internal error amplifier and controls system stability and transient response. A series resistor-capacitor (R-C) combination sets a pole zero combination to control the control system's characteristics (see Figure 9). The DC gain of the voltage feedback loop can be calculated with Equation (15):

$$A_{VDC}=R_{LOAD}\times G_{CS}\times A_O\times\frac{V_{FB}}{V_{OUT}} \quad (15)$$

Where A_O is the error amplifier voltage gain (3000V/V), G_{CS} is the current sense transconductance 1/(12xR_{SENSE}) (A/V), and R_{LOAD} is the load resistor value.

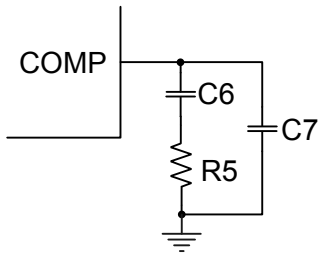

Figure 9: Compensation Network

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The system has two important poles: one from the compensation capacitor (C6) and the output resistor of the error amplifier, and the other from the output capacitor and the load resistor (see Figure 9). These poles can be calculated with Equation (16) and Equation (17):

$$f_{P1} = \frac{G_m}{2\pi \times C6 \times A_O} \quad (16)$$

$$f_{P2} = \frac{1}{2\pi \times Co \times R_{LOAD}} \quad (17)$$

Where G_m is the error amplifier transconductance (500μA/V), and Co is the output capacitor.

The system has one important zero due to the compensation capacitor and the compensation resistor (R5), which can be calculated with Equation (18):

$$f_{Z1} = \frac{1}{2\pi \times C6 \times R5} \quad (18)$$

The system may have another significant zero if the output capacitor has a large capacitance or high ESR value and can be calculated with Equation (19):

$$f_{ESR} = \frac{1}{2\pi \times Co \times R_{ESR}} \quad (19)$$

In this case, a third pole set by the compensation capacitor (C7) and the compensation resistor can compensate for the effect of the ESR zero. This pole is calculated with Equation (20):

$$f_{P3} = \frac{1}{2\pi \times C7 \times R5} \quad (20)$$

The goal of the compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important, since lower crossover frequencies result in slower line and load transient responses, and higher crossover frequencies lead to system instability. Set the crossover frequency to ~0.1 x f_{SW}.

Follow the steps below to design the compensation.

1. Choose R5 to set the desired crossover frequency with Equation (21):

$$R5 = \frac{2\pi \times Co \times f_C}{G_m \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (21)$$

   Where f_C is the desired crossover frequency.

2. Choose C6 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero (f_{Z1}) <0.25 x f_C to provide a sufficient phase margin. C6 is then calculated with Equation (22):

$$C6 > \frac{4}{2\pi \times R5 \times f_C} \quad (22)$$

3. C7 is required if the ESR zero of the output capacitor is located at <0.5 x f_{SW}, or Equation (23) is valid:

$$\frac{1}{2\pi \times Co \times R_{ESR}} < \frac{f_{SW}}{2} \quad (23)$$

   If this is the case, use C7 to set the pole (f_{P3}) at the location of the ESR zero. Determine C7 with Equation (24):

$$C7 = \frac{Co \times R_{ESR}}{R5} \quad (24)$$

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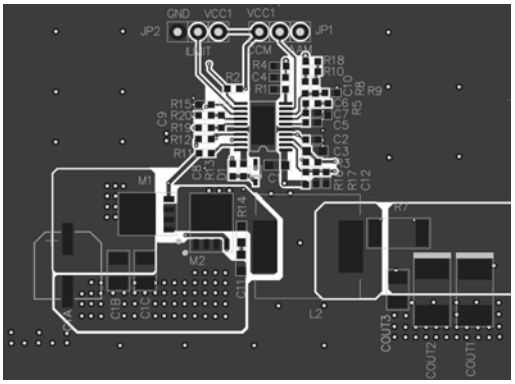
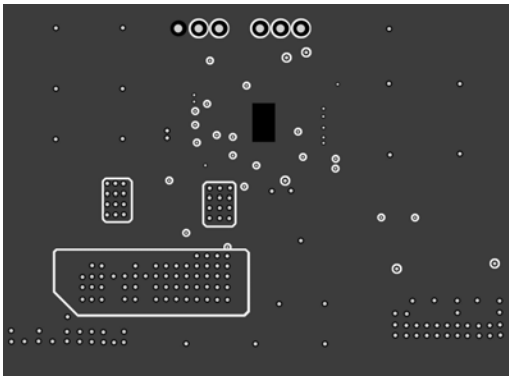
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, especially for the input capacitor placement. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 10 and Figure 11 and follow the guidelines below.

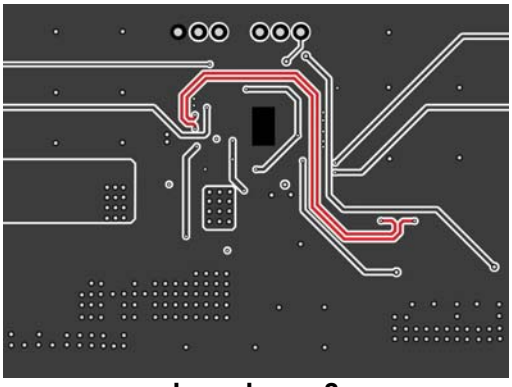
1. Place the MOSFETs as close as possible to the device.
2. Make the sense lines (the red lines in Inner Layer 2 of Figure 10 and Figure 11) run close together using a Kelvin connection to reduce the line drop error.
3. Use a large ground plane to connect to PGND directly.
4. Add vias near PGND if the bottom layer is a ground plane.
5. Ensure that the high-current paths at PGND and V_{IN} have short, direct, and wide traces.
6. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to IN and PGND as possible to minimize high-frequency noise.
7. Keep the connection of the input capacitor and IN as short and wide as possible.
8. Place the VCC1 capacitor as close to VCC1 and SGND as possible.
9. Route SW and BST away from sensitive analog areas such as FB.
10. Place the feedback resistors close to the chip to ensure that the trace which connects to FB is as short as possible.
11. Use multiple vias to connect the power planes to the internal layers.



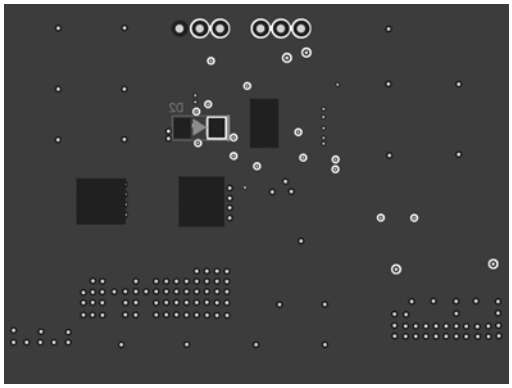
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 10: Recommended PCB Layout for TSSOP Package (6)

NOTE:

6) The recommended PCB layout is based on Figure 12.

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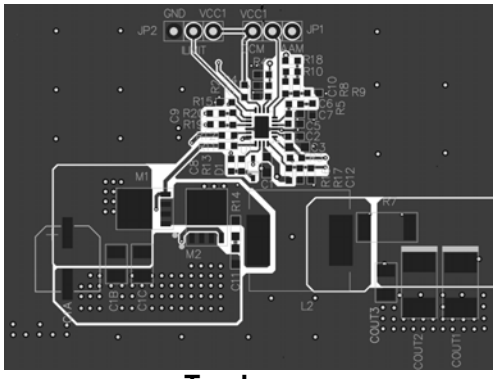
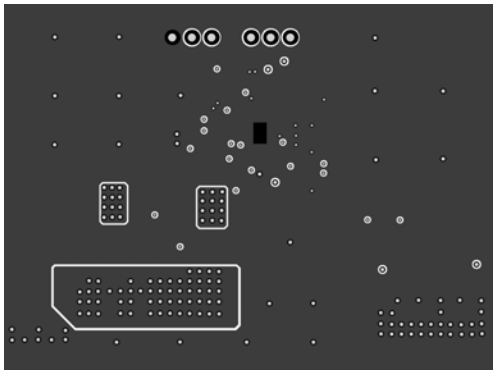
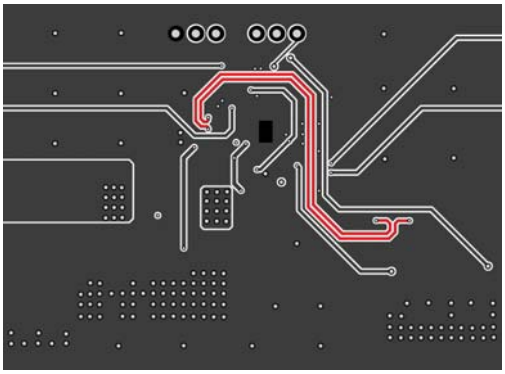


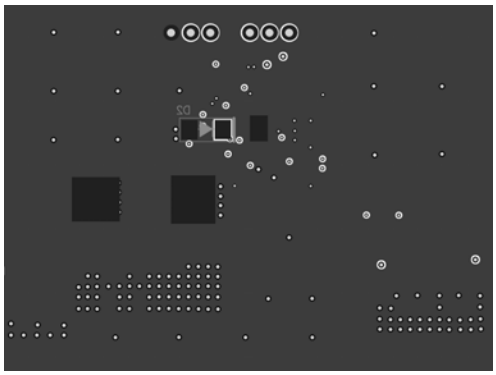
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout for QFN Package (7)

NOTE:

7) The recommended PCB layout is based on Figure 14.

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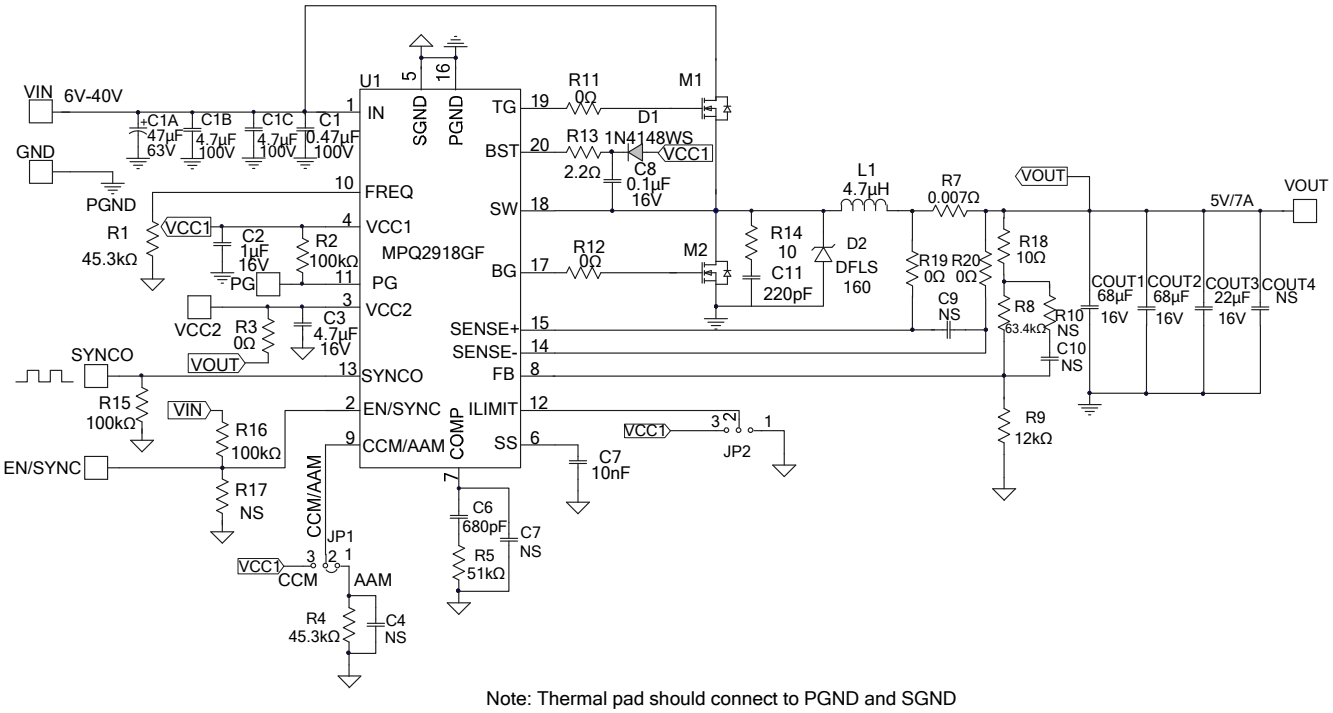
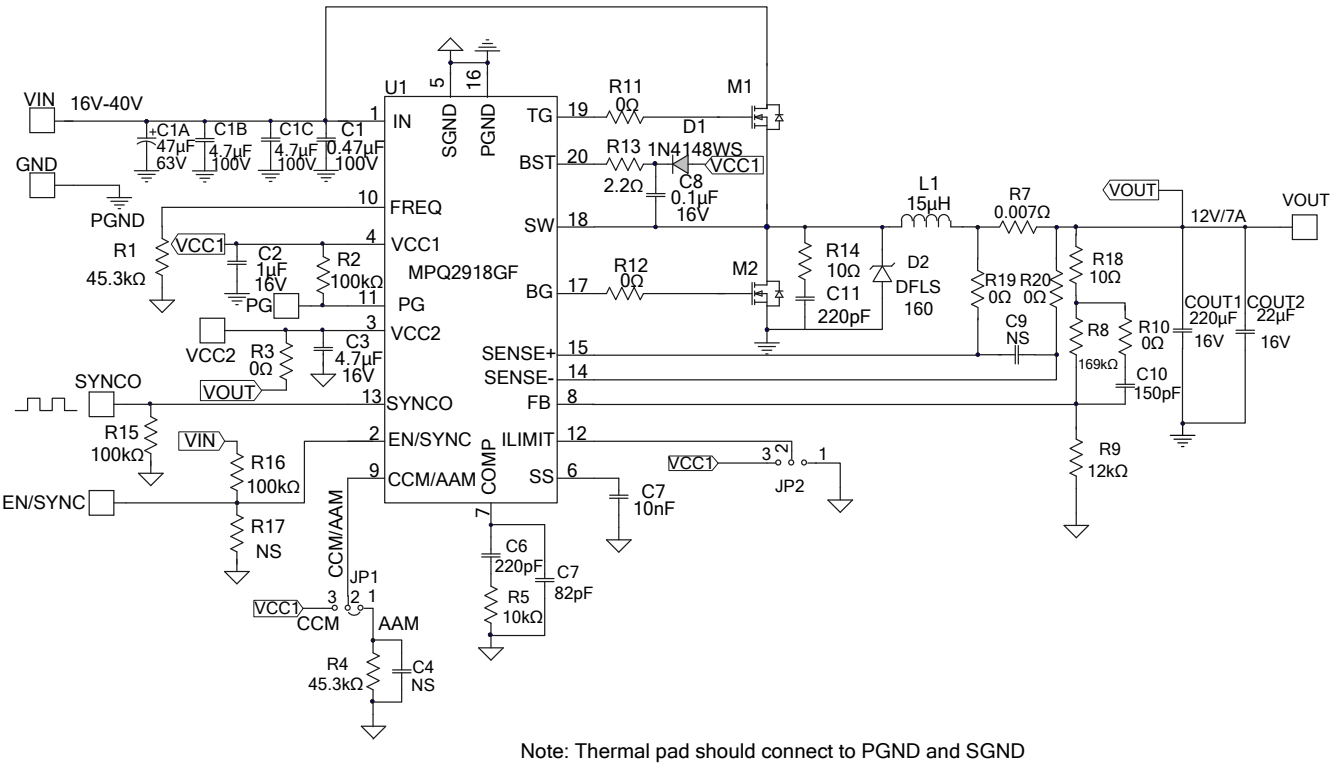
TYPICAL APPLICATION CIRCUITS



Note: Thermal pad should connect to PGND and SGND

Figure 12: 5V Output Application Circuit for TSSOP Package



Note: Thermal pad should connect to PGND and SGND

Figure 13: 12V Output Application Circuit for TSSOP Package

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TYPICAL APPLICATION CIRCUITS *(continued)*

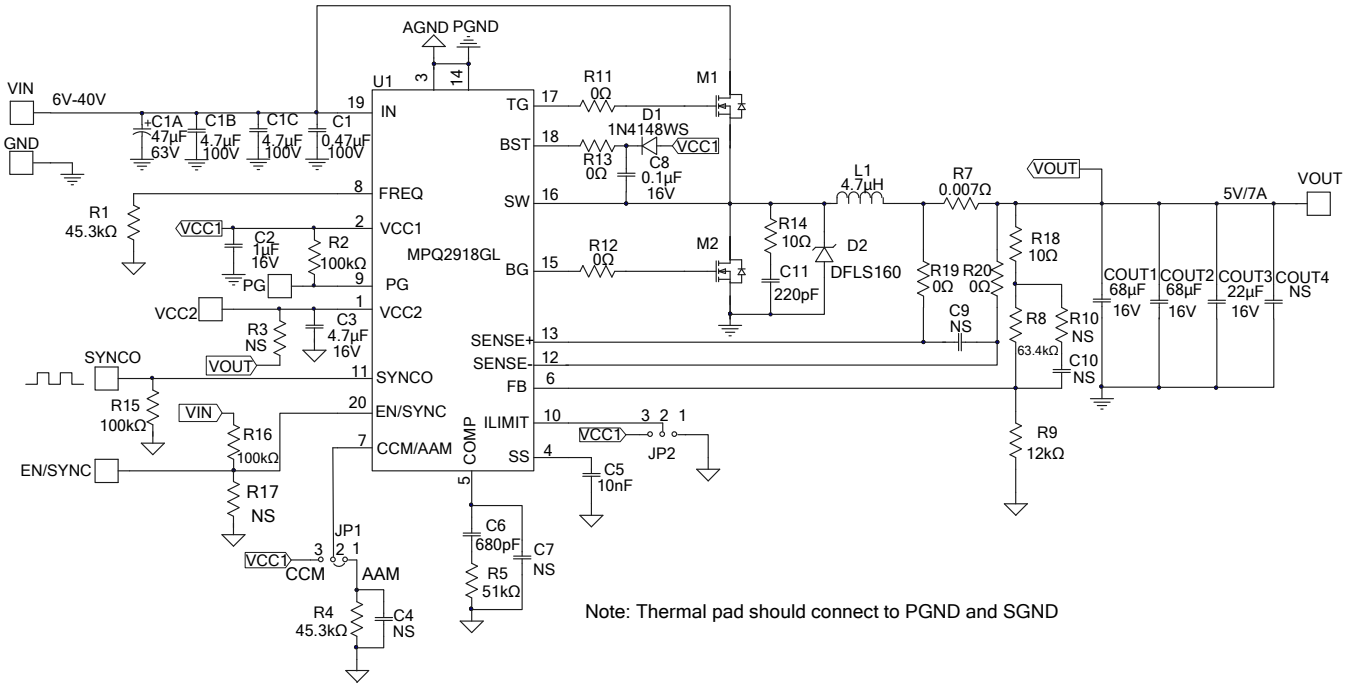

Figure 14: 5V Output Application Circuit for QFN Package

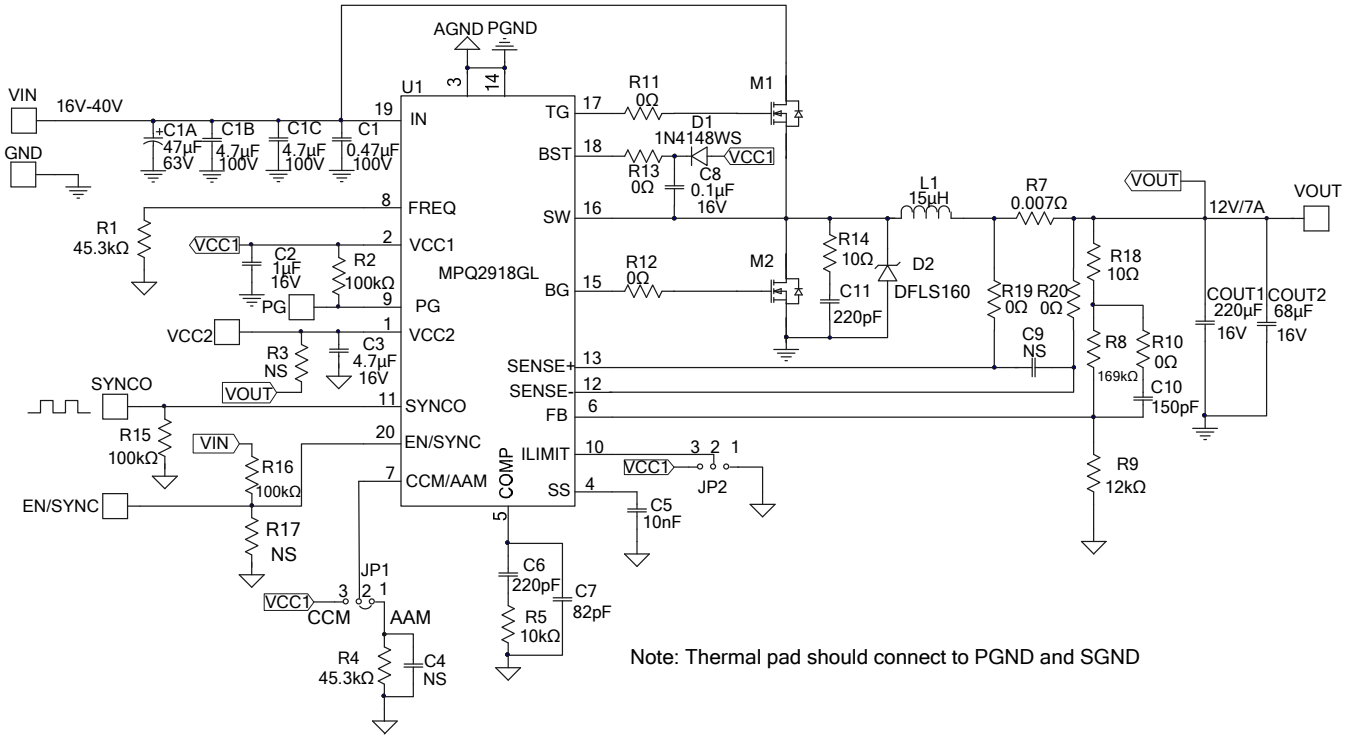

Figure 15: 12V Output Application Circuit for QFN Package

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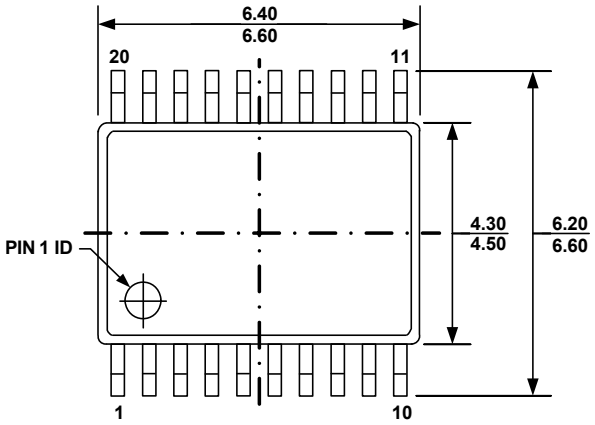
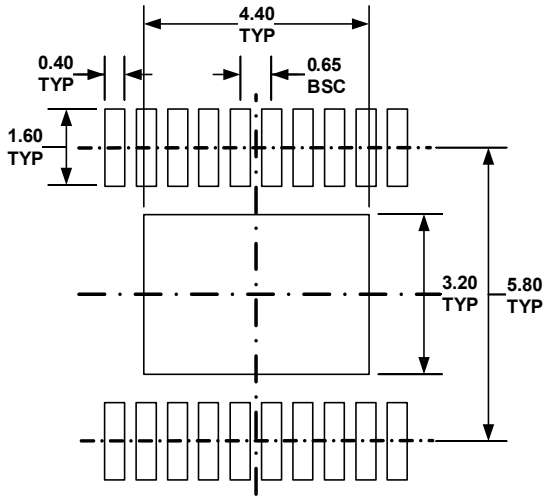
PACKAGE INFORMATION

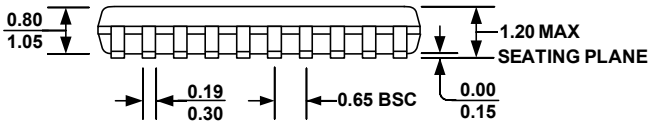
TSSOP-20 EP



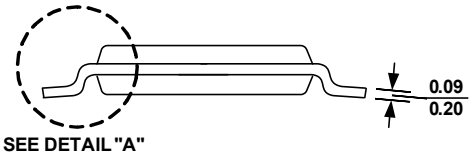
TOP VIEW



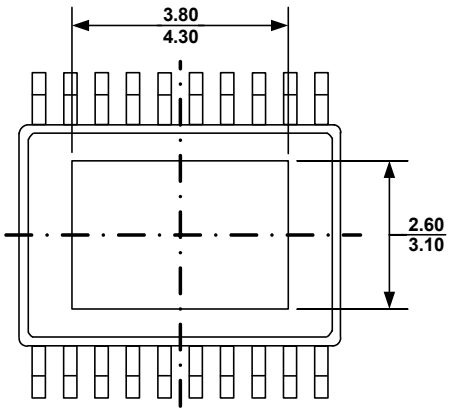
RECOMMENDED LAND PATTERN



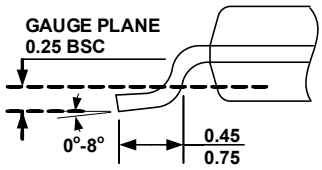
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE

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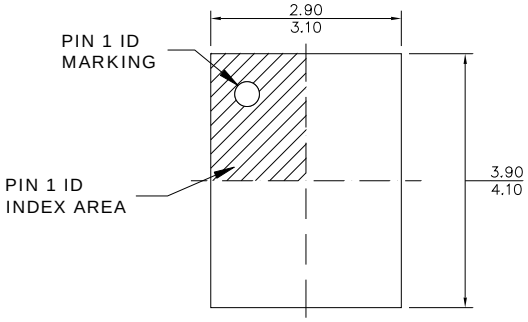
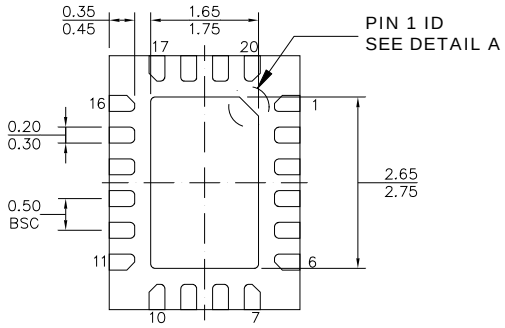
PACKAGE INFORMATION *(continued)*

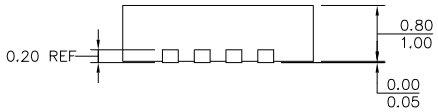
QFN-20 (3mmx4mm)
Non-Wettable Flank



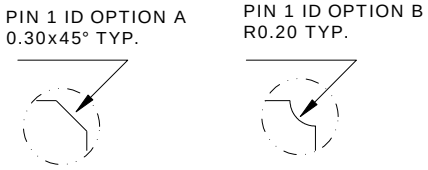
TOP VIEW



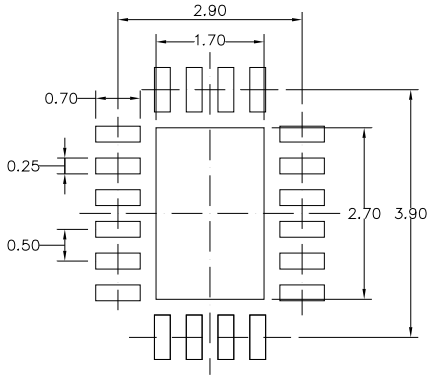
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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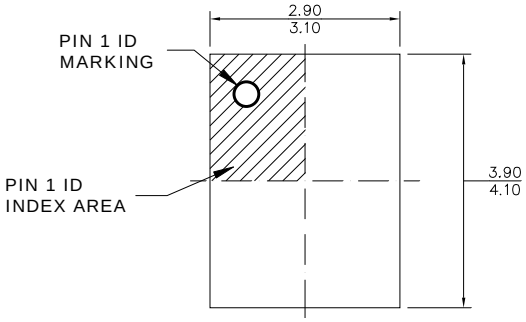
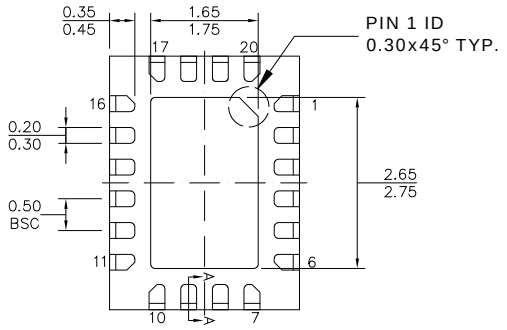
PACKAGE INFORMATION *(continued)*

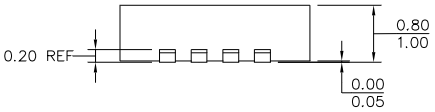
QFN-20 (3mmx4mm)
Wettable Flank



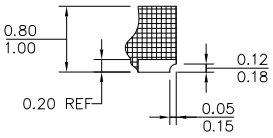
TOP VIEW



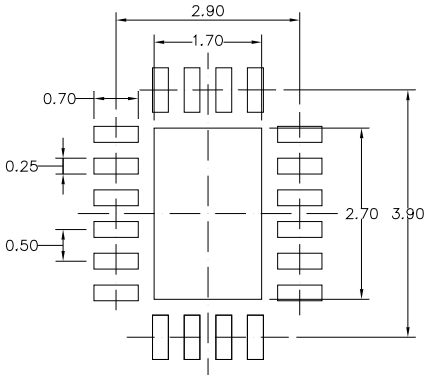
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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