

Phase Control Thyristors

Features

1. 800PT series Thyristors are designed for various power controls
2. Voltage rating up to 1600V
3. Typical application
 - DC motor control
 - Controlled DC power supplies
 - AC controllers

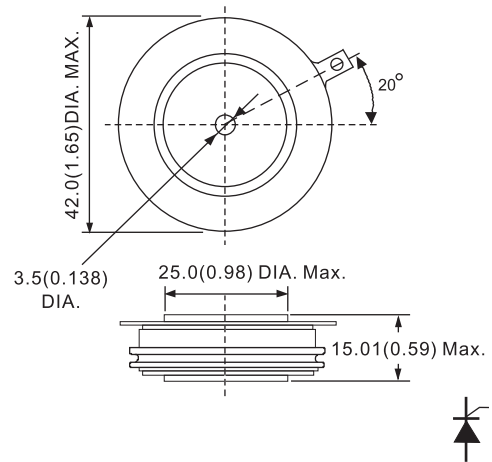
Ordering code

800	PT	xx	B	0
(1)	(2)	(3)	(4)	(5)

- (1) Maximum average on-state current , A
 (2) For Phase Control Thyristor
 (3) Voltage code , code x 100 = V_{RRM} / V_{DRM}
 (4) package style : A , B , C , D ,E for Disc Type
 (5) Terminal types
 0 - for eyelet

Electrical Characteristics

B TYPE



All dimensions in millimeters (inches)

Symbol	Parameter	Condition	Value			Unit
			Min.	Type	Max.	
$I_T(AV)$	Mean on-state current	180° half sine wave , 50Hz Double side cooled , $T_C = 55^\circ C$			800	A
$I_T(RMS)$	Max. RMS on-state current	Double side cooled , $T_{hs}=55^\circ C$			1270	A
V_{RRM} V_{DRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM} & V_{RRM} $t_p=10ms$ V_{DsM} & $V_{RsM} = V_{DRM}$ & $V_{RRM} + 100V$	1100		1800	V
I_{TSM}	Surge on-state current	10 ms half sine wave			10	KA
I_t^2	For fusing coordination	$V_R = 0.6V_{RRM}$			500	$A^2s \cdot 10^3$
$V_T(TO)$	Threshold voltage				0.91	V
r_t	On-state slope resistance				0.35	mΩ
V_{TM}	Max. Forward voltage drop	$I_{TM}=900A$, $F=8.0KN$			2.2	V
I_H	Holding current	$V_A=12V$, $I_A=1A$	20		250	mA
di/dt	Cirtical rate of rise of turned-on current	Gate drive 20V , 20 Ω , $t_r \leq 0.5 \mu s$			100	A/μs
t_q	Typical turn-off time	$di_{RR}/dt=-10 A/\mu s$			100	μs
d_v/dt	Cirtical rate of rise of off-state voltage	$V_{DM}=0.67 V_{DRM}$			300	V/μs
I_{RRM} I_{DRM}	Repetitive peak reverse current	$V_R = V_{RRM}$ $V_D = V_{DRM}$			50	mA
P_G	Max. average gate power	Square wavepulse width 100 μs			2	W
P_{GM}	Max. peak gate power square				10	W
I_{GT}	Gate trigger current	$V_A=12V$, $I_A=1A$	40		300	mA
V_{GT}	Gate trigger voltage		0.8		3	V
V_{GD}	DC voltage not to trigger	At 67% V_{DRM} , $T_j=T_j \text{ max.}$			0.30	V
I_{FGM}	Max. peak positive gate current	$T_j=T_j \text{ max.}$ $t_p \leq 3s$			3	A
V_{FGM}	Max. peak positive gate voltage				16	V
V_{RGM}	Max. peak negative gate voltage				5	V
T_j	Max.operating temperaturerange		- 40		125	°C
T_{stg}	Storage temperature		- 40		140	°C
$R_{th(j-h)}$	Thermal resistance(junction to heatsink)	Double side cooled , clamping force 8.0 KN			0.032	°C/ W
F_m	Mounting force		5.3		10	KN
W_t	Approximate weight			80		g

Fig. 1

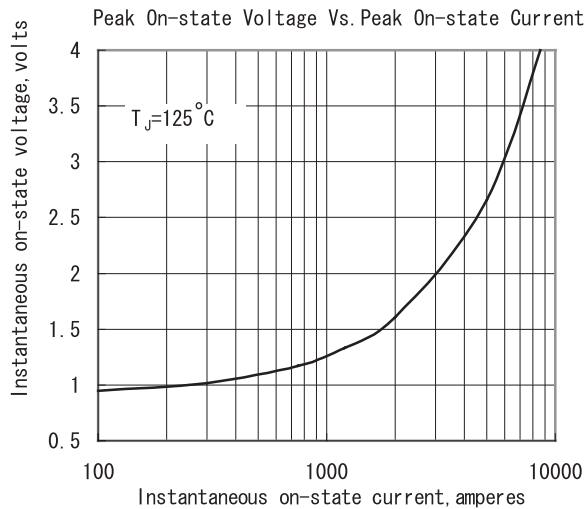


Fig. 2

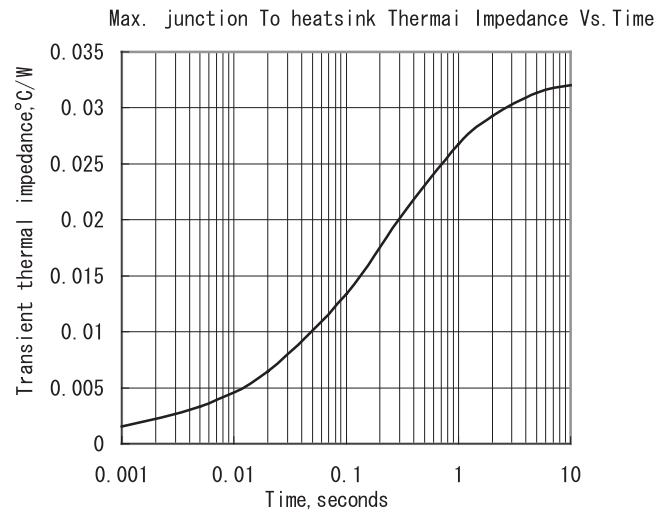


Fig. 3

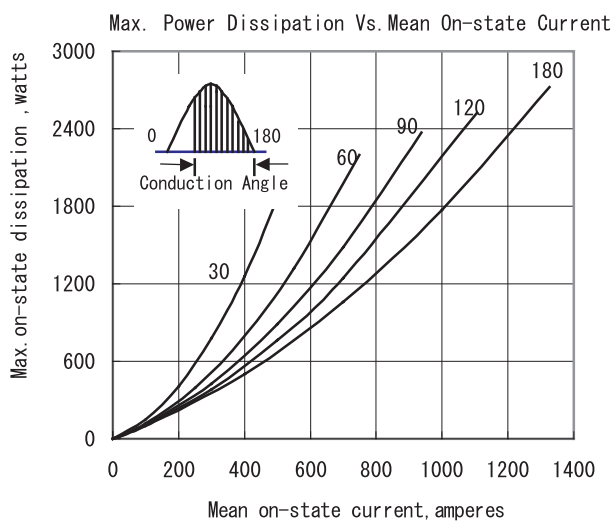


Fig. 4

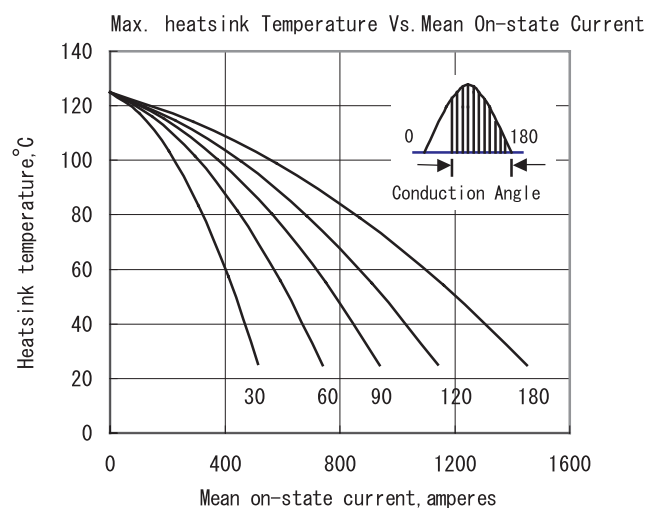


Fig. 5

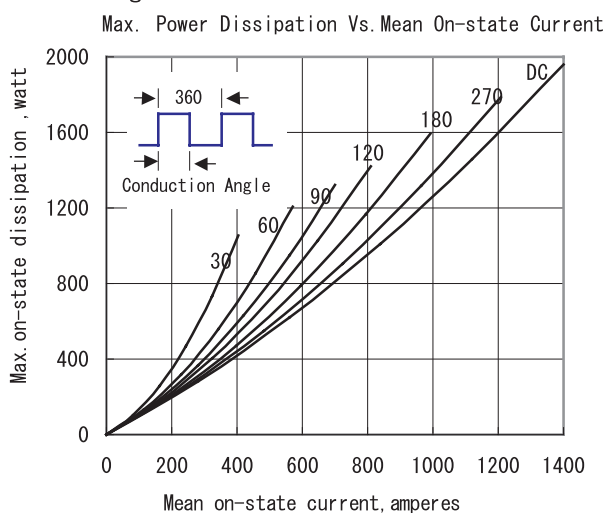


Fig. 6

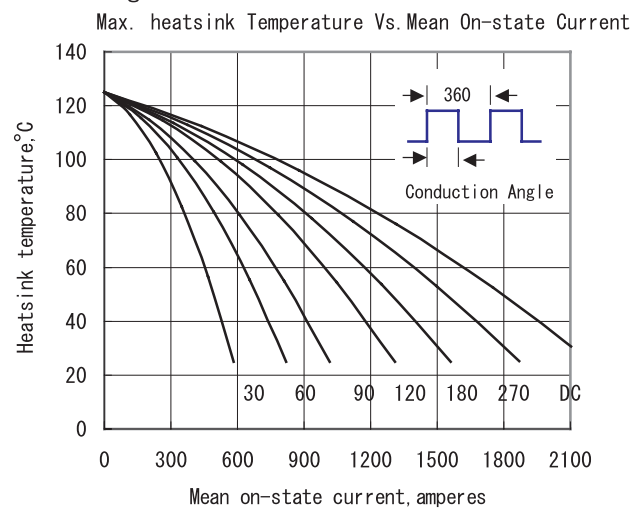


Fig. 7

Surge Current Vs. Cycles

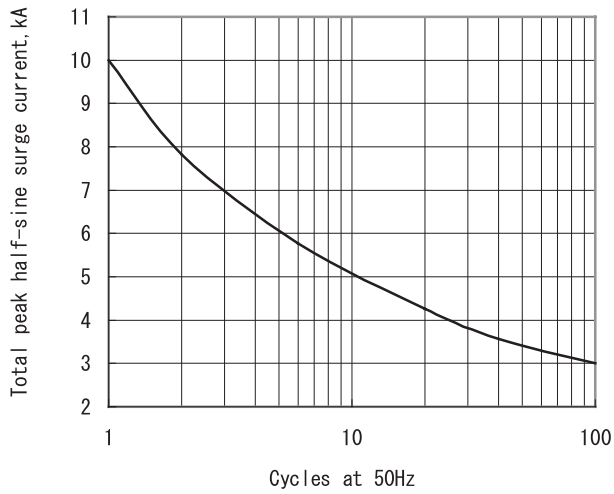


Fig. 8

I^2t Vs. Time

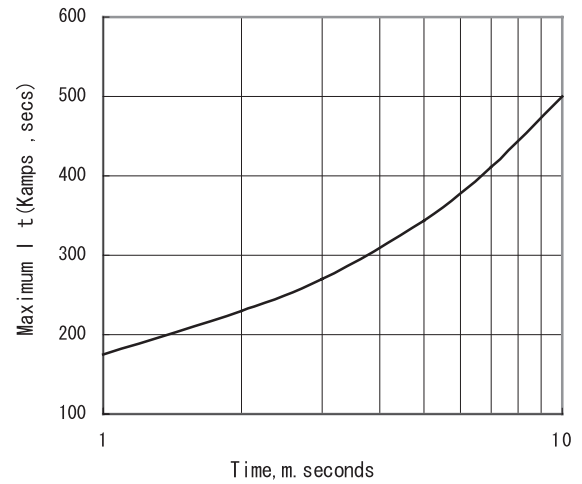


Fig. 9

Gate characteristic at 25°C junction temperature

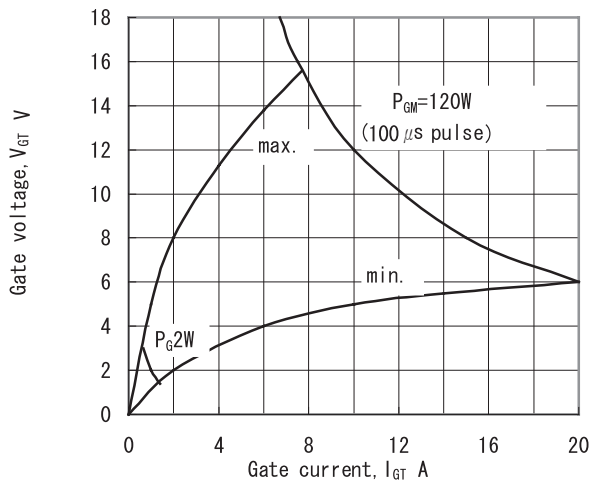


Fig. 10

Gate Trigger Zone at varies temperature

