SONY

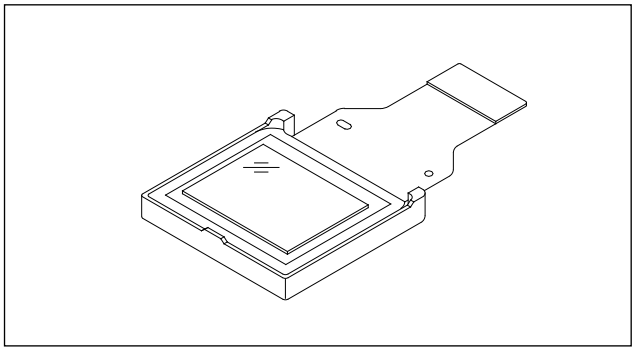
LCX005BK

1.4cm (0.55-inch) NTSC/PAL Color LCD Panel

For the availability of this product, please contact the sales office.

Description

The LCX005BK is a 1.4cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel provides full-color representation in NTSC/PAL mode. RGB dots are arranged in a delta pattern featuring high picture quality of no fixed color patterns, which is inherent in vertical stripes and mosaic pattern arrangements.



Features

- The number of active dots: 113,578 (0.55-inch; 1.397cm in diagonal)
- Horizontal resolution: 260 TV lines
- High optical transmittance: 3.4% (typ.)
- High contrast ratio with normally white mode: 270 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, TTL drive possible)
- High quality picture representation with RGB delta arranged color filters
- Full-color representation
- NTSC/PAL compatible
- Right/left inverse display function

Element Structure

- Dots

  Total dots : 537 (H) × 222 (V) = 119,214

  Active dots: 521 (H) × 218 (V) = 113,578

- Built-in peripheral driver using polycrystalline silicon super thin film transistors.

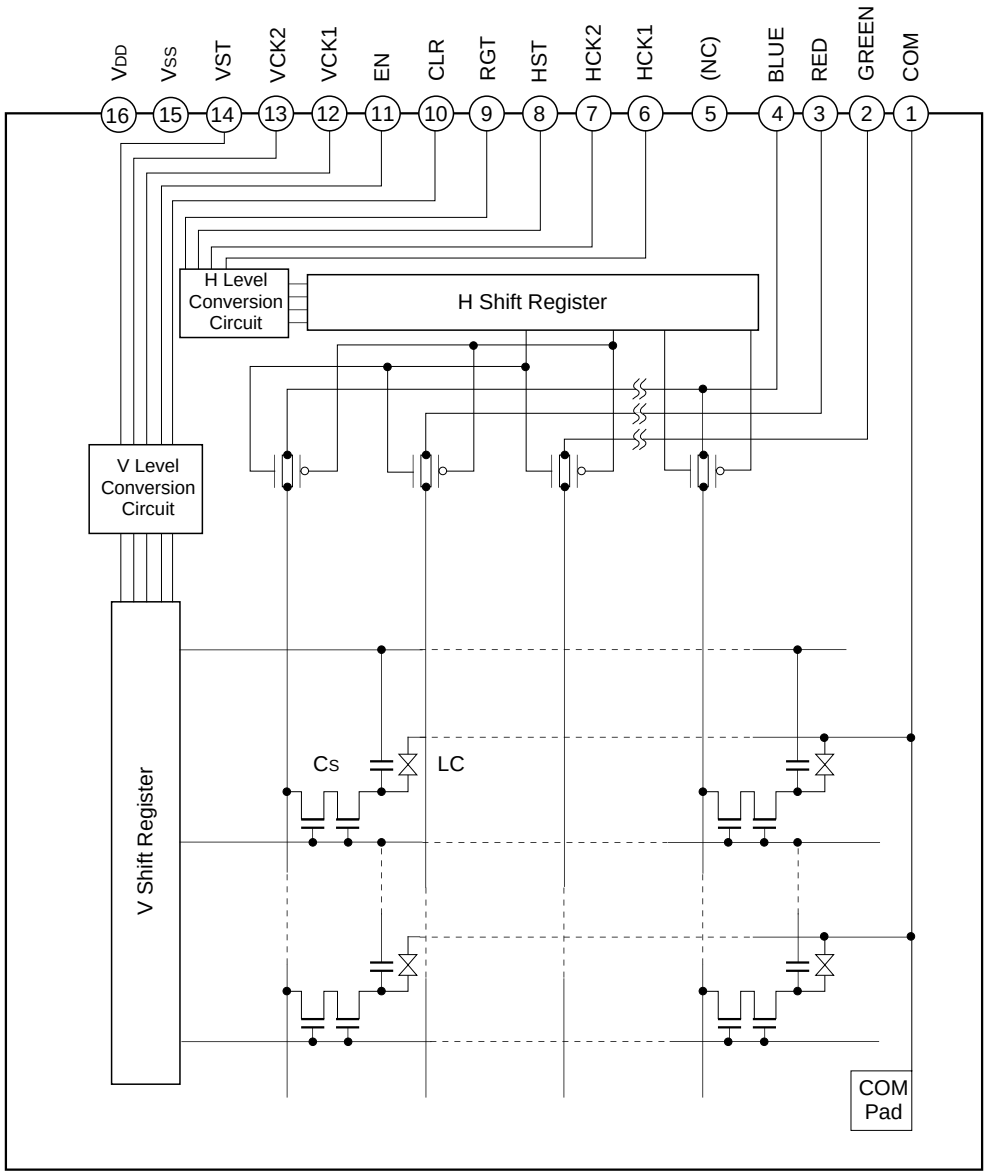
Applications

- Viewfinders
- Super compact liquid crystal monitors etc.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

E94Z24A5X-PS

Block Diagram



Absolute Maximum Ratings (V_{SS} = 0V)

• H and V driver supply voltages	V_{DD}	–1.0 to +17	V
• H driver input pin voltage	HST, HCK1, HCK2 RGT	–1.0 to +17	V
• V driver input pin voltage	VST, VCK1, VCK2 CLR, EN	–1.0 to +17	V
• Video signal input pin voltage	GREEN, RED, BLUE	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (V_{SS} = 0V)

Supply voltage

V_{DD} 13.5 ± 0.5 V

Input pulse voltage (Vp-p of all input pins except video signal input pins)

Vin 2.8V (more than)

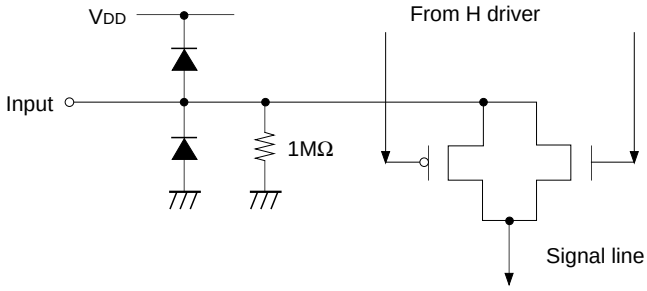
Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	COM	Common voltage of panel	9	RGT	Drive direction pulse for H shift register (H: normal, L: reverse)
2	GREEN	Video signal (G) to panel	10	CLR	Improvement pulse for uniformity
3	RED	Video signal (R) to panel	11	EN	Enable pulse for gate selection
4	BLUE	Video signal (B) to panel	12	VCK1	Clock pulse for V shift register drive
(5)	(NC)	Not connected	13	VCK2	Clock pulse for V shift register drive
6	HCK1	Clock pulse for H shift register drive	14	VST	Start pulse for V shift register drive
7	HCK2	Clock pulse for H shift register drive	15	Vss	GND (H, V drivers)
8	HST	Start pulse for H shift register drive	16	V_{DD}	Power supply for H and V drivers

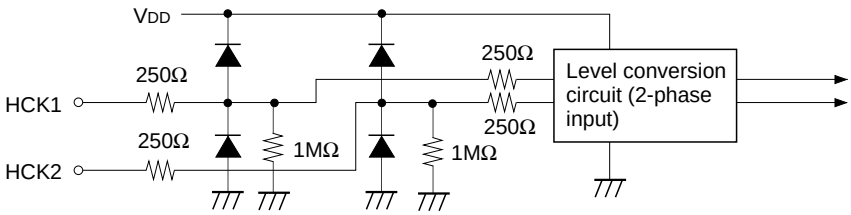
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supply. In addition, protective resistors are added to all pins except video signal input. All pins are connected to Vss with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (The resistor value: typ.)

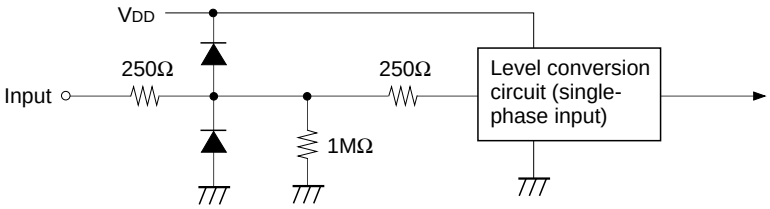
(1) Video signal input



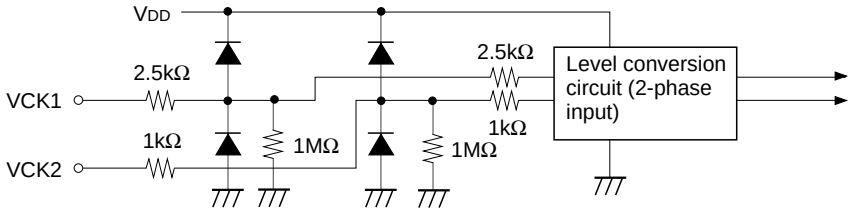
(2) HCK1, HCK2



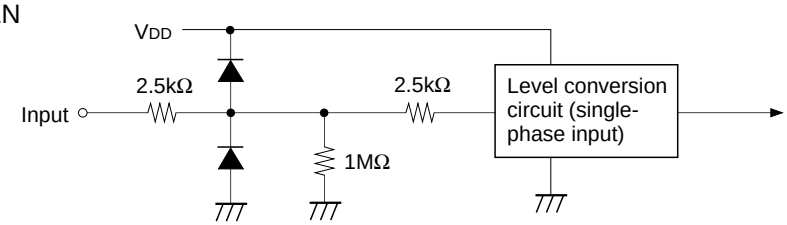
(3) HST



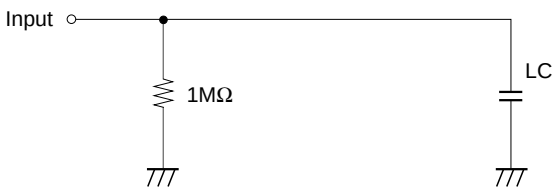
(4) VCK1, VCK2



(5) RGT, VST, CLR, EN



(6) COM



Level Conversion Circuit

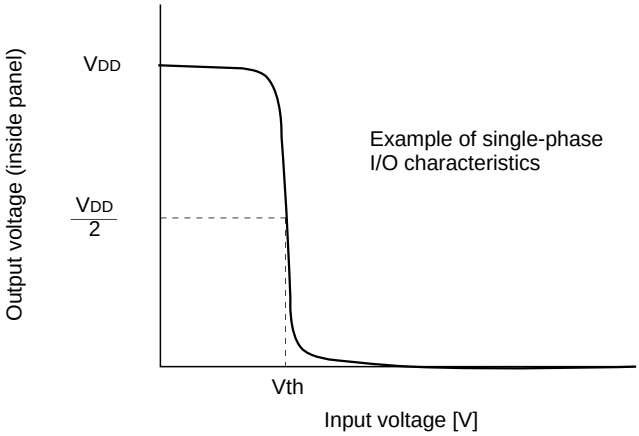
The LCX005BK has a built-in level conversion circuit in the clock input unit located inside the panel. The circuit voltage is stepped up to V_{DD} inside the panel. This level conversion circuit meets the specifications of a 3.0V to 5.0V power supply of the externally-driven IC.

1. I/O characteristics of level conversion circuit

(For a single-phase input unit)

An example of the I/O voltage characteristics of a level conversion circuit is shown in the figure to the right. The input voltage value that becomes half the output voltage (after voltage conversion) is defined as Vth.

The Vth value varies depending on the V_{DD} voltage. The Vth values under standard conditions are indicated in the table below. (HST, VST, EN, CLR, and RGT in the case of a single-phase input)

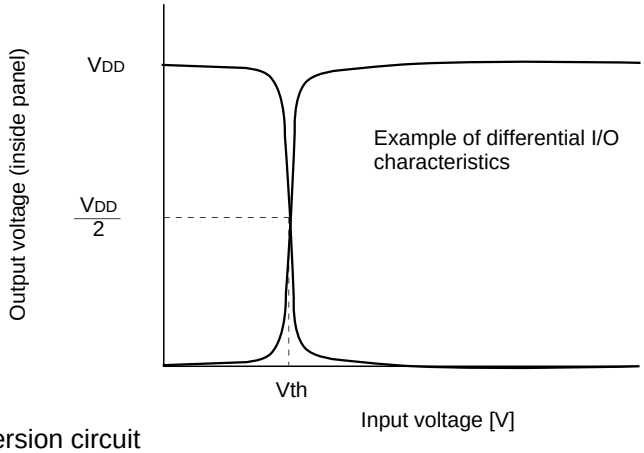


V_{DD} = 13.5V

Item	Symbol	Min.	Typ.	Max.	Unit
Vth voltage of circuit	Vth	0.4	1.50	2.75	V

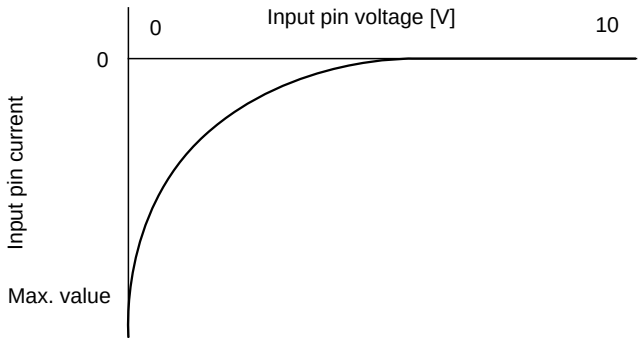
(For a differential input unit)

An example of I/O voltage characteristics of a level conversion circuit for a differential input is shown in the figure to the right. Although the characteristics, including those of the Vth voltage, are basically the same as those for a single-phased input, the two-phased input phase is defined. (Refer to clock timing conditions.)

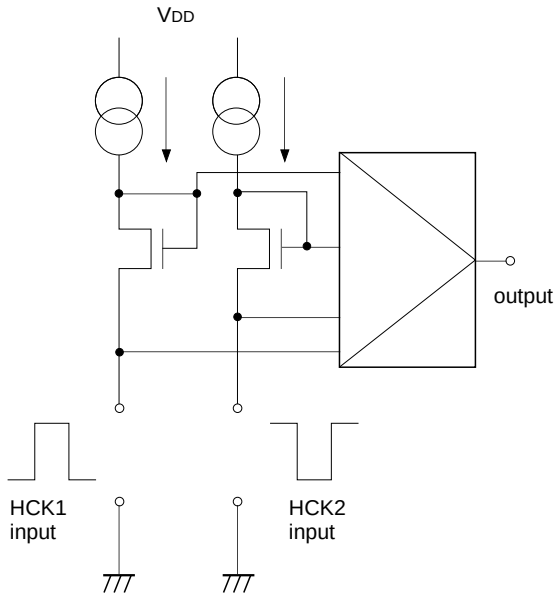


2. Current characteristics at the input pin of level conversion circuit

A slight pull-in current is generated at the input pin of the level conversion circuit. (The equivalent circuit is shown to the right.) The current volume increases as the voltage at the input pin decreases, and is maximized when the pin is grounded. (Refer to electrical characteristics.)



Pull-in current characteristics at the input pin



Level conversion equivalent circuit

Input Signals

1. Input signal voltage conditions (V_{SS} = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
H driver input voltage (HST, HCK1, HCK2, RGT)	(Low)	VHIL	–0.35	0.0	+0.35	V
	(High)	VHIH	2.8	5.0	5.5	V
V driver input voltage (VST, VCK1, VCK2, CLR, EN)	(Low)	VVIL	–0.35	0.0	+0.35	V
	(High)	VVIH	2.8	5.0	5.5	V
Video signal center voltage		VVC	5.8	6.0	6.2	V
Video signal input range*1		Vsig	VVC – 4.5		VVC + 4.5	V
Common voltage of panel		VCOM	VVC – 0.55	VVC – 0.40	VVC – 0.25	V

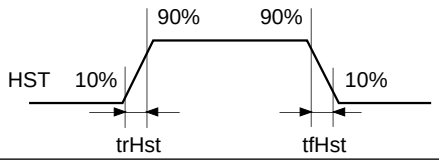
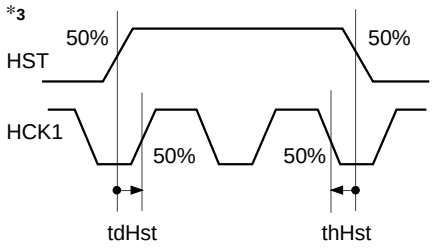
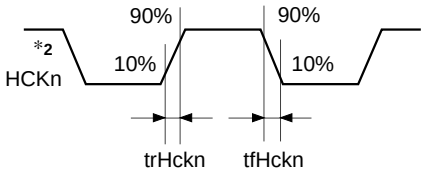
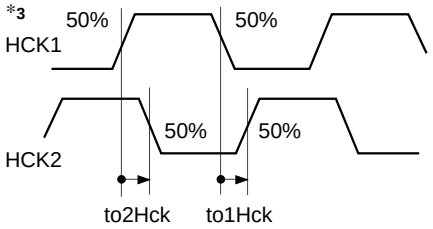
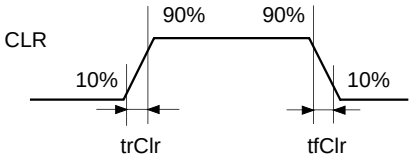
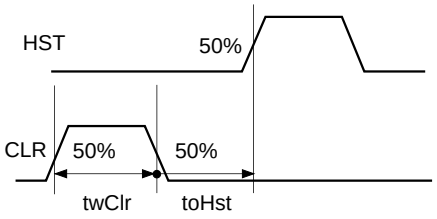
*1 Video input signal shall be symmetrical to VVC.

2. Clock timing conditions (Ta = 25°C, Input voltage = 5.0V)

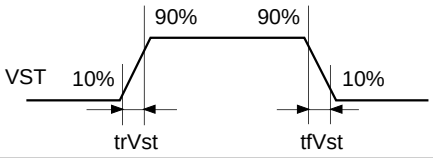
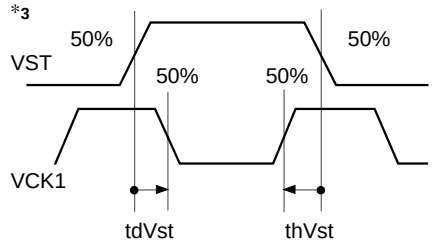
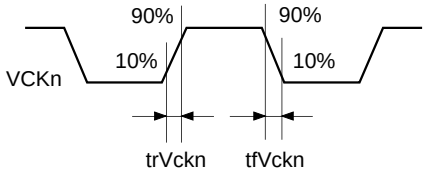
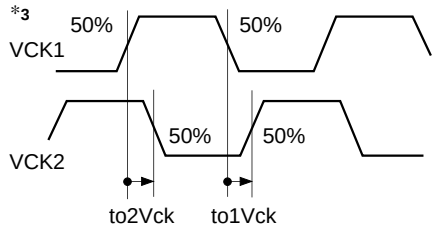
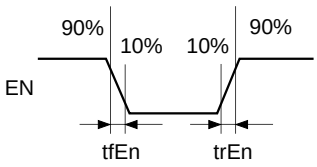
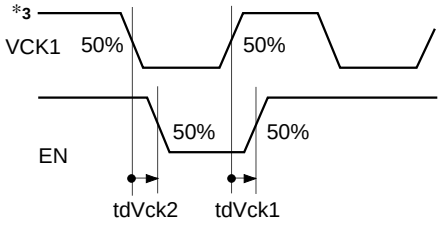
	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst			100	ns
	Hst fall time	tfHst			100	
	Hst data set-up time	tdHst	–170	135	170	
	Hst data hold time	thHst	–455	–135	–50	
HCK	Hckn*2 rise time	trHckn			100	
	Hckn*2 fall time	tfHckn			100	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
CLR	Clr rise time	trClr			100	
	Clr fall time	tfClr			100	
	Clr pulse width	twClr	3400	3500	3600	
	Clr fall to Hst rise time	toHst	1100	1200	1300	
VST	Vst rise time	trVst			100	
	Vst fall time	tfVst			100	
	Vst data set-up time	tdVst	–50	32	50	µs
	Vst data hold time	thVst	–50	–32	–20	
VCK	Vckn*2 rise time	trVckn			100	ns
	Vckn*2 fall time	tfVckn			100	
	Vck1 fall to Vck2 rise time	to1Vck	–100	0	100	
	Vck1 rise to Vck2 fall time	to2Vck	–100	0	100	
EN	En rise time	trEn			100	
	En fall time	tfEn			100	
	Vck2 rise to En fall time	tdVck2	–100	0	100	
	Vck1 rise to En rise time	tdVck1	–100	0	100	

*2 Hckn and Vckn mean Hck1, Hck2 and Vck1, Vck2. (fHckn = 1.84MHz, fVckn = 7.865kHz)

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		◯ HCKn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		◯ HCKn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn*2 rise time	trHckn		◯ HCKn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns tdHst = 135ns thHst = –135ns
	Hckn*2 fall time	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		◯ tdHst = 135ns thHst = –135ns
	Hck1 rise to Hck2 fall time	to2Hck		
CLR	Clr rise time	trClr		◯ HCKn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Clr fall time	tfClr		
	Clr pulse width	twClr		◯ HCKn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Clr fall to Hst rise time	toHst		

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		◯ VCKn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		◯ VCKn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	Vst data hold time	thVst		
VCK	Vckn*2 rise time	trVckn		◯ VCKn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns tdVst = 32µs thVst = –32µs
	Vckn*2 fall time	tfVckn		
	Vck1 fall to Vck2 rise time	to1Vck		◯ tdVst = 32µs thVst = –32µs
	Vck1 rise to Vck2 fall time	to2Vck		
EN	En rise time	trEn		◯ VCKn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	En fall time	tfEn		
	Vck1 rise to En rise time	tdVck1		◯ VCKn*2 duty cycle 50% to1Vck = 0ns to2Vck = 0ns
	Vck2 rise to En fall time	tdVck2		

*3 Definitions: The right-pointing arrow (•→) means +.
The left-pointing arrow (←•) means –.
The black dot at an arrow (•) indicates the start of measurement.

Electrical Characteristics

1. Horizontal drivers (Ta = 25°C, V_{DD} = 13.5V, Input voltage = 5.0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	HCKn	CHckn		5	10	pF	
	HST	CHst		5	10	pF	
Input pin current	HCK1	IHck1	–200	–60		µA	HCK1 = GND
	HCK2	IHck2	–500	–260		µA	HCK2 = GND
	HST	IHst	–300	–100		µA	HST = GND
	RGT	IRgt	–100	–15		µA	RGT = GND
Video signal input pin capacitance		Csig		30	45	pF	

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	VCKn	CVckn		5	10	pF	
	VST	CVst		5	10	pF	
Input pin current	VCK1	IVck1	–100	–30		µA	VCK1 = GND
	VCK2	IVck2	–400	–200		µA	VCK2 = GND
	VST EN CLR	IVst IEn IClr	–100	–15		µA	VST, EN, CLR = GND

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (NTSC)	PWR		35	55	mW

4. VCOM input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
VCOM – Vss input resistance	Rcom	0.5	1		MΩ

Electro-optical Characteristics (Ta = 25°C, NTSC mode)

Item			Symbol	Measurement method	Min	Typ.	Max.	Unit
Contrast ratio		25°C	CR_{25}	1	80	270	—	—
		60°C	CR_{60}		80	270	—	
Optical transmittance			T	2	2.6	3.4	—	%
Chromaticity	R	X	Rx	3	0.560	0.630	0.670	CIE standards
		Y	Ry		0.300	0.345	0.390	
	G	X	Gx		0.275	0.310	0.347	
		Y	Gy		0.541	0.595	0.650	
	B	X	Bx		0.120	0.148	0.187	
		Y	By		0.040	0.088	0.122	
V-T characteristics	V_{90}	25°C	$V_{90\text{-}25}$	4	1.1	1.6	2.2	V
		60°C	$V_{90\text{-}60}$		1.0	1.5	2.1	
	V_{50}	25°C	$V_{50\text{-}25}$		1.5	2.0	2.5	
		60°C	$V_{50\text{-}60}$		1.4	1.8	2.4	
	V_{10}	25°C	$V_{10\text{-}25}$		2.2	2.5	3.2	
		60°C	$V_{10\text{-}60}$		2.1	2.4	3.1	
Half tone color reproduction range		R vs. G	V_{50RG}	5	—	–0.10	–0.25	V
		B vs. G	V_{50BG}		—	0.10	0.45	
Response time	ON time	0°C	ton0	6	—	30	100	ms
		25°C	ton25		—	8	40	
	OFF time	0°C	toff0		—	65	150	
		25°C	toff25		—	20	60	
Flicker		60°C	F	7	—	—	–40	dB
Image retention time		60 min.	YT60	8	—	—	20	s

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

V_{DD} = 13.5V

VVC = 6.0V, VCOM = 5.6V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of screen unless otherwise specified.

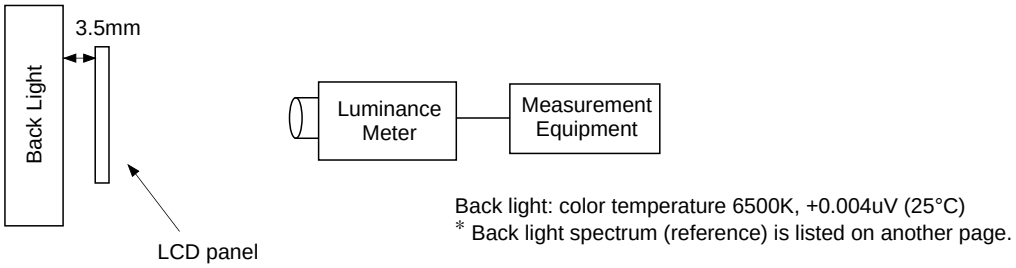
(4) Measurement systems

Two types of measurement system are used as shown below.

(5) RGB input signal voltage (Vsig)

Vsig = 6 ± V_{AC} (V) (V_{AC}: signal amplitude)

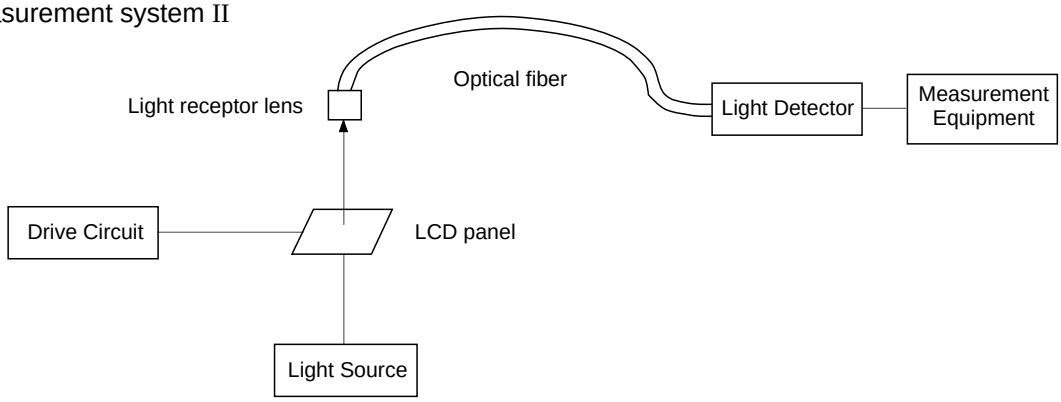
* Measurement system I



Back light: color temperature 6500K, +0.004uV (25°C)

* Back light spectrum (reference) is listed on another page.

* Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L\ (White)}{L\ (Black)} \quad ...(1)$$

L (White): Surface luminance of the TFT-LCD panel at the RGB signal amplitude V_{AC} = 0.5V.

L (Black): Surface luminance of the panel at V_{AC} = 4.5V.

Both luminosities are measured by System I.

2. Optical Transmittance

Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{L\ (White)}{Luminance\ of\ Back\ Light} \times 100\ [\%] \quad ...(2)$$

L (White) is the same expression as defined in the "Contrast Ratio" section.

3. Chromaticity

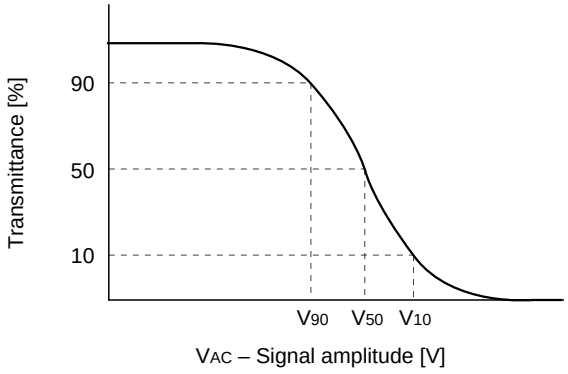
Chromaticity of the panels are measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses Chromaticity of x and y on the CIE standards here.

		Signal amplitudes (V_{AC}) supplied to each input		
		R input	G input	B input
Raster	R	0.5	4.5	4.5
	G	4.5	0.5	4.5
	B	4.5	4.5	0.5

(Unit : V)

4. V-T Characteristics

V-T characteristics, the relationship between signal amplitude and the transmittance of the panels, are measured by System II. V_{90}, V_{50} and V_{10} correspond to the each voltage which defines 90%, 50% and 10% of transmittance respectively. (Transmittance at V_{AC} = 0.5V is 100%.)

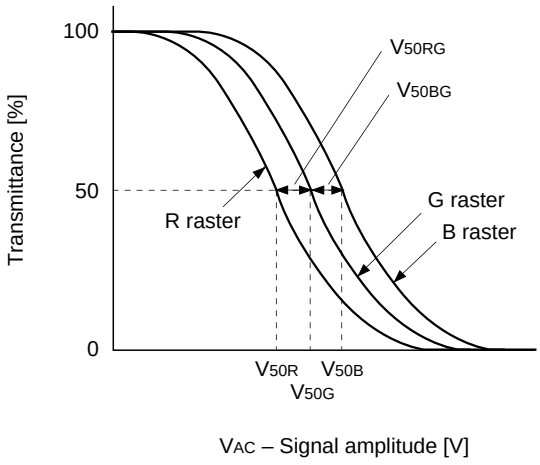


5. Half Tone Color Reproduction Range

Half tone color reproduction range of the LCD panels is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by System II. System II defines signal voltages of each R, G, B raster modes which correspond to 50% of transmittance, V_{50R}, V_{50G} and V_{50B} respectively. V_{50RG} and V_{50BG}, the voltage differences between V_{50R} and V_{50G}, V_{50B} and V_{50G}, are simply given by the following formulas (3) and (4) respectively.

$V_{50RG} = V_{50R} - V_{50G}$ ...(3)

$V_{50BG} = V_{50B} - V_{50G}$ ...(4)



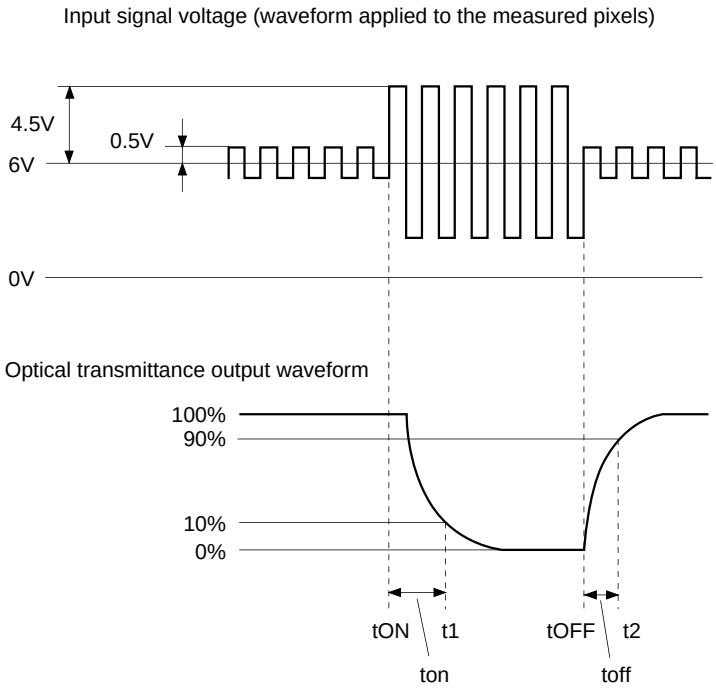
6. Response Time

Response time ton and toff are defined by the formulas (5) and (6) respectively.

ton = t1 – tON ...(5)
toff = t2 – tOFF ...(6)

t1: time which gives 10% transmittance of the panel.
t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



7. Flicker

Flicker (F) is given by the formula (7). DC and AC (NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

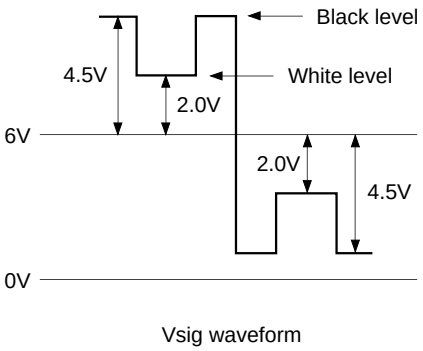
$$F\ (dB) = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\} \quad ...(7)$$

* R, G, B input signal condition for gray raster mode is given by Vsig = 6 ± V_{50} (V)
where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

8. Image Retention Time

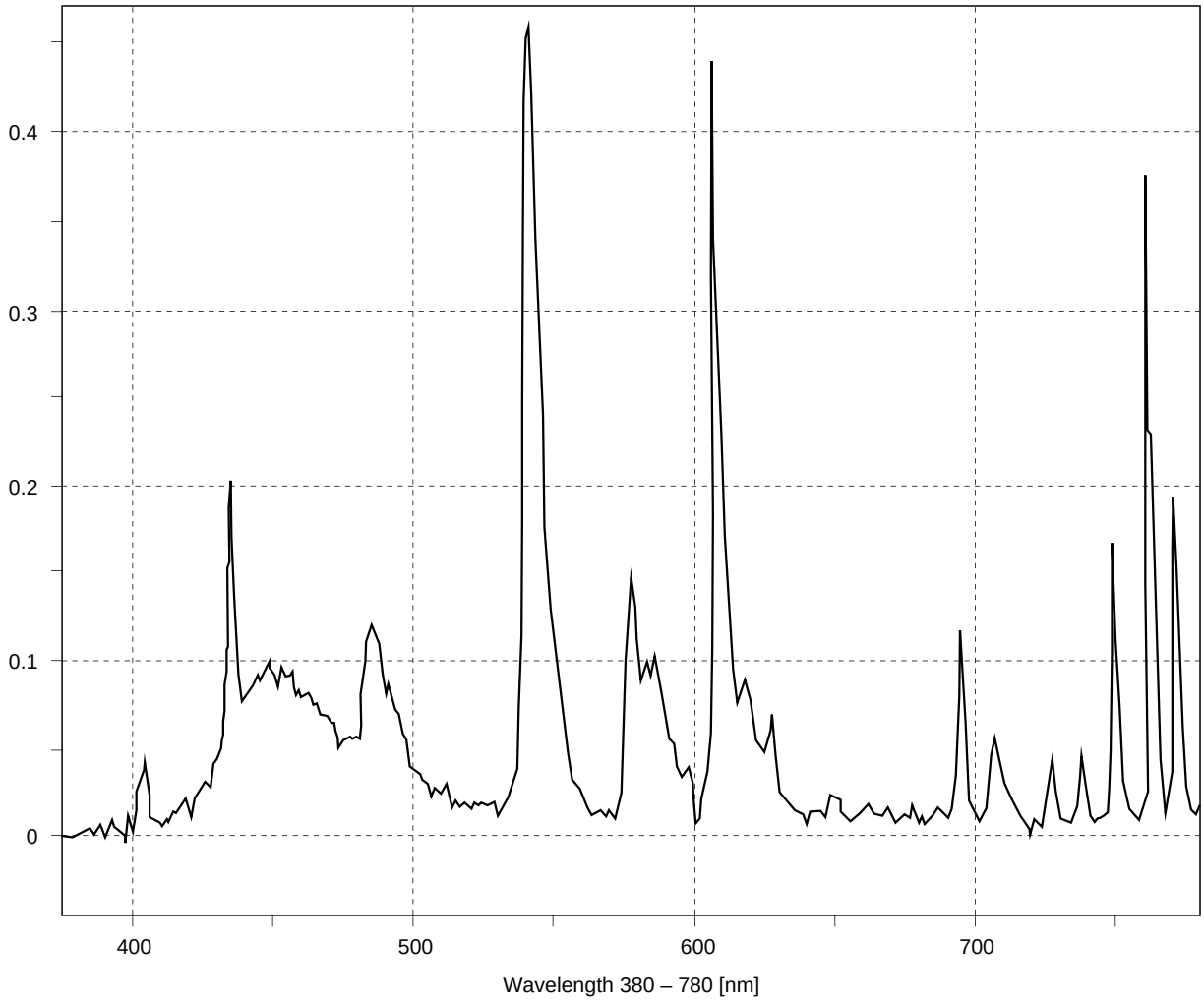
Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of Vsig = 6 ± V_{AC} (V_{AC}: 3 to 4V), judging by sight at V_{AC} that hold the maximum image retention, measure the time till the residual image becomes indistinct.

* Monoscope signal conditions:
Vsig = 6 ± 4.5 or 6 ± 2.0 (V)
(shown in the right figure)
V_{COM} = 5.6V



Vsig waveform

Example of Back Light Spectrum (Reference)

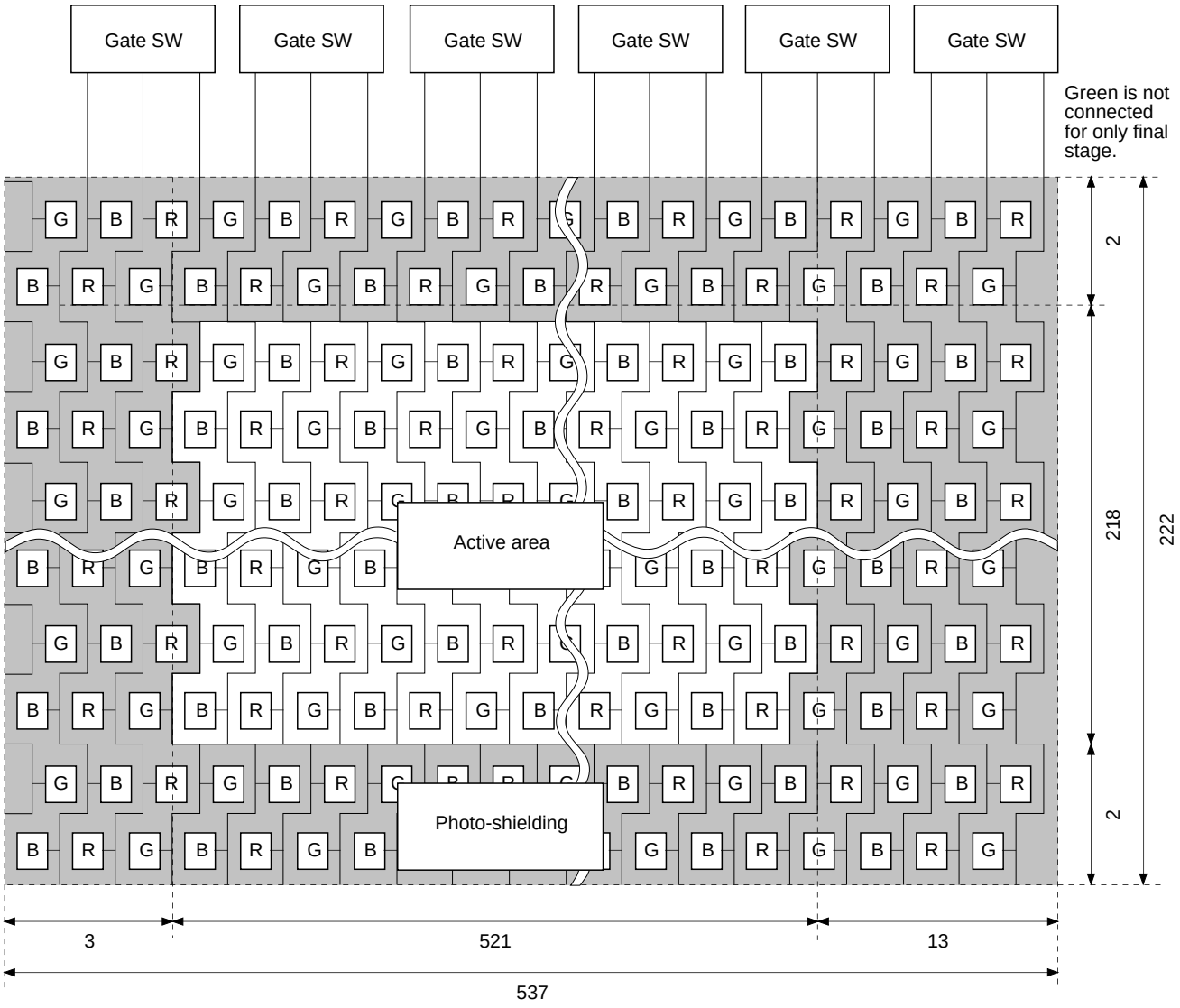


Description of Operation

1. Color Coding

   Color filters are coded in a delta arrangement.

   The shaded area is used for the dark border around the display.



2. LCD Panel Operations

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 218 gate lines sequentially in every horizontal scanning period. A vertical shift register scans the gate lines from the top to bottom of the panel.

- The selected pulse is delivered when the enable pin turns to High level. PAL mode images are displayed by controlling the enable and VCK1, VCK2 pins. The enable pin should be High when not in use.

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits applies selected pulses to every 521 signal electrodes sequentially in a single horizontal scanning period.

- Scanning direction of horizontal shift register can be switched with RGT pin. Scanning direction is left to right for RGT pin at High level; and right to left for RGT pin at Low level. (These scanning directions are from a front view.) Normally, set to High level.

- Vertical and horizontal drivers address one pixel and then turn on Thin Film Transistors (TFTs; two TFTs) to apply a video signal to the dot. The same procedures lead to the entire 218 × 521 dots to display a picture in a single vertical scanning period.

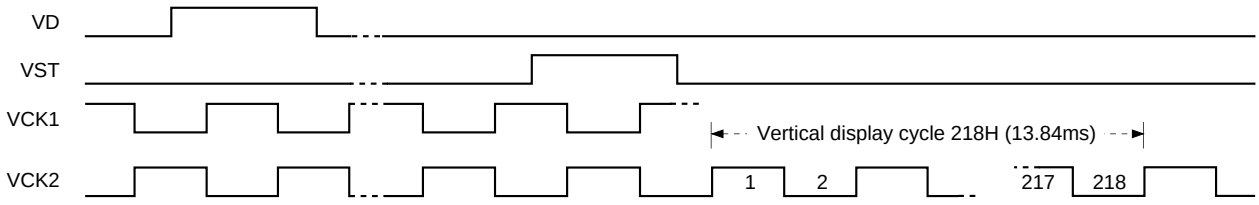
- Pixel dots are arranged in a delta pattern, where sets of RGB pixels are positioned with 1.5-dot shifted against adjacent horizontal line. 1.5-dot shift of a horizontal driver output pulse against horizontal synchronized signal is required to apply a video signal to each dot properly. 1H reversed displaying mode is required to apply video signal to the panel.

- The CLR pin is provided to eliminate the shading effect caused by the coupling of selected pulses. While maintaining the CLR at High level, the V_{DD} potential of gate output inverter drops to approximately 8.5V. This pin shall be grounded when not in use.

- The video signal shall be input with polarity-inverted system in every horizontal cycle.

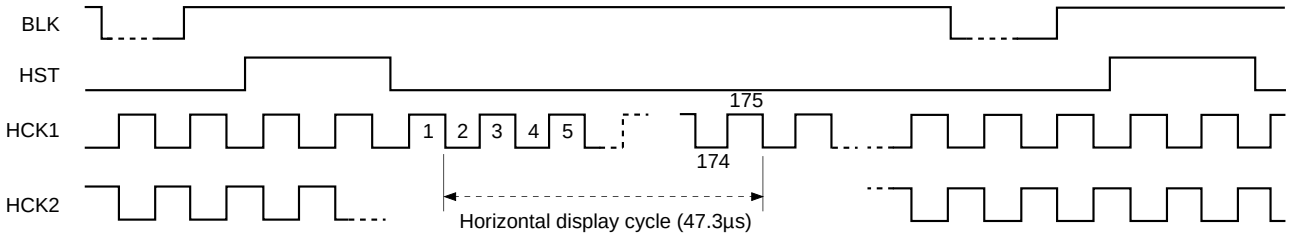
- Timing diagrams of the vertical and the horizontal right-direction scanning (RGT = High level) display cycle are shown below:

(1) Vertical display cycle



* VST is sampled at first for VCK2.

(2) Horizontal display cycle (right scan)



* HST is sampled at first for HCK1.

The horizontal display cycle consists of 521/3 = 174 clock pulses because of RGB simultaneous sampling.

* Refer to Description of Operation "3. RGB Simultaneous Sampling."

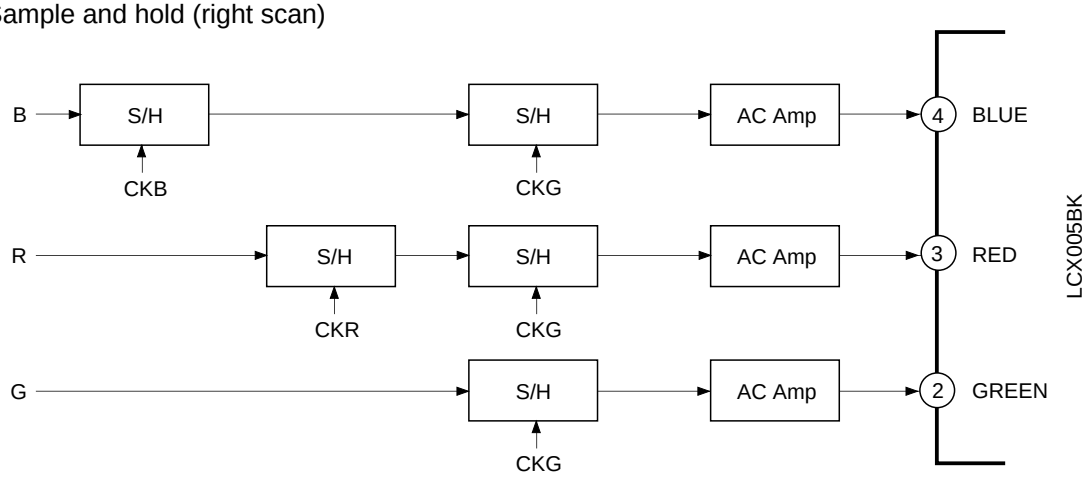
3. RGB Simultaneous Sampling

Horizontal driver samples R, G and B signal simultaneously, which requires the phase matching between R, G and B signals to prevent horizontal resolution from deteriorating. Thus phase matching between each signal is required using an external signal delaying circuit before applying video signal to the LCD panel.

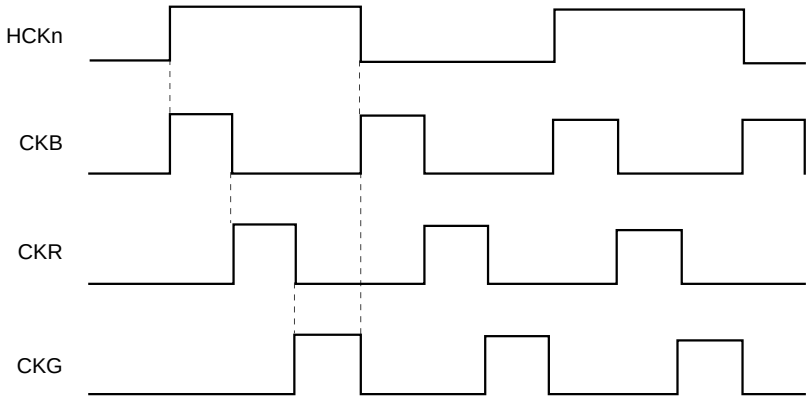
Two methods are applied for the delaying procedure: Sample and hold and Delay circuit. These two block diagrams are as follows.

The LCX005BK has the right/left inverse function. The following phase relationship diagram indicates the phase setting for the right scan (RGT = High level). For the left scan (RGT = Low level), the phase setting shall be inverted between B and G signals.

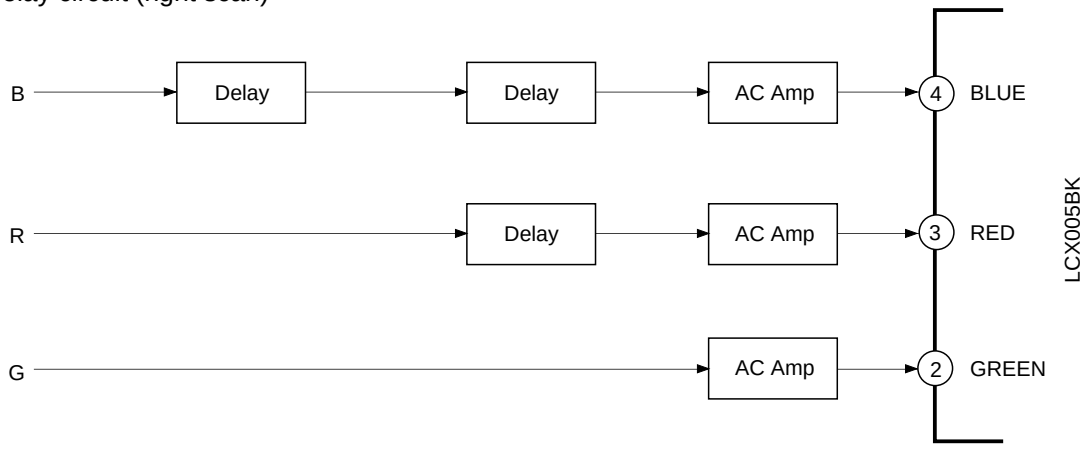
(1) Sample and hold (right scan)



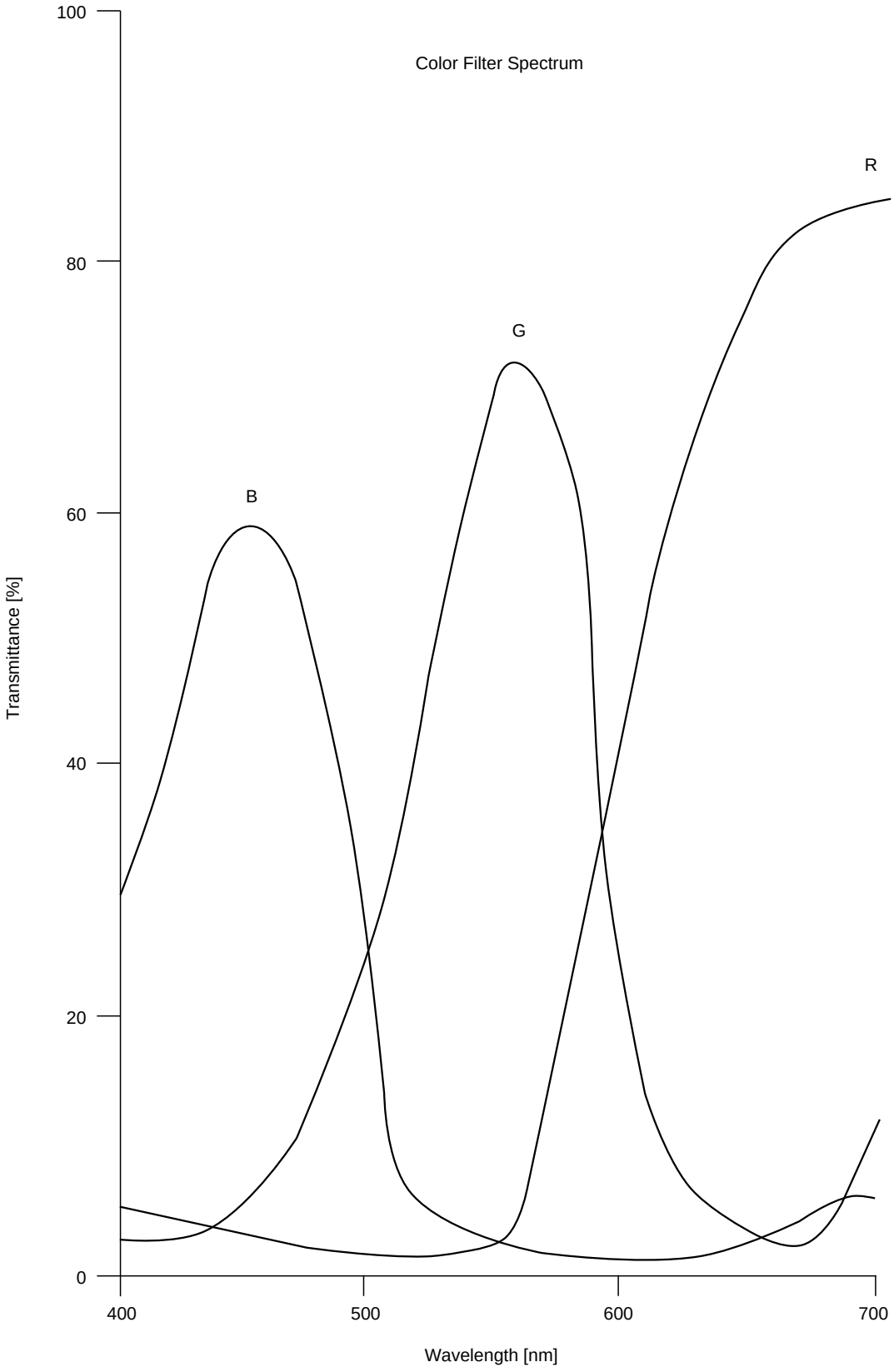
<Phase relationship of delaying sample-and-hold pulses> (right scan)



(2) Delay circuit (right scan)

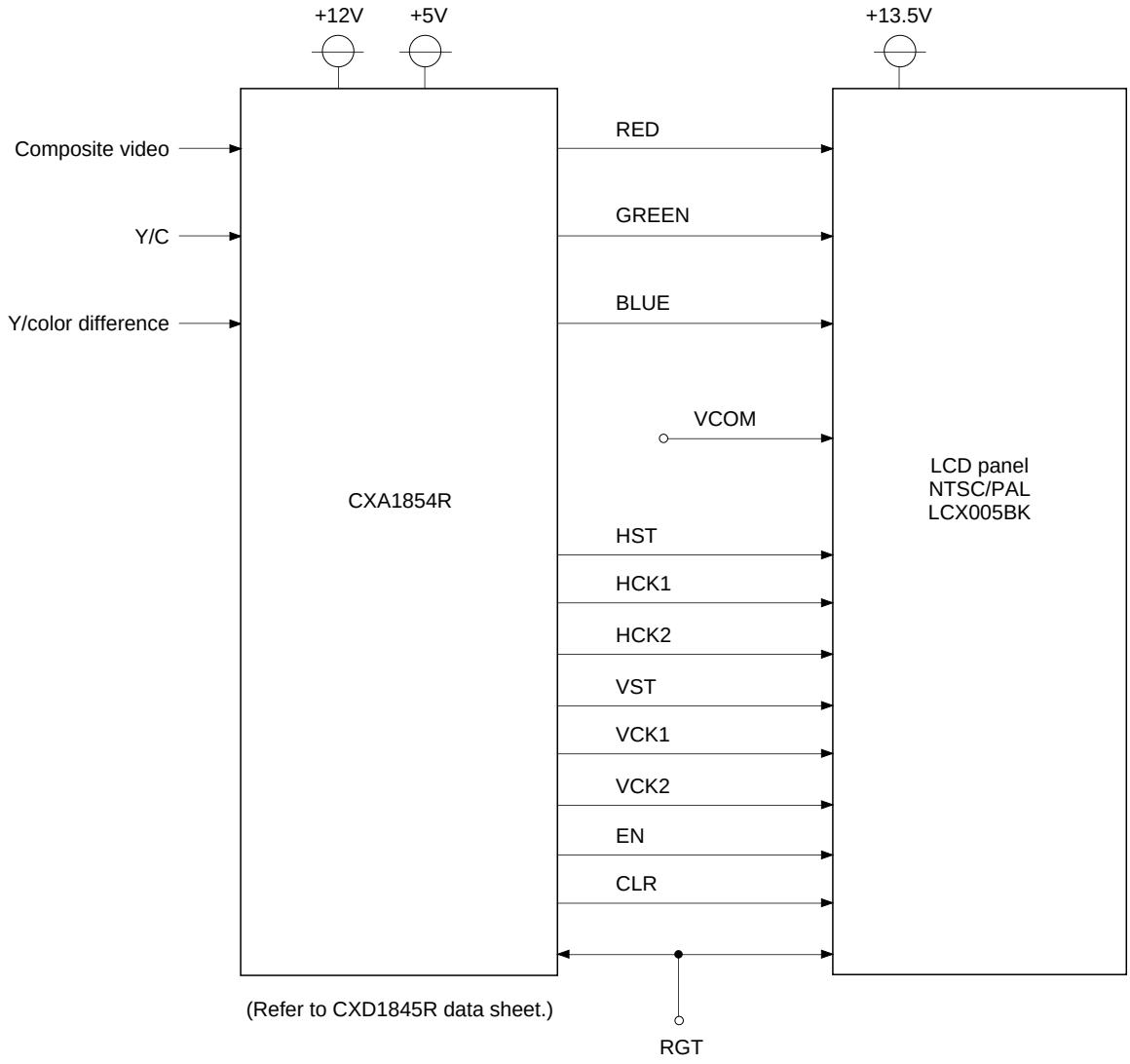


Example of Color Filter Spectrum (Reference)



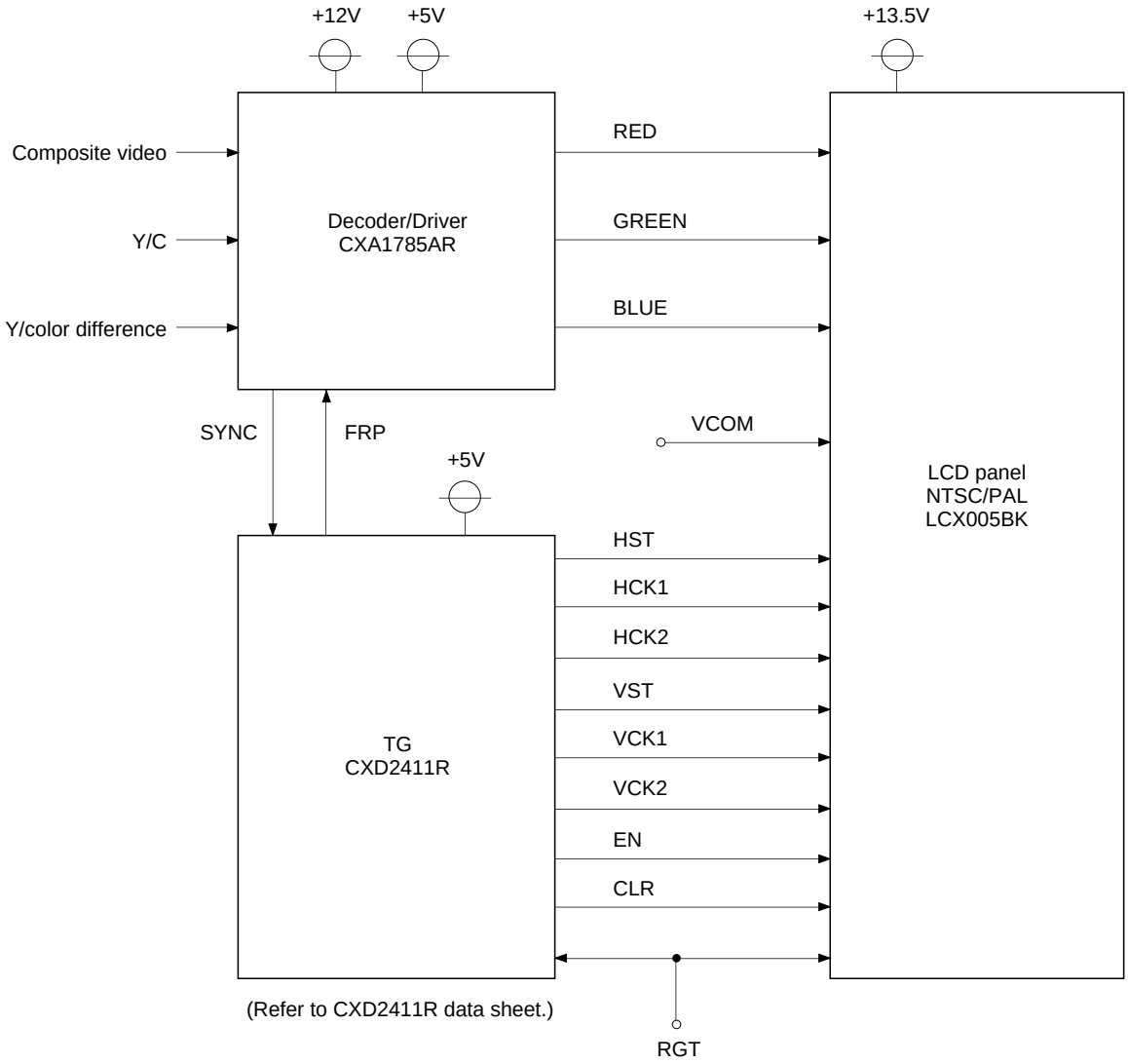
Color Display System Block Diagram (1)

An example of single-chip display system is shown below.



Color Display System Block Diagram (2)

An example of dual-chip display system is shown below.



Notes on Handling

(1) Static charge prevention

Be sure to take following protective measures. TFT-LCD panels are easily damaged by static charge.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mat on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

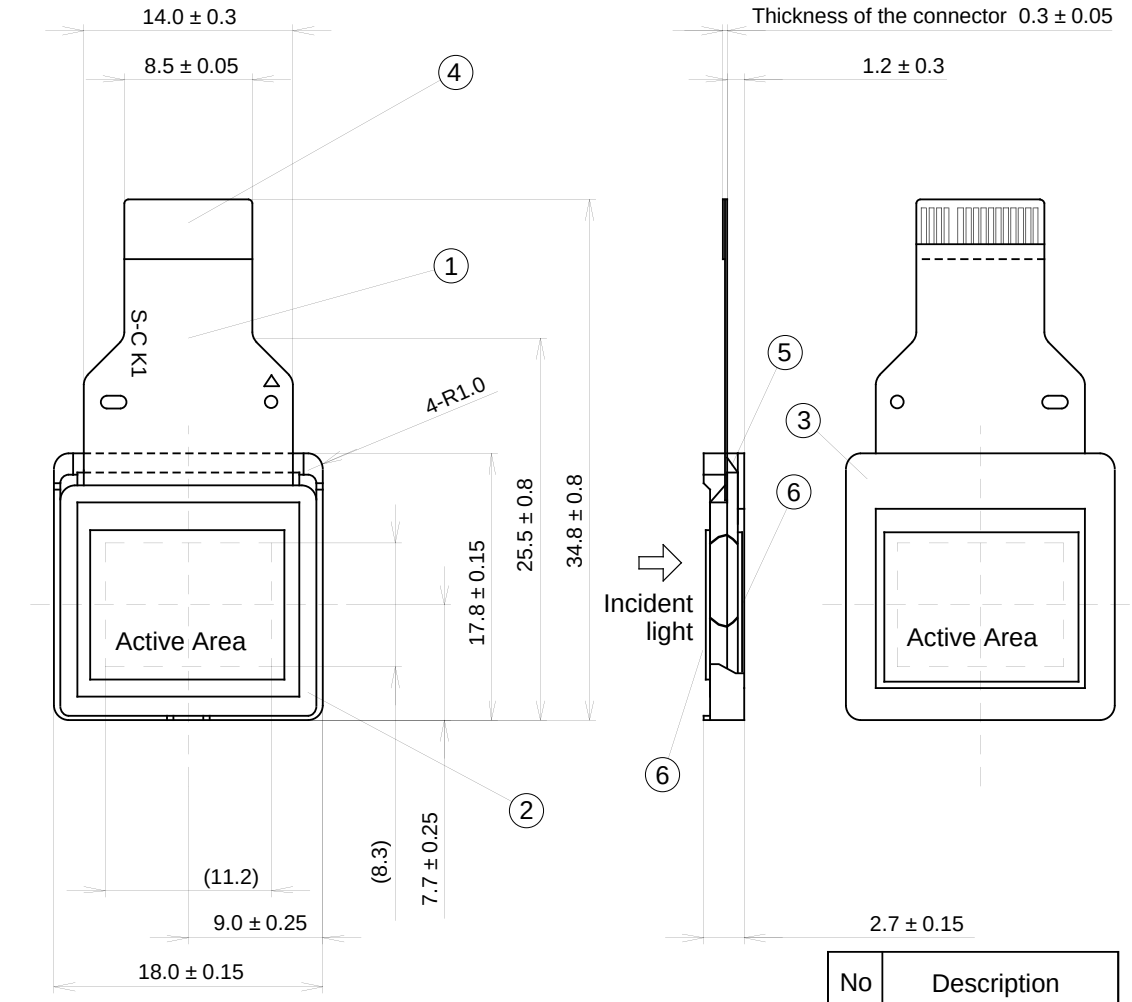
(2) Protection from dust and dirt

a) Operate in clean environment.
b) When delivered, a surface of a panel (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully not to damage the panel.
c) Do not touch the surface of a panel. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stain on the surface.
d) Use ionized air to blow off dust at a panel.

(3) Other handling precautions

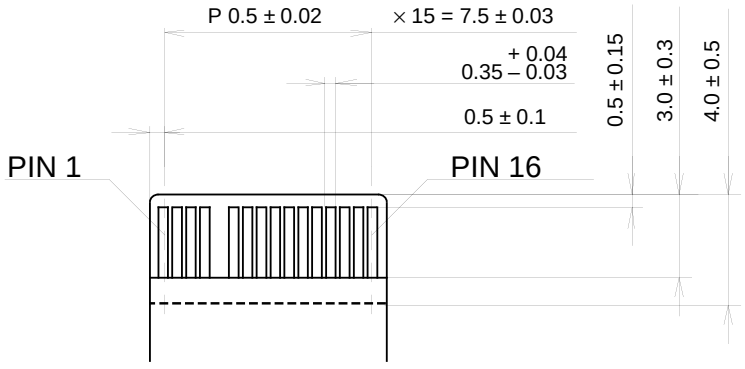
a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop a panel.
c) Do not twist or bend a panel or a panel frame.
d) Keep a panel away from heat source.
e) Do not dampen a panel with water or other solvents.
f) Avoid to store or to use a panel in a high temperature or in a high humidity, which may result in panel damages.

Package Outline Unit: mm



No	Description
1	F P C
2	Molding material
3	Outside frame
4	Reinforcing board
5	Reinforcing material
6	Polarizing film

weight 1.3g



electrode (enlarged)