FAIRCHILD SEMICONDUCTOR™

July 1988
Revised August 2000

100341
Low Power 8-Bit Shift Register

General Description

The 100341 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 kΩ pull-down resistors.

Features

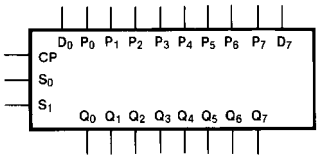
- 35% power reduction of the 100141
- 2000V ESD protection
- Pin/function compatible with 100141
- Voltage compensated operating range = –4.2V to –5.7V
- Available to industrial grade temperature range

Ordering Code:

Order Number	Package Number	Package Description
10034SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100341PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100341QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100341QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (–40°C to +85°C)

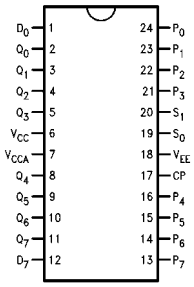
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

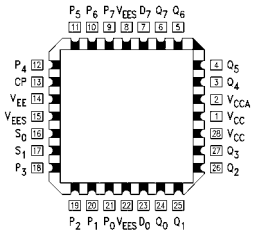


Connection Diagrams

24-Pin DIP/SOIC



28-Pin PLCC



Pin Descriptions

Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

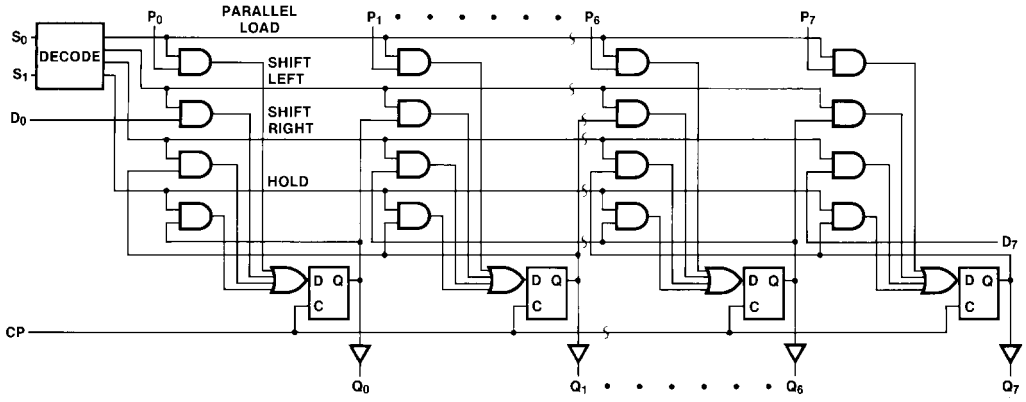
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Truth Table

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	⌐	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	⌐	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	⌐	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	⌐	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	⌐	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH Transition

Logic Diagram



Absolute Maximum Ratings (Note 1)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 3)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or V_{IL} (Min)	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or V_{IL} (Max)	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	μA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current					Inputs OPEN	
		−157		−75	mA	V_{EE} = −4.2V to −4.8V	
		−167		−75	mA	V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter		T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
			Min	Max	Min	Max	Min	Max		
f_{MAX}	Max Clock Frequency		400		400		400		MHz	Figures 2, 3
t_{PLH}	Propagation Delay		0.90	1.90	1.00	2.00	1.00	2.10	ns	Figures 1, 3
t_{PHL}	CP to Output									(Note 4)
t_{TLH}	Transition Time		0.35	1.30	0.35	1.30	0.35	1.30	ns	Figures 1, 3
t_{THL}	20% to 80%, 80% to 20%									
t_S	Setup Time	D_n, P_n	0.65		0.65		0.65		ns	Figure 4
		S_n	1.60		1.60		1.60			
t_H	Hold	D_n, P_n	0.80		0.80		0.80		ns	
		S_n	0.60		0.60		0.60			
t_{PW}(H)	Pulse Width HIGH	CP	2.00		2.00		2.00		ns	Figure 3

Note 4: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Commercial Version (Continued)
SOIC and PLCC AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	425		425		425		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	1.70	1.00	1.80	1.00	1.90	ns	Figures 1, 3 (Note 5)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1, 3
t_S	Setup Time D_n, P_n	0.55		0.55		0.55		ns	Figure 4
	S_n	1.50		1.50		1.50			
t_H	Hold Time D_n, P_n	0.70		0.70		0.70		ns	
	S_n	0.50		0.50		0.50			
t_{PW}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figure 3
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PLCC Only (Note 6)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Clock to Output Path		200		200		200	ps	PLCC Only (Note 6)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Clock to Output Path		250		250		250	ps	PLCC Only (Note 6)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Clock to Output Path		250		250		250	ps	PLCC Only (Note 6)

Note 5: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Note 6: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design

Industrial Version

PLCC DC Electrical Characteristics (Note 7)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = V_{IH}(Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	or V_{IL} (Min)	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage		−1565		−1610	mV	or V_{IL} (Max)	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for all Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for all Inputs	
I_{IL}	Input LOW Current	0.50		0.50		µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	µA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current						Inputs OPEN	
		−157	−75	−157	−75	mA	V_{EE} = −4.2V to −4.8V	
		−167	−75	−167	−75	mA	V_{EE} = −4.2V to −5.7V	

Note 7: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

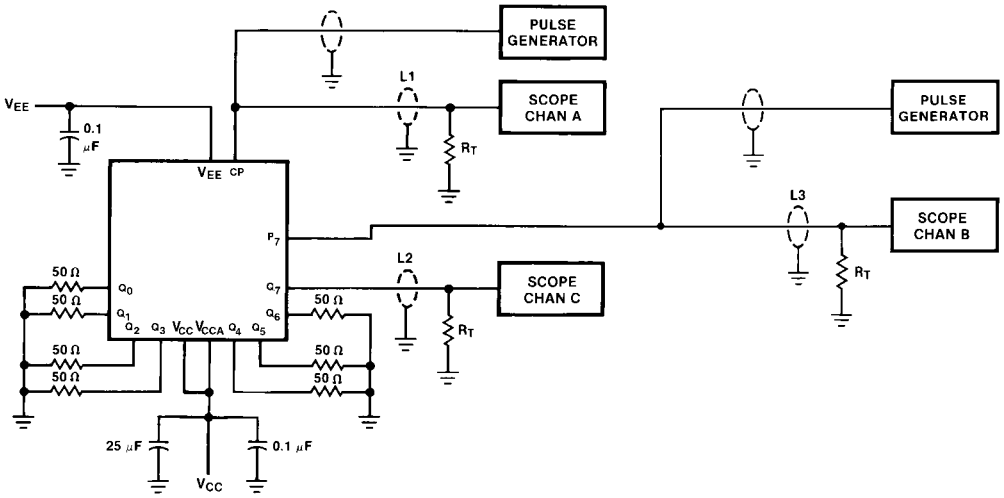
PLCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter		T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
			Min	Max	Min	Max	Min	Max		
f_{MAX}	Max Clock Frequency		425		425		425		MHz	Figures 2, 3
t_{PLH} t_{PHL}	Propagation Delay CP to Output		0.90	1.80	1.00	1.80	1.00	1.90	ns	Figures 1, 3 (Note 8)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%		0.30	1.90	0.35	1.20	0.35	1.20	ns	Figures 1, 3
t_S	Setup Time	D_n, P_n	0.60		0.55		0.55		ns	Figure 4
		S_n	1.70		1.50		1.50			
t_H	Hold Time	D_n, P_n	0.90		0.70		0.70		ns	
		S_n	0.50		0.50		0.50			
t_{PW}(H)	Pulse Width HIGH	CP	2.00		2.00		2.00		ns	Figure 3

Note 8: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

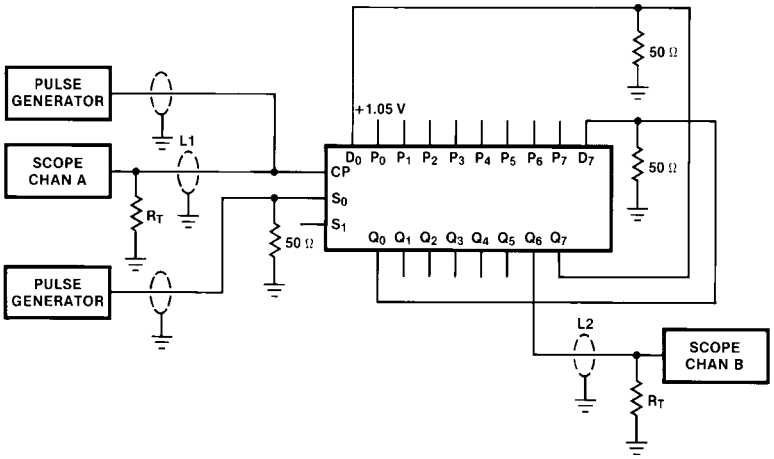
Test Circuitry



Note:

- V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
- L1, L2 and L3 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to $V_{CC}$and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



Note:

- For shift right mode pulse generator connected to S_0 is moved to S_1.
- Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.
- The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Switching Waveforms

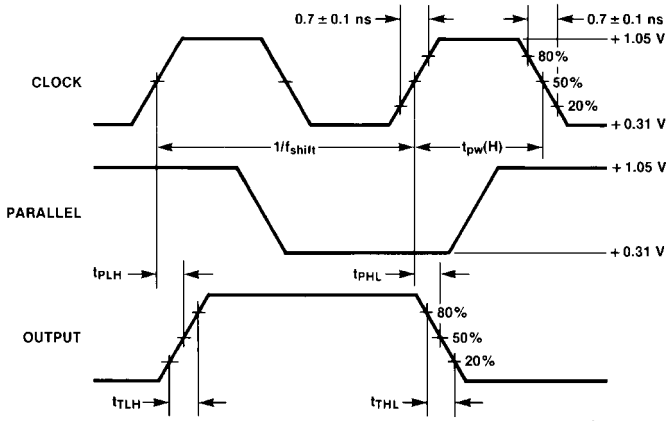
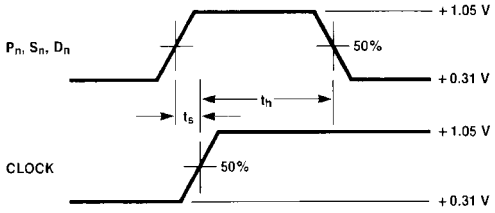


FIGURE 3. Propagation Delay and Transition Times



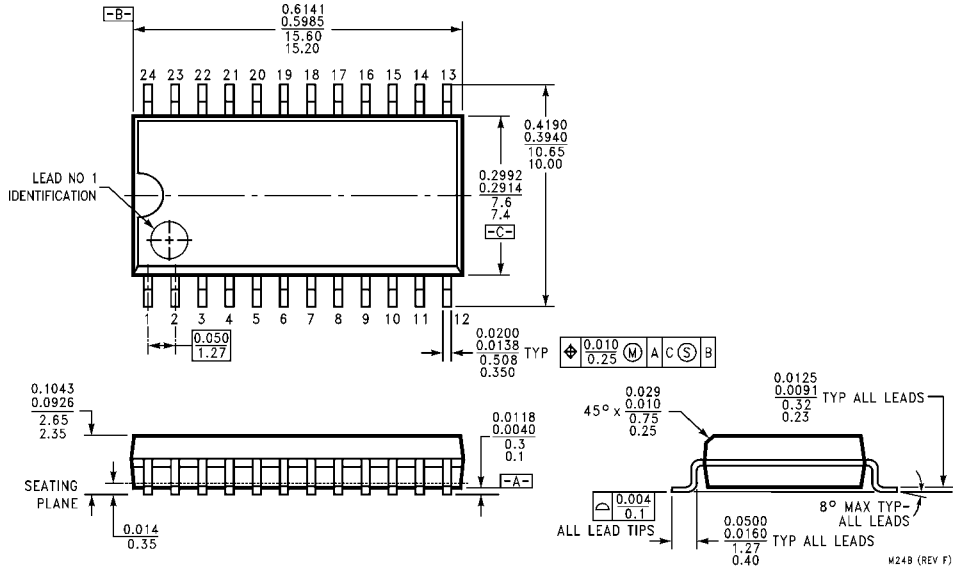
Note:

t_S is the minimum time before the transition of the clock that information must be present at the data input.

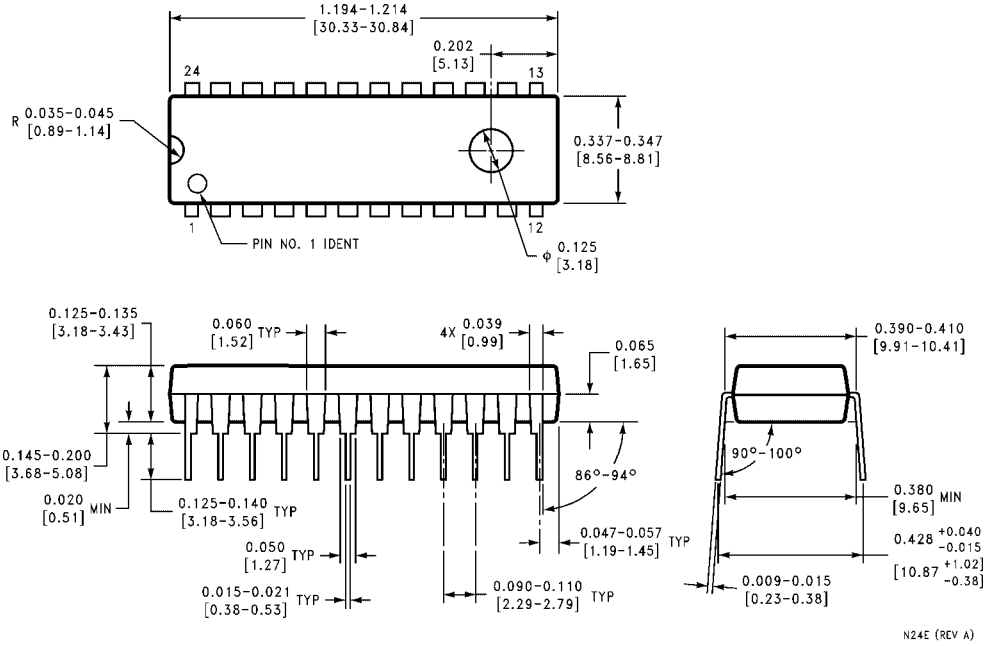
t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 4. Setup and Hold Times

Physical Dimensions inches (millimeters) unless otherwise noted

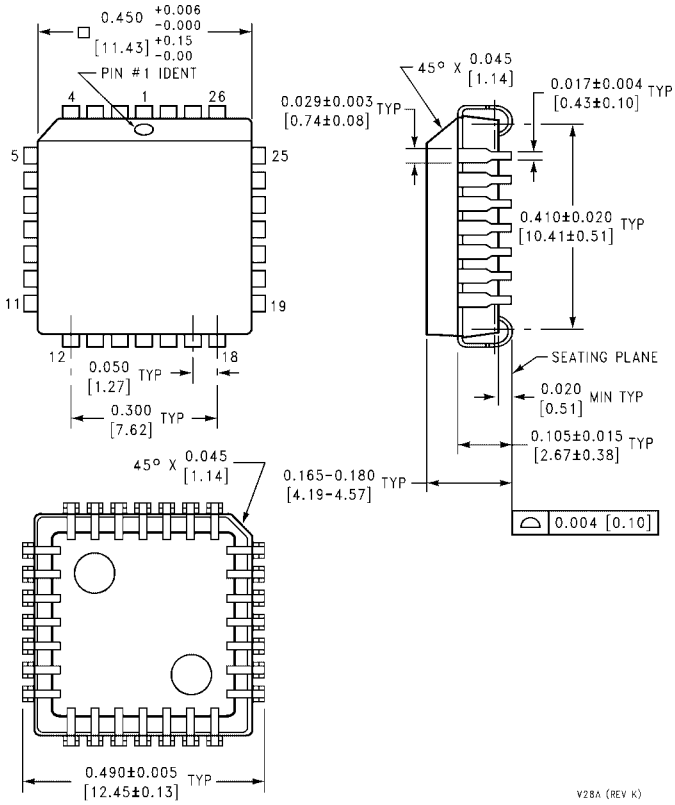


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

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