transphorm

# TPH3206PSB

## 650V GaN FET in TO-220 (source tab)

### Description

The TPH3206PSB 650V, 150mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

Transphorm GaN offers improved efficiency over silicon, through lower gate charge, lower crossover loss, and smaller reverse recovery charge.

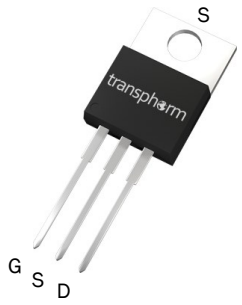
### Related Literature

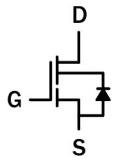
- AN0009: Recommended External Circuitry for GaN FETs
- AN0003: Printed Circuit Board Layout and Probing
- AN0010: Paralleling GaN FETs

### Ordering Information

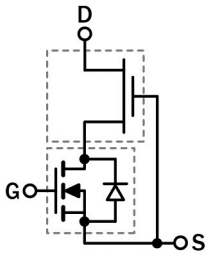
| Part Number | Package | Package Configuration |
|---|---|---|
| TPH3206PSB | 3 lead TO-220 | Source |

**TPH3206PSB**
**TO-220**
(top view)




**Cascode Schematic Symbol**




**Cascode Device Structure**

### Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Intrinsic lifetime tests
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low $Q_{RR}$
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

### Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

### Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor

| Key Specifications | |
|---|---|
| $V_{DSS}$ (V) | 650 |
| $V_{(TR)DSS}$ (V) | 800 |
| $R_{DS(on)eff}$ (mΩ) max* | 180 |
| $Q_{RR}$ (nC) typ | 52 |
| $Q_G$ (nC) typ | 6.2 |

* Dynamic on-resistance; see Figures 19 and 20

| Common Topology Power Recommendations | |
|---|---|
| CCM bridgeless totem-pole* | 1519W max |
| Hard-switched inverter** | 1717W max |

Conditions: $F_{SW}$=45kHz; $T_J$=115°C; $T_{HEATSINK}$=90°C; insulator between device and heatsink (6 mil Sil-Pad® K-10); power de-rates at lower voltages with constant current

* $V_{IN}$=230$V_{AC}$; $V_{OUT}$=390$V_{DC}$
** $V_{IN}$=380$V_{DC}$; $V_{OUT}$=240$V_{AC}$


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## Absolute Maximum Ratings ($T_C$=25°C unless otherwise stated.)

| Symbol | Parameter | | Limit Value | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to source voltage ($T_J$ = -55°C to 150°C) | | 650 | V |
| $V_{(TR)DSS}$ | Transient drain to source voltage [a] | | 800 | |
| $V_{GSS}$ | Gate to source voltage | | ±18 | |
| $P_D$ | Maximum power dissipation @$T_C$=25°C | | 81 | W |
| $I_D$ | Continuous drain current @$T_C$=25°C [b] | | 16 | A |
| | Continuous drain current @$T_C$=100°C [b] | | 10 | A |
| $I_{DM}$ | Pulsed drain current (pulse width: 10µs) | | 60 | A |
| $(di/dt)_{RDMC}$ | Reverse diode di/dt, repetitive [c] | | 1200 | A/µs |
| $(di/dt)_{RDMT}$ | Reverse diode di/dt, transient [d] | | 2400 | A/µs |
| $T_C$ | Operating temperature | Case | -55 to +150 | °C |
| $T_J$ | | Junction | -55 to +150 | °C |
| $T_S$ | Storage temperature | | -55 to +150 | °C |
| $T_{SOLD}$ | Soldering peak temperature [e] | | 260 | °C |

Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <1µs
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. Continuous switching operation
d. ≤300 pulses per second for a total duration ≤20 minutes
e. For 10 sec., 1.6mm from the case

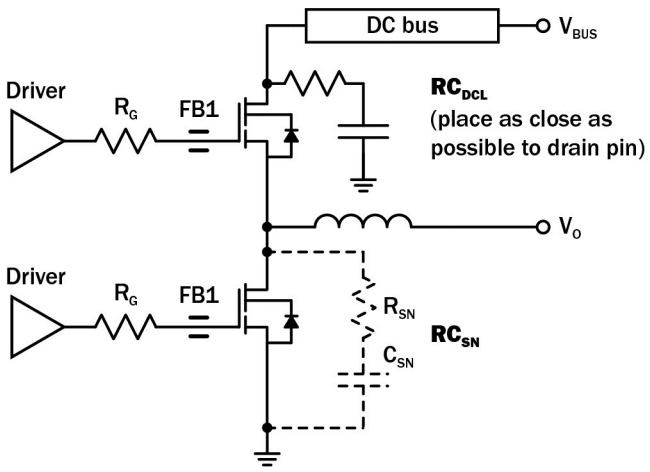
## Thermal Resistance

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Junction-to-case | 1.55 | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient | 62 | °C/W |

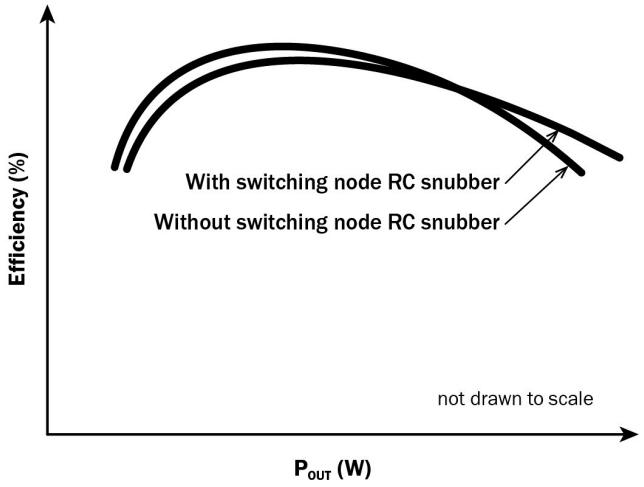


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## Circuit Implementation




Simplified Half-bridge Schematic




Efficiency vs Output Power

Recommended gate drive: (0V, 8-10V) with $R_{G(tot)}$ = 25Ω, where $R_{G(tot)} = R_G + R_{DRIVER}$

| Gate Ferrite Bead (FB1) | Required DC Link RC Snubber ($RC_{DCL}$) [a] | Recommended Switching Node RC Snubber ($RC_{SN}$) [b, c] |
|---|---|---|
| MMZ1608Q121BTA00 | 10nF + 8Ω | 22pF + 15Ω |

Notes:
a. $RC_{DCL}$ should be placed as close as possible to the drain pin
b. A switching node RC snubber (C, R) is recommended for high switching currents (>70% of $I_{RDMC1}$ or $I_{RDMC2}$; see page 5 for $I_{RDMC1}$ and $I_{RDMC2}$)
c. $I_{RDM}$ values can be increased by increasing $R_G$ and $C_{SN}$



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**Electrical Parameters** ($T_J$=25°C unless otherwise stated)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| **Forward Device Characteristics** | | | | | | |
| $V_{(BL)DSS}$ | Drain-source voltage | 650 | — | — | V | $V_{GS}$=0V |
| $V_{GS(th)}$ | Gate threshold voltage | 1.65 | 2.1 | 2.6 | V | $V_{DS}$=$V_{GS}$, $I_D$=500µA |
| $R_{DS(on)eff}$ | Drain-source on-resistance [a] | — | 150 | 180 | mΩ | $V_{GS}$=8V, $I_D$=10A |
| | | — | 308 | — | | $V_{GS}$=8V, $I_D$=10A, $T_J$=150°C |
| $I_{DSS}$ | Drain-to-source leakage current | — | 2.5 | 30 | µA | $V_{DS}$=650V, $V_{GS}$=0V |
| | | — | 8 | — | | $V_{DS}$=650V, $V_{GS}$=0V, $T_J$=150°C |
| $I_{GSS}$ | Gate-to-source forward leakage current | — | — | 100 | nA | $V_{GS}$=18V |
| | Gate-to-source reverse leakage current | — | — | -100 | | $V_{GS}$=-18V |
| $C_{ISS}$ | Input capacitance | — | 720 | — | pF | $V_{GS}$=0V, $V_{DS}$=480V, *f*=1MHz |
| $C_{OSS}$ | Output capacitance | — | 46 | — | | |
| $C_{RSS}$ | Reverse transfer capacitance | — | 5.5 | — | | |
| $C_{O(er)}$ | Output capacitance, energy related [b] | — | 65 | — | pF | $V_{GS}$=0V, $V_{DS}$=0V to 480V |
| $C_{O(tr)}$ | Output capacitance, time related [c] | — | 106 | — | | |
| $Q_G$ | Total gate charge | — | 6.2 | — | nC | $V_{DS}$=100V, $V_{GS}$=0V to 4.5V, $I_D$=10A |
| $Q_{GS}$ | Gate-source charge | — | 2.1 | — | | |
| $Q_{GD}$ | Gate-drain charge | — | 2.2 | — | | |
| $Q_{OSS}$ | Output charge | — | 44.4 | — | nC | $V_{GS}$=0V, $V_{DS}$=0V to 400V |
| $t_{D(on)}$ | Turn-on delay | — | 6 | — | ns | $V_{DS}$=480V, $V_{GS}$=0V to 10V, $I_D$=10A, $R_G$=22Ω |
| $t_R$ | Rise time | — | 4.5 | — | | |
| $t_{D(off)}$ | Turn-off delay | — | 9.7 | — | | |
| $t_F$ | Fall time | — | 4 | — | | |

Notes:
a. Dynamic on-resistance; see Figures 19 and 20 for test circuit and conditions
b. Equivalent capacitance to give same stored energy as $V_{DS}$ rises from 0V to 400V
c. Equivalent capacitance to give same charging time as $V_{DS}$ rises from 0V to 400V



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**Electrical Parameters** ($T_J$=25°C unless otherwise stated)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| **Reverse Device Characteristics** | | | | | | |
| $I_S$ | Reverse current | — | — | 10 | A | $V_{GS}$=0V, $T_C$=100°C, ≤25% duty cycle |
| $V_{SD}$ | Reverse voltage [a] | — | 2.4 | — | V | $V_{GS}$=0V, $I_S$=10A |
| | | — | 3.7 | — | | $V_{GS}$=0V, $I_S$=10A, $T_J$=150°C |
| | | — | 1.7 | — | | $V_{GS}$=0V, $I_S$=5A |
| $t_{RR}$ | Reverse recovery time | — | 17 | — | ns | $I_S$=11A, $V_{DD}$=400V, di/dt=2000A/µs |
| $Q_{RR}$ | Reverse recovery charge | — | 52 | — | nC | |
| $(di/dt)_{RDMC}$ | Reverse diode di/dt, repetitive [b] | — | — | 1200 | A/µs | |
| $I_{RDMC1}$ | Reverse diode switching current, repetitive (dc) [c, e] | — | — | 11 | A | Circuit implementation and parameters on page 3 |
| $I_{RDMC2}$ | Reverse diode switching current, repetitive (ac) [c, e] | — | — | 14 | A | Circuit implementation and parameters on page 3 |
| $(di/dt)_{RDMT}$ | Reverse diode di/dt, transient [d] | — | — | 2400 | A/µs | |
| $I_{RDMT}$ | Reverse diode switching current, transient [d,e] | — | — | 18 | A | Circuit implementation and parameters on page 3 |

Notes:
a. Includes dynamic $R_{DS(on)}$ effect
b. Continuous switching operation
c. Definitions: dc = dc-to-dc converter topologies; ac = inverter and PFC topologies, 50-60Hz line frequency
d. ≤300 pulses per second for a total duration ≤20 minutes
e. $I_{RDM}$ values can be increased by increasing $R_G$ and $C_{SN}$ on page 3



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**Typical Characteristics** ($T_C$=25°C unless otherwise stated)

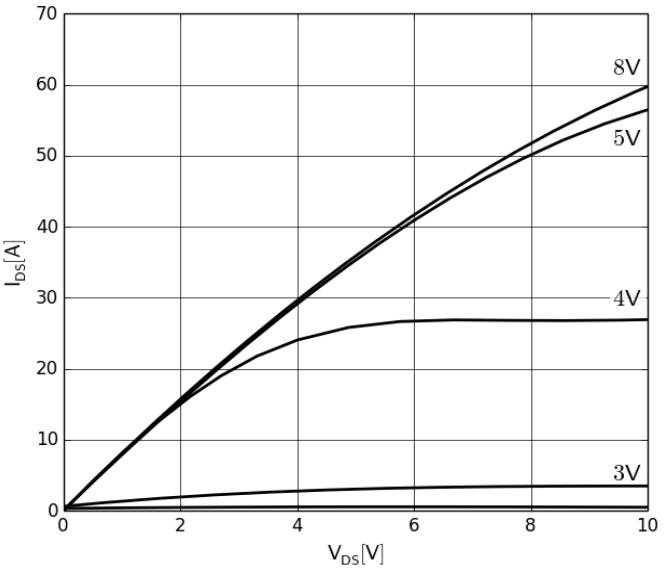



**Figure 1. Typical Output Characteristics $T_J$=25°C**
Parameter: $V_{GS}$

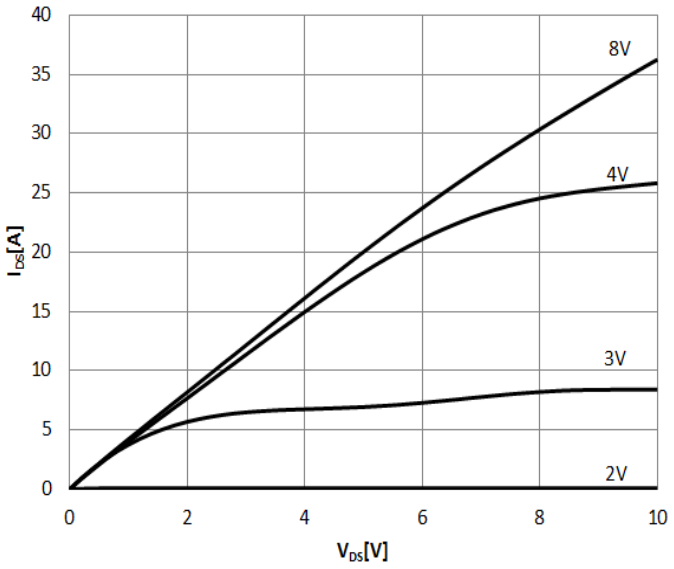



**Figure 2. Typical Output Characteristics $T_J$=150°C**
Parameter: $V_{GS}$

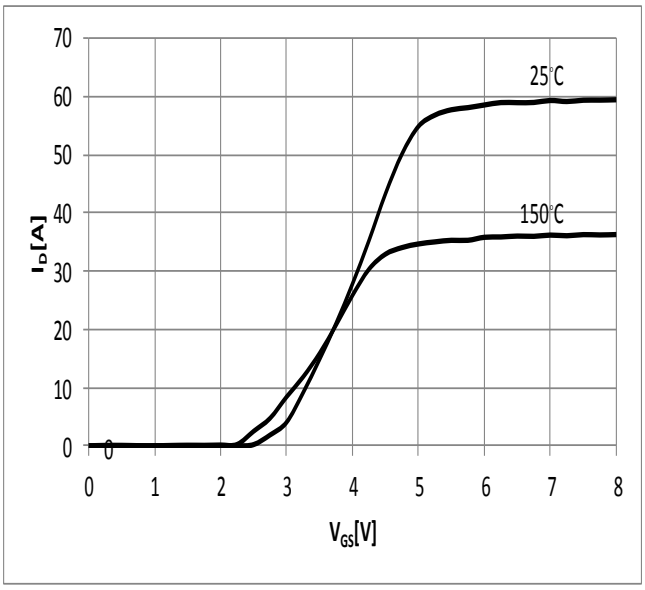



**Figure 3. Typical Transfer Characteristics**
$V_{DS}$=10V, parameter: $T_J$

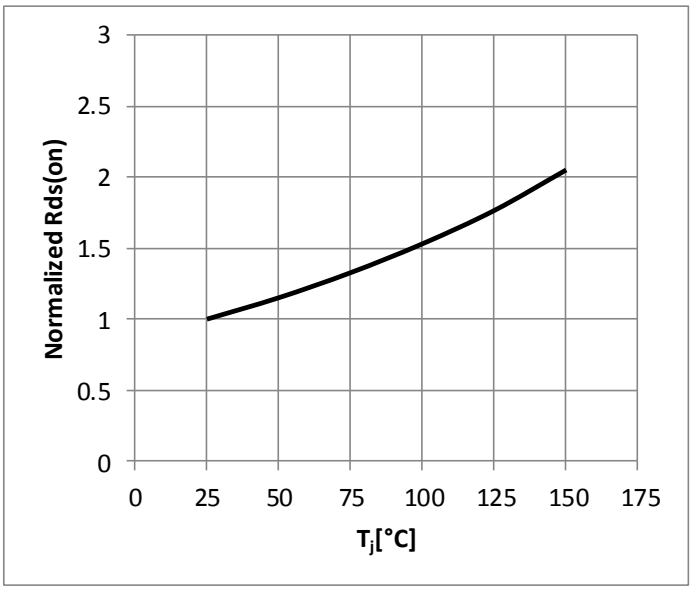



**Figure 4. Normalized On-resistance**
$I_D$=10A, $V_{GS}$=8V



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**Typical Characteristics** ($T_C$=25 °C unless otherwise stated)

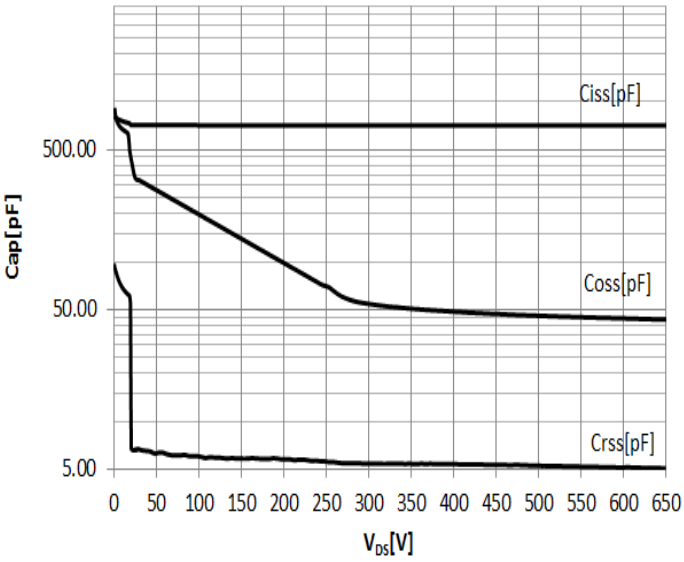



**Figure 5. Typical Capacitance**
$V_{GS}$=0V, f=1MHz

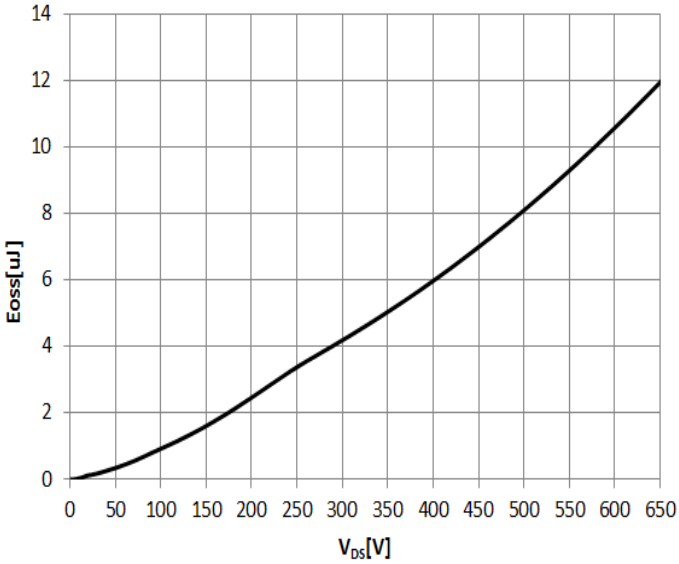



**Figure 6. Typical $C_{oss}$ Stored Energy**

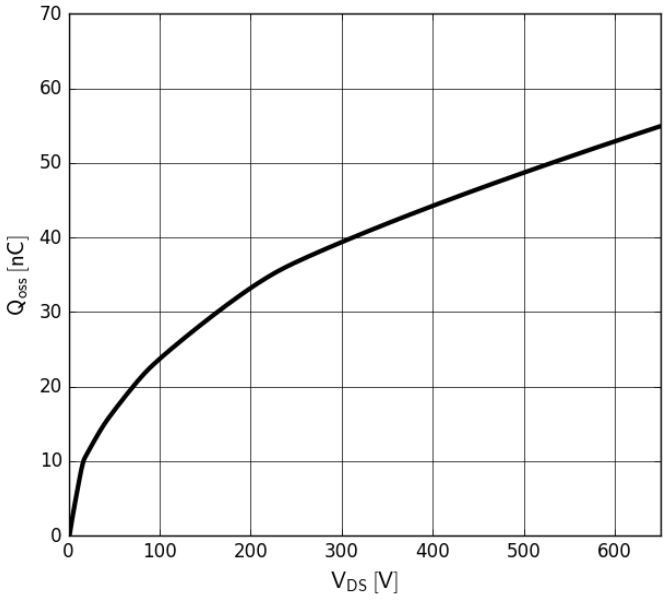



**Figure 7. Typical $Q_{oss}$**

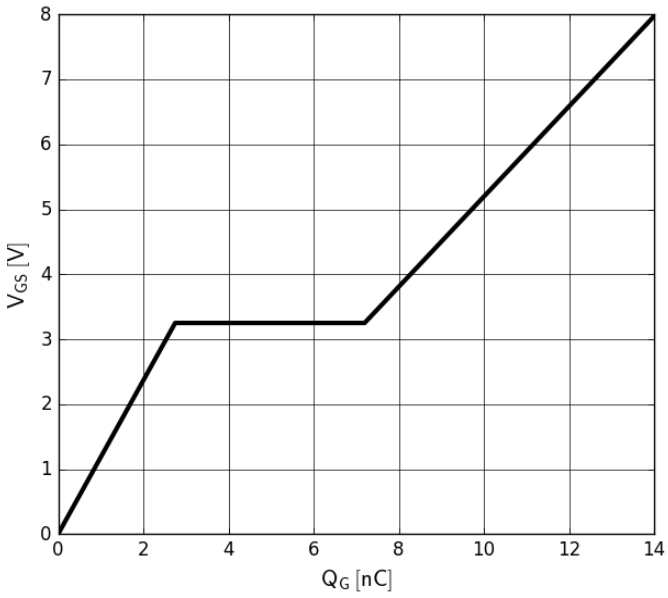



**Figure 8. Typical Gate Charge**
$I_{DS}$=10A, $V_{DS}$=400V



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**Typical Characteristics** ($T_C$=25°C unless otherwise stated)

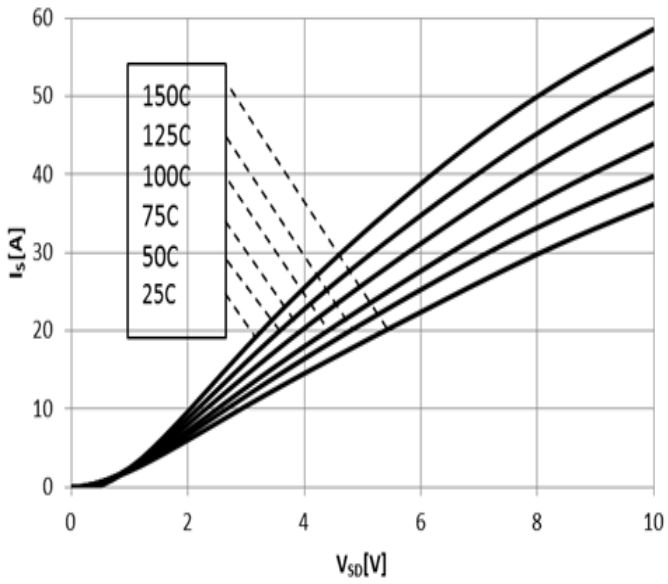



**Figure 9. Forward Characteristics of Rev. Diode**
$I_S=f(V_{SD})$, Parameter $T_J$

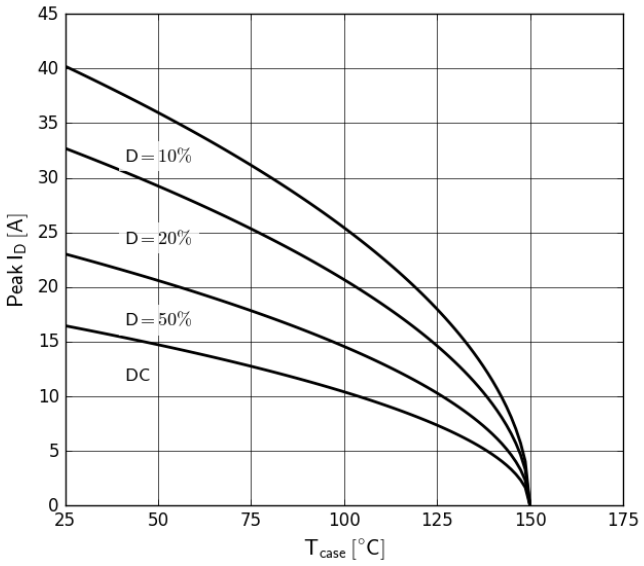



**Figure 10. Current Derating**
Pulse width = 100µs

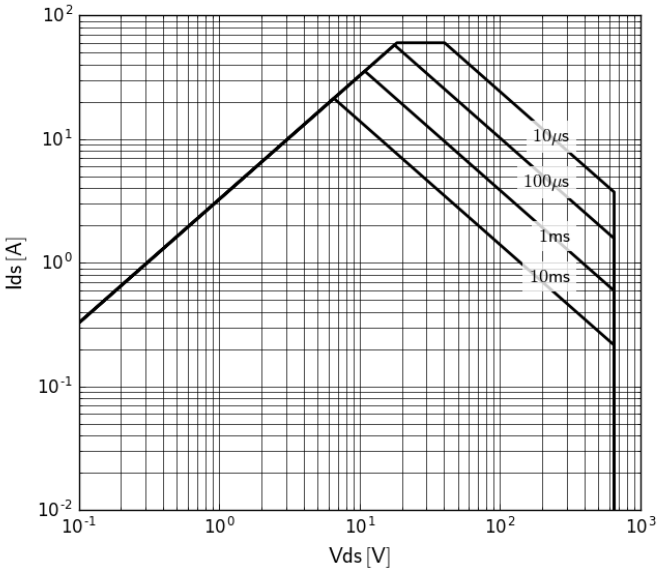



**Figure 11. Safe Operating Area $T_C$=25°C**
(calculated based on thermal limit)

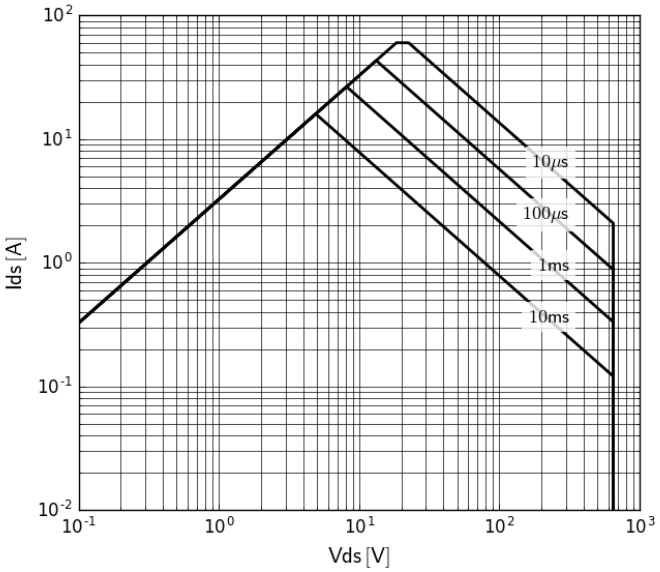



**Figure 12. Safe Operating Area $T_C$=80°C**
(calculated based on thermal limit)



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**Typical Characteristics** ($T_C$=25 °C unless otherwise stated)

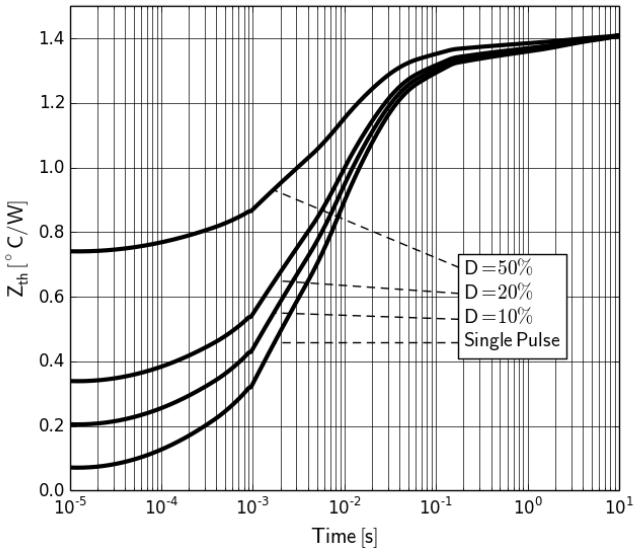



**Figure 13. Transient Thermal Resistance**

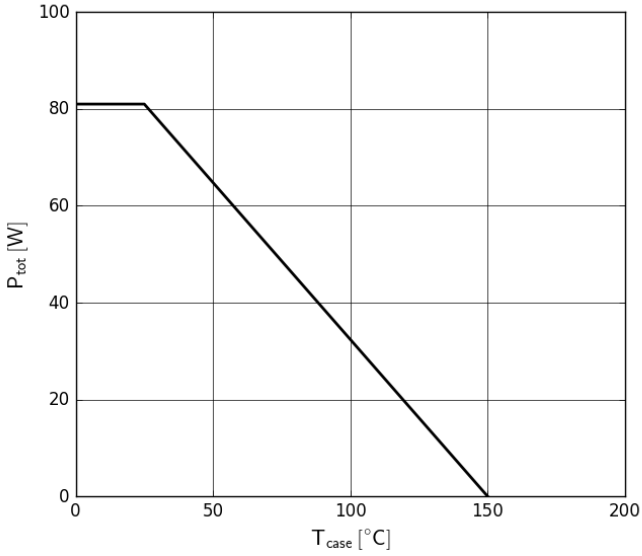



**Figure 14. Power Dissipation**



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## Test Circuits and Waveforms

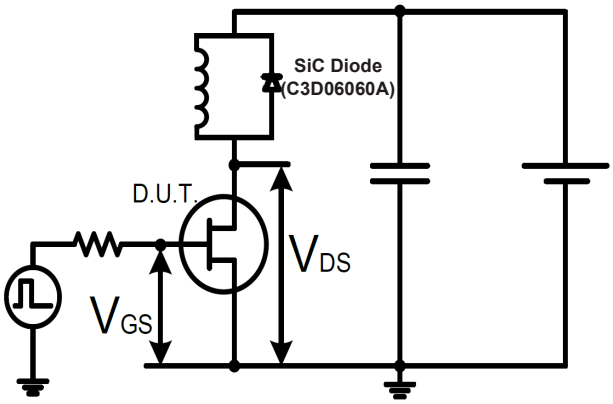



**Figure 15. Switching Time Test Circuit**
(see circuit implementation on page 3
for methods to ensure clean switching)

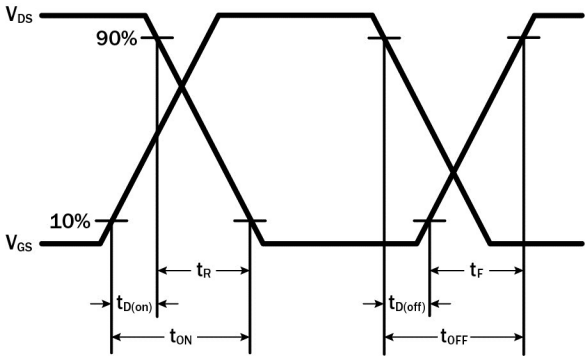



**Figure 16. Switching Time Waveform**

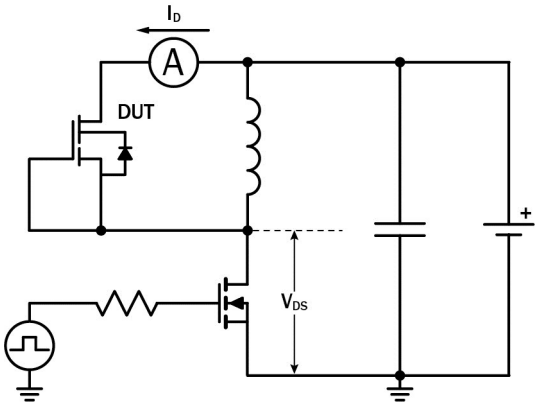



**Figure 17. Diode Characteristics Test Circuit**

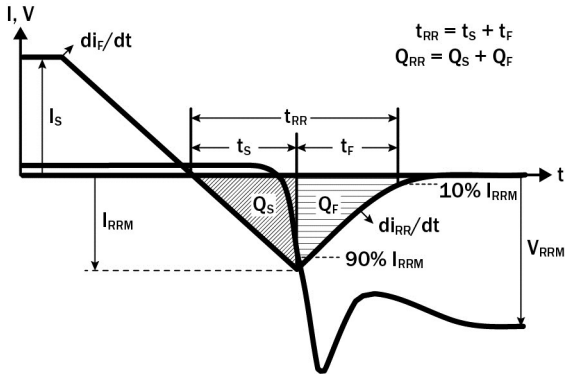



**Figure 18. Diode Recovery Waveform**

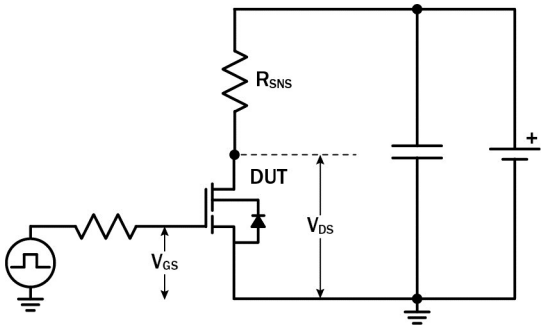



**Figure 19. Dynamic $R_{DS(on)eff}$ Test Circuit**

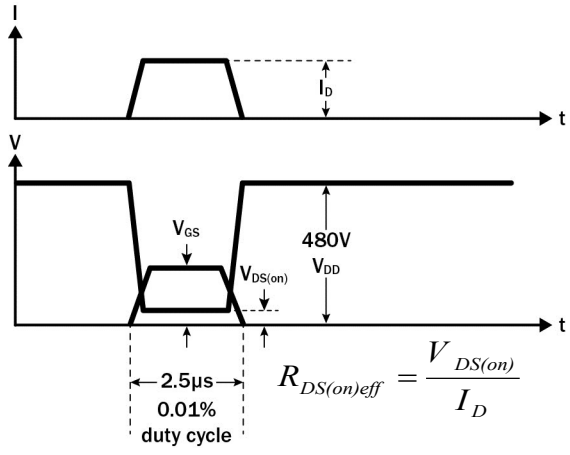



**Figure 20. Dynamic $R_{DS(on)eff}$ Waveform**



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## Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

**When Evaluating Transphorm GaN Devices:**

| DO | DO NOT |
|---|---|
| Minimize circuit inductance by keeping traces short, both in the drive and power loop | Twist the pins of TO-220 or TO-247 to accommodate GDS board layout |
| Minimize lead length of TO-220 and TO-247 package when mounting to the PCB | Use long traces in drive circuit, long lead length of the devices |
| Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points | Use differential mode probe or probe ground clip with long wire |
| See AN0003: Printed Circuit Board Layout and Probing | |

## GaN Design Resources

The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

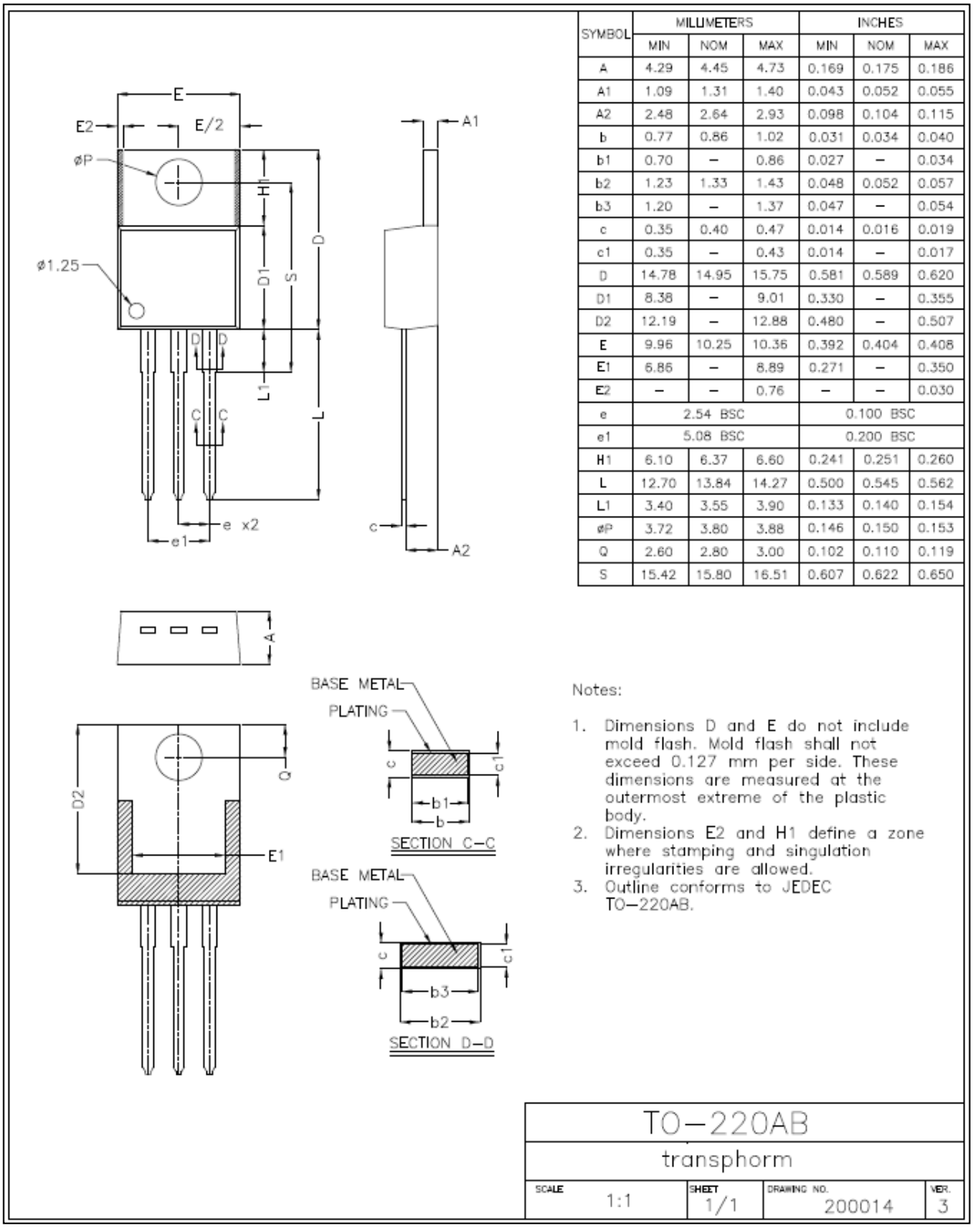


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## Mechanical

## 3 Lead TO-220 (PS) Package

Pin 1: Gate; Pin 2: Source; Pin 3: Drain, Tab: Source




| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 4.29 | 4.45 | 4.73 | 0.169 | 0.175 | 0.186 |
| A1 | 1.09 | 1.31 | 1.40 | 0.043 | 0.052 | 0.055 |
| A2 | 2.48 | 2.64 | 2.93 | 0.098 | 0.104 | 0.115 |
| b | 0.77 | 0.86 | 1.02 | 0.031 | 0.034 | 0.040 |
| b1 | 0.70 | – | 0.86 | 0.027 | – | 0.034 |
| b2 | 1.23 | 1.33 | 1.43 | 0.048 | 0.052 | 0.057 |
| b3 | 1.20 | – | 1.37 | 0.047 | – | 0.054 |
| c | 0.35 | 0.40 | 0.47 | 0.014 | 0.016 | 0.019 |
| c1 | 0.35 | – | 0.43 | 0.014 | – | 0.017 |
| D | 14.78 | 14.95 | 15.75 | 0.581 | 0.589 | 0.620 |
| D1 | 8.38 | – | 9.01 | 0.330 | – | 0.355 |
| D2 | 12.19 | – | 12.88 | 0.480 | – | 0.507 |
| E | 9.96 | 10.25 | 10.36 | 0.392 | 0.404 | 0.408 |
| E1 | 6.86 | – | 8.89 | 0.271 | – | 0.350 |
| E2 | – | – | 0.76 | – | – | 0.030 |
| e | 2.54 BSC | | | 0.100 BSC | | |
| e1 | 5.08 BSC | | | 0.200 BSC | | |
| H1 | 6.10 | 6.37 | 6.60 | 0.241 | 0.251 | 0.260 |
| L | 12.70 | 13.84 | 14.27 | 0.500 | 0.545 | 0.562 |
| L1 | 3.40 | 3.55 | 3.90 | 0.133 | 0.140 | 0.154 |
| øP | 3.72 | 3.80 | 3.88 | 0.146 | 0.150 | 0.153 |
| Q | 2.60 | 2.80 | 3.00 | 0.102 | 0.110 | 0.119 |
| S | 15.42 | 15.80 | 16.51 | 0.607 | 0.622 | 0.650 |

Notes:

1. Dimensions D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extreme of the plastic body.
2. Dimensions E2 and H1 define a zone where stamping and singulation irregularities are allowed.
3. Outline conforms to JEDEC TO–220AB.

| TO–220AB | | | |
|---|---|---|---|
| transphorm | | | |
| SCALE 1:1 | SHEET 1/1 | DRAWING NO. 200014 | VER. 3 |



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## Revision History

| Version | Date | Change(s) |
|---|---|---|
| 0 | 11/7/2016 | B version integrates bleed resistor |
| 1 | 4/19/2017 | **Updated** package drawing |
| 2 | 11/2/2017 | **Updated** Figures 11 & 12 (pg 7), effective on-resistance symbol to $R_{DS(on)eff}$ to adhere to new JEDEC standards;<br>**Added** common topology max power recommendations (pg 1), switching current values (pg 2), Circuit Implementation (pg 3), $Q_{OSS}$ value (pg 4), Figures 7 & 8 (pg 6) |



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