TLV704 24-V Input Voltage, 150-mA, Ultralow I_Q Low-Dropout Regulators

1 Features

- Wide Input Voltage Range: 2.5 V to 24 V
- Low 3.2-µA Quiescent Current
- Ground Pin Current: 3.4 µA at 100-mA I_{OUT}
- Stable With a Low-ESR, 1-µF Typical Output Capacitor
- Operating Junction Temperature: –40°C to 125°C
- Available in SOT23-5 Package
  - See *Package Option Addendum* at end of this document for complete list of available voltage options

2 Applications

- Ultralow Power Microcontrollers
- E-Meters
- Fire Alarms and Smoke Detector Systems
- Handset Peripherals
- Industrial and Automotive Applications
- Remote Controllers
- Zigbee® Networks
- Portable, Battery-Powered Equipment

3 Description

The TLV704 series of low-dropout (LDO) regulators are ultralow quiescent current devices designed for extremely power-sensitive applications. Quiescent current is virtually constant over the complete load current and ambient temperature range. These devices are an ideal power-management attachment to low-power microcontrollers, such as the MSP430.

The TLV704 operates over a wide operating input voltage of 2.5 V to 24 V. Thus, the device is an excellent choice for both battery-powered systems as well as industrial applications that undergo large line transients.

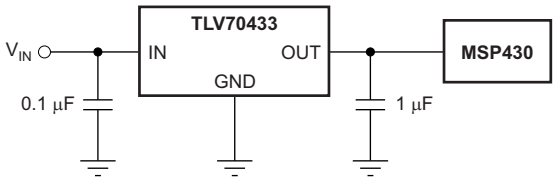
The TLV704 is available in a 3-mm × 3-mm SOT23-5 package, which is ideal for cost-effective board manufacturing.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (nom)
TLV704	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 4
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 6
6.6 Typical Characteristics ... 7
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 10
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 11
8 Application and Implementation ... 12
8.1 Application Information ... 12
8.2 Typical Application ... 12
9 Power Supply Recommendations ... 13
10 Layout ... 13
10.1 Layout Guidelines ... 13
10.2 Layout Example ... 13
10.3 Power Dissipation and Junction Temperature ... 14
10.4 Estimating Junction Temperature ... 14
10.5 Package Mounting ... 14
11 Device and Documentation Support ... 15
11.1 Device Support ... 15
11.2 Documentation Support ... 15
11.3 Trademarks ... 15
11.4 Electrostatic Discharge Caution ... 15
11.5 Glossary ... 15
12 Mechanical, Packaging, and Orderable Information ... 15

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August, 2011) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed fourth bullet in Features list ... 1
- Changed Applications list ... 1
- Changed front-page figure; removed pinout ... 1
- Changed *Pin Configuration and Functions* section; updated table format, renamed pin package to meet new standards ... 4
- Changed "free-air" to "junction" temperature in condition statement for *Absolute Maximum Ratings* ... 5
- Changed "free-air" to "junction" temperature in condition statement for *Recommended Operating Conditions* ... 5
- Deleted *Power Dissipation Rating* table ... 5
- Changed "T_A" to "T_J" in condition statement for *Electrical Characteristics* ... 6
- Changed parametric symbol for line regulation ... 6
- Changed parametric symbol for load regulation ... 6

Changes from Revision B (November, 2010) to Revision C — **Page**

- Revised document to reflect PK package option removal ... 1
- Removed SOT89 (PK) package from front-page figure ... 1
- Deleted PK package information from *Pin Functions* table ... 4
- Revised *Thermal Information* table and *Power Dissipation Rating* table ... 5
- Added load regulation specifications for $V_{OUT} \geq 3.3$ V ... 6
- Removed Figure 15 and Figure 16 ... 14

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Changes from Revision A (October, 2010) to Revision B **Page**

- Updated document to reflect availability of PK package option 1
- Corrected typo in front-page figure 1
- Changed *Pin Functions* table to correct pin numbering for PK package option 4
- Revised *Typical Characteristics* section; added and removed graphs 7
- Updated format of *Application Information* section 10

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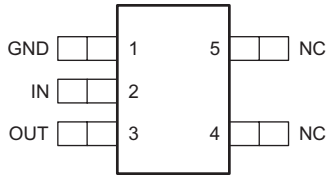
5 Pin Configuration and Functions

DBV Package
SOT-23 (5)
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground
IN	2	I	Unregulated input voltage.
OUT	3	O	Regulated output voltage. Any capacitor greater than 1 µF between this pin and ground is needed for stability.
NC	4, 5	—	Not internally connected. This pin can be left open or tied to ground for improved thermal performance.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted(1).

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	24	V
Current source	OUT	Internally limited		
Temperature	Operating junction, T_J	–40	150	°C
	Storage range, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		24	V
I_{OUT}	Output current	0		150	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV704 DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	213.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	110.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	97.4	
ψ_{JT}	Junction-to-top characterization parameter	22.0	
ψ_{JB}	Junction-to-board characterization parameter	78.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

All values are at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range					24	V
	Output voltage range			1.2		5	V
V_{OUT}	DC output accuracy			–2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{(nom)}$ + 1 V < V_{IN} < 24 V			20	50	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	V_{OUT} ≤ 3.3 V	0 mA < I_{OUT} < 10 mA		10		mV
			0 mA < I_{OUT} < 50 mA		25		
			0 mA < I_{OUT} < 100 mA		33	50	
		V_{OUT} ≥ 3.3 V	0 mA < I_{OUT} < 10 mA		7		
			0 mA < I_{OUT} < 50 mA		35		
			0 mA < I_{OUT} < 100 mA		50	75	
V_{DO}	Dropout voltage(1)	I_{OUT} = 10 mA			75		mV
		I_{OUT} = 50 mA			400		
		I_{OUT} = 100 mA			850	1100	
I_{CL}	Output current limit	V_{OUT} = 0 V		160		1000	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA			3.2	4.5	µA
		I_{OUT} = 100 mA			3.4	5.5	
PSRR	Power-supply rejection ratio	f = 100 kHz, C_{OUT} = 10 µF			60		dB
T_J	Operating junction temperature			–40		125	°C

(1) V_{IN} = $V_{OUT(nom)}$ – 0.1 V.

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6.6 Typical Characteristics

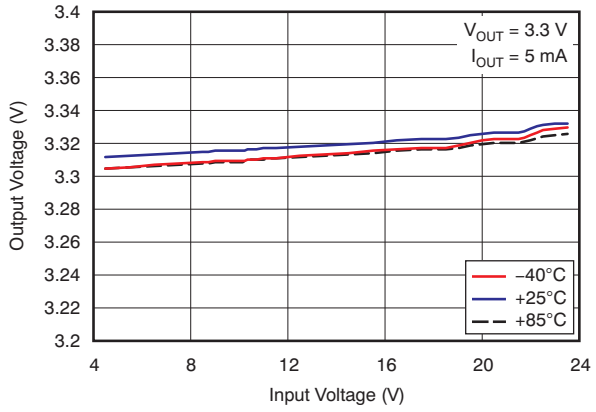

Figure 1. Line Regulation

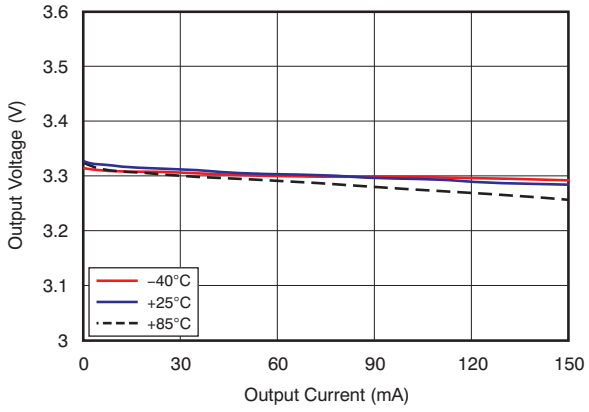

Figure 2. Load Regulation (V_{OUT} = 3.3 V)

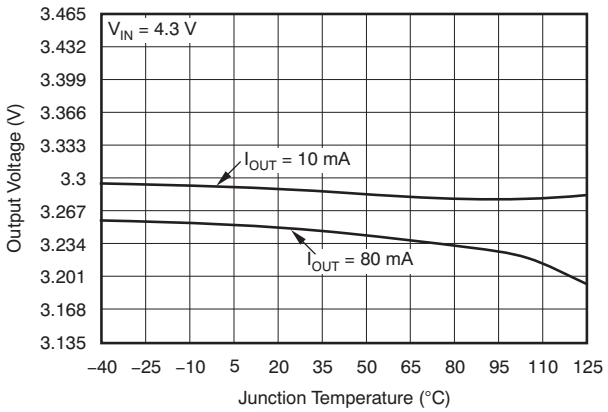

Figure 3. Output Voltage vs Junction Temperature

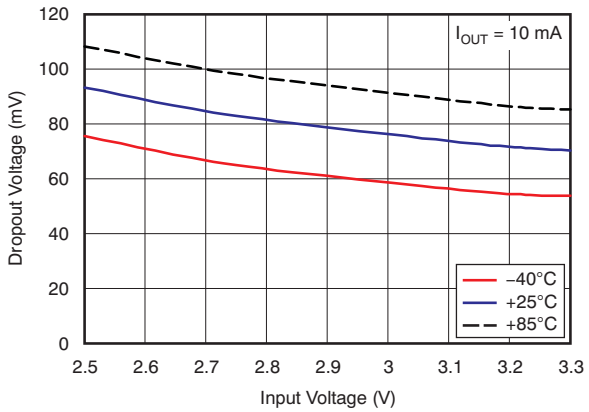

Figure 4. Dropout Voltage vs Input Voltage (TLV70433)

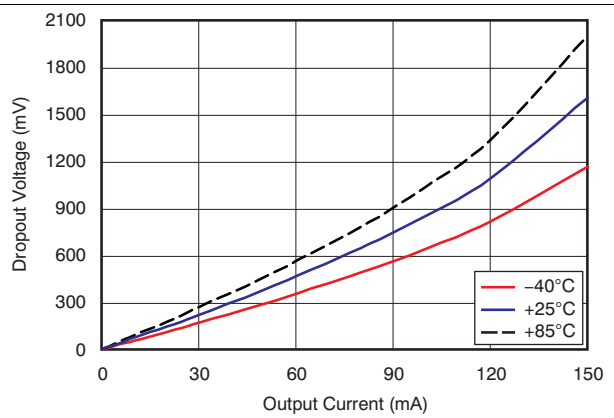

Figure 5. Dropout Voltage vs Output Current

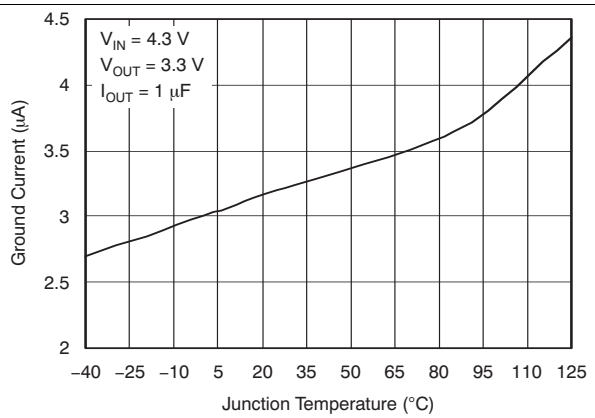

Figure 6. Ground Current vs Junction Temperature

Typical Characteristics (continued)

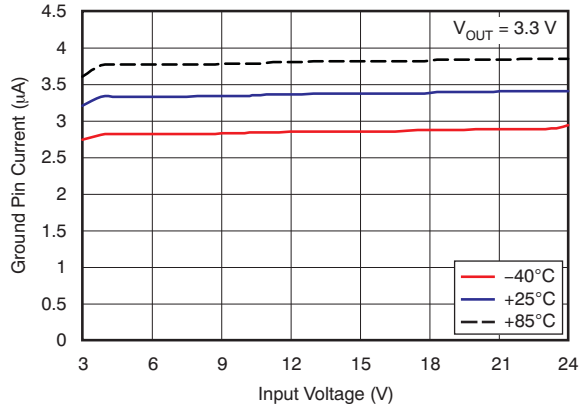

Figure 7. Ground Pin Current vs Input Voltage

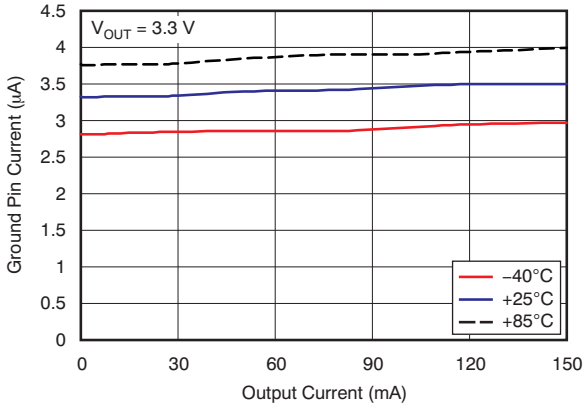

Figure 8. Ground Pin Current vs Load Current

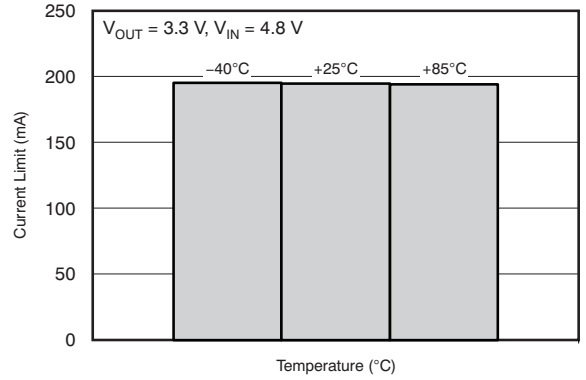

Figure 9. Current Limit vs Junction Temperature

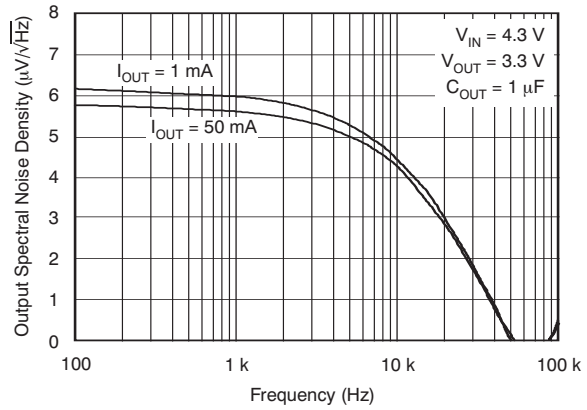

Figure 10. Output Spectral Noise Density vs Frequency

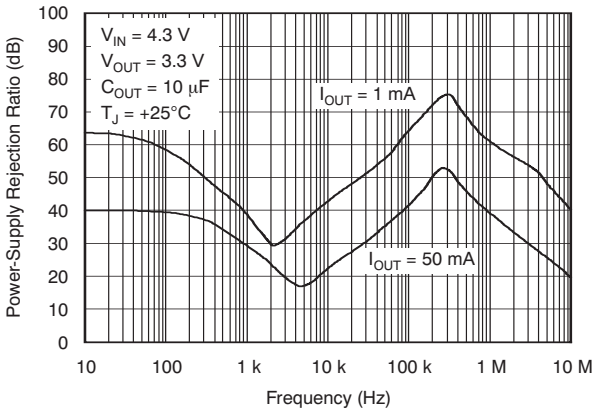

Figure 11. Power-Supply Ripple Rejection vs Frequency

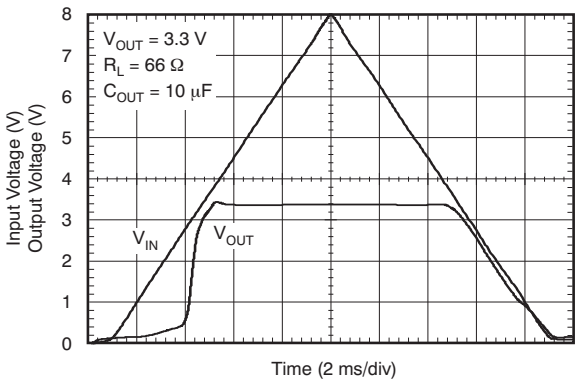

Figure 12. Power Up/Power Down

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Typical Characteristics (continued)

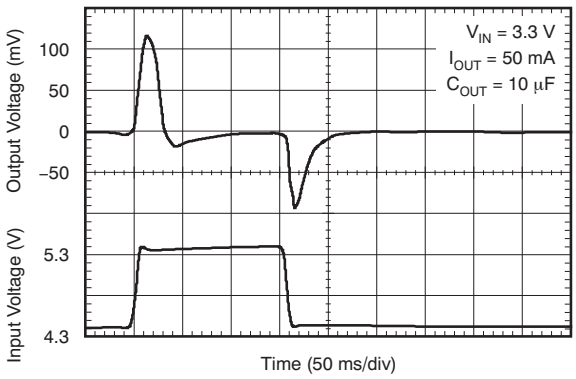


Figure 13. Line Transient Response

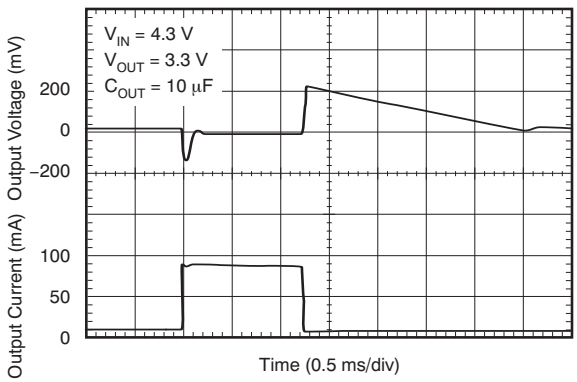


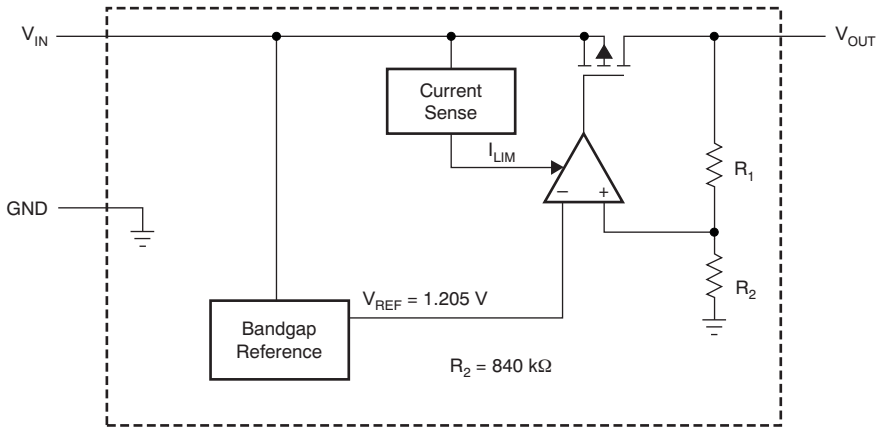
Figure 14. Load Transient Response

7 Detailed Description

7.1 Overview

The TLV704 series belong to a family of ultralow I_Q LDO regulators. I_Q remains fairly constant over the complete output load current and temperature range. The devices are ensured to operate over a temperature range of –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Regulator Protection

The TLV704 series of LDO regulators use a PMOS-pass transistor that has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting is appropriate.

The TLV704 features internal current limiting. During normal operation, the TLV704 limits output current to approximately 250 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Do not exceed the rated maximum operating junction temperature of 125°C. Continuously running the device under conditions where the junction temperature exceeds 125°C degrades device reliability.

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

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7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The output current is less than the current limit.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout mode	$V_{IN} < V_{OUT\ (nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV704 family of LDOs are designed for power-sensitive applications and feature low quiescent current. These devices pair well with low-power microcontrollers, such as the MSP430.

8.2 Typical Application

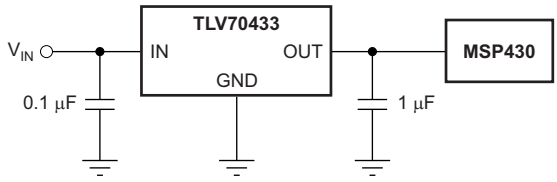

Figure 15. Typical Application

8.2.1 Design Requirements

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

The TLV704 requires a 1-µF or larger capacitor connected between OUT and GND for stability. Ceramic or tantalum capacitors can be used. Larger value capacitors result in better transient and noise performance.

Although an input capacitor is not required for stability, when a 0.1-µF or larger capacitor is placed between IN and GND, it counteracts reactive input sources and improves transient and noise performance. Higher value capacitors are necessary if large, fast rise time load transients are anticipated.

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Typical Application (continued)

8.2.3 Application Curves

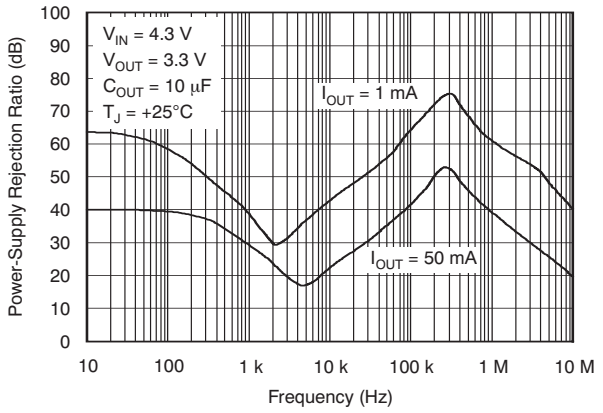

Figure 16. Power-Supply Ripple Rejection vs Frequency

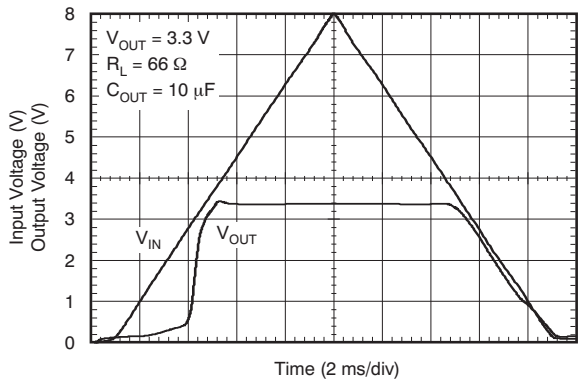

Figure 17. Power Up/Power Down

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV704. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To avoid interference of noise and ripple on the board, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the ground connection for the output capacitor should be connected directly to the device GND pin.

10.2 Layout Example

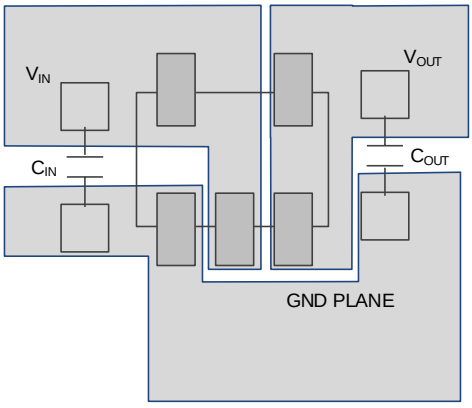

Figure 18. Layout Example for the DBV Package

10.3 Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using Equation 1:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}} \quad (1)$$

where:

T_{Jmax} is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table).

T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

10.4 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO while in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with Equation 3.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \quad (3)$$

where:

- P_D is the power dissipated as explained in *Thermal Information*
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge.

10.5 Package Mounting

Solder pad footprint recommendations for the TLV704 are available from the TI's website at www.ti.com through the TLV704 series product folders. The recommended land pattern for the DBV package is appended to this data sheet.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV704. The TLV70433DBVEVM-712 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Table 2. Available Options(1)

PRODUCT	V_{OUT}
TLV704**xxyyyz**	**xx** is nominal output voltage (for example 33 = 3.3 V) **yyy** is Package Designator **z** is Package Quantity

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

- *TLV70433DBVEVM-712, TLV70433PKEVM-712 Evaluation Modules*, SBVU017

11.3 Trademarks

Zigbee is a registered trademark of ZigBee Alliance.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70430DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUQ	Samples
TLV70430DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QUQ	Samples
TLV70433DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAO	Samples
TLV70433DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAO	Samples
TLV704345DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	13T	Samples
TLV704345DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	13T	Samples
TLV70436DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAW	Samples
TLV70436DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAW	Samples
TLV70450DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAX	Samples
TLV70450DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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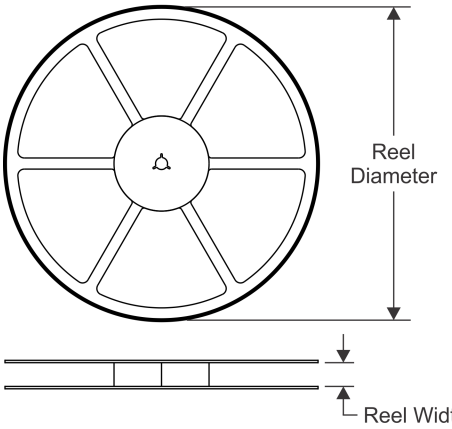
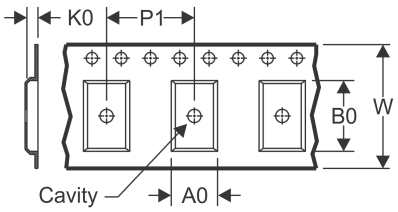
TAPE AND REEL INFORMATION

REEL DIMENSIONS

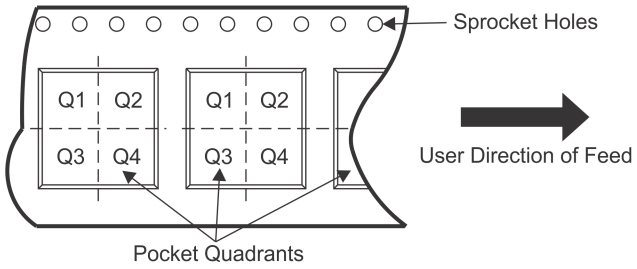


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

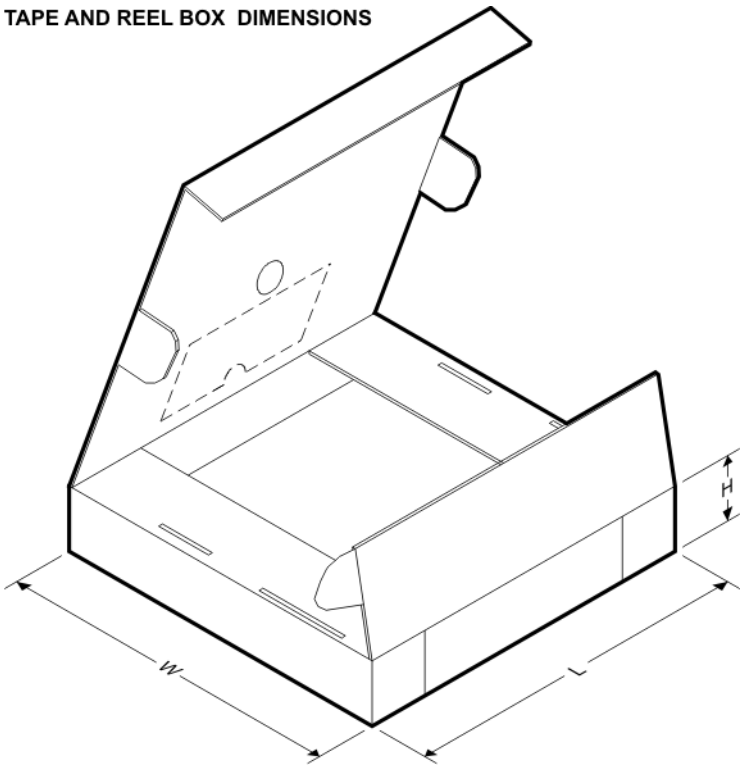
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70430DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70430DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70433DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70433DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70436DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70436DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV70450DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV70450DBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3

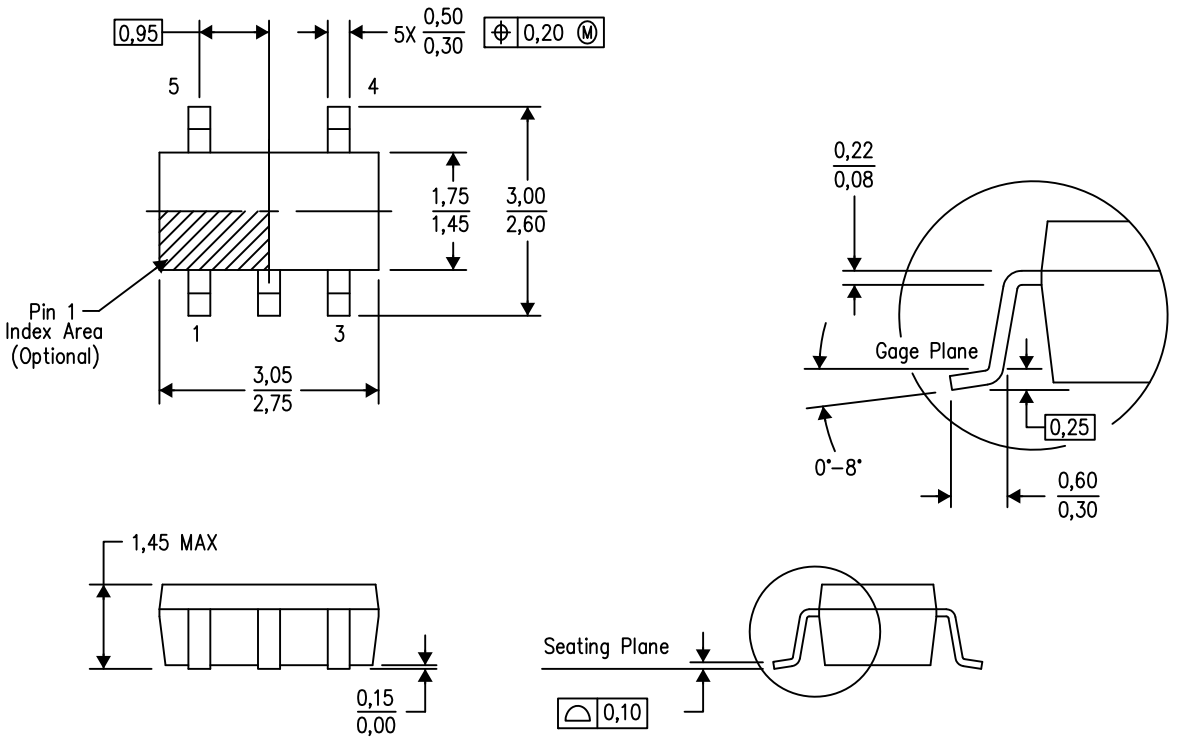
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70430DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70430DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70433DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70433DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70436DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70436DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV70450DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV70450DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

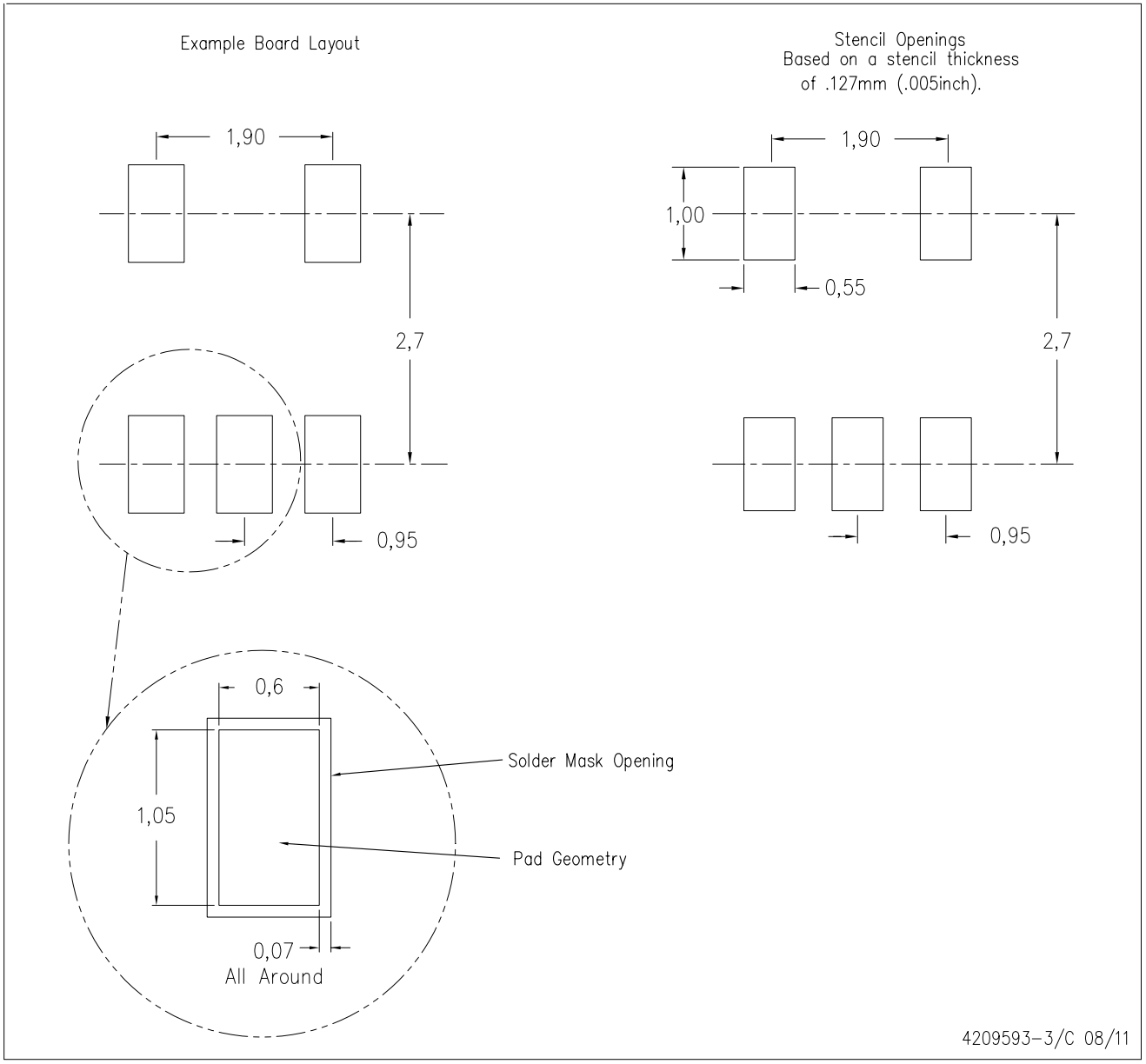
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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