LOW EMI CURRENT SENSE HIGH SIDE SWITCH

Features

- Suitable for 12V systems
- Over current shutdown
- Over temperature shutdown
- Current sensing
- Repetitive avalanche robustness
- Low quiescent current
- Reverse battery protection
- ESD protection
- Optimized Turn On/Off for EMI
- Lead-Free, Halogen-Free, RoHS compliant

Product Summary

Rds(on)	3.9 mΩ typ.
Current Ratio	6200
Ishutdown	60A min.
Vbr	35V typ.

Applications

- Glow plug
- PTC
- Seat heater
- Relay replacement

Package



DPak – 5Leads

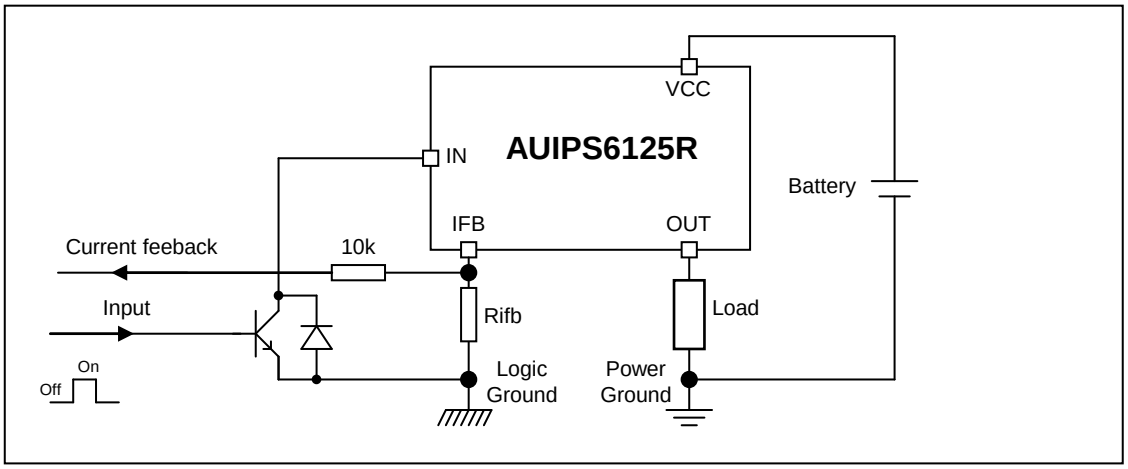
Description

The AUIPS6125R is a fully protected four terminals high side switch. It features current sensing, over-current, over-temperature, and ESD protections. Shutdown type of protection provides a good reliability under short circuit condition. The Ifb pin provides both an analog feedback during normal operation and a digital flag when the part is in protection mode.

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIPS6125R	D-Pak-5-Leads	Tape and reel left	3000	AUIPS6125RTRL

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (Tambient=25°C unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
Vcc-Vin	Maximum Vcc voltage	-16	65	V
Vcc-Vifb	Maximum Ifb voltage	-0.3	65	
Vcc-Vout	Maximum output voltage	-0.3	29	
Pd	Maximum power dissipation Rth=22°C/W Tambient=25°C	—	5.7	W
Tj max.	Maximum operating junction temperature	-40	150	°C
	Maximum storage temperature	-55	150	
Ifb max.	Max. Ifb current	-50	50	mA
EAS	Inductive load switch-off energy (single pulse) Vcc=13.5V, Iload=25A,Tj≤150 °C	—	400	mJ
Fmax.	Maximum operating frequency, Vcc<18V. See page 9	—	50	Hz
Tfall In	Maximum falling time on the input pin during the turn on	—	2	µs

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
Rth1	Thermal resistance junction to ambient DPak Std footprint	70	—	°C/W
Rth2	Thermal resistance junction to ambient DPak -2s2p (1)	22	—	
Rth3	Thermal resistance junction to case DPak	1.2	—	

(1) Specified according to Jedec51-2,-5,-7 at natural convection on FR4 2s2p board. The product (Chip+Package) was simulated on a 76.2x114.3x1.5mm board with 2 inner copper layers(2x70mm Cu, 2x35mm Cu). Where applicable a thermal via array under exposed pad contacted the first inner copper layer.

Recommended Operating Conditions

These values are given for a quick design.

Symbol	Parameter	Min.	Max.	Units
Iout	Continuous output current	—	19	A
	Tambient=85°C, Rth=22°C/W, Tj=150°C			

Static Electrical Characteristics

Tj=-40°C..150°C, Vcc=6..18V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Vcc op.	Operating voltage range	5.8	—	18	V	
Rds(on)	ON state resistance Tj=25°C	—	3.9	—	mΩ	Ids=10A
	ON state resistance Tj=150°C(2)	—	6	8		
Icc off	Supply leakage current	—	1	3	µA	Vin=Vcc=14V,Vifb=Vgnd Vout=Vgnd, Tj=25°C
Iout off	Output leakage current	—	1	3		
Iin on	Input current when device on	1	2.7	6	mA	Vcc-Vin=14V
Vbr	Vcc to Vout breakdown voltage	30.5	35	50	V	Tj=25°C, Id=10mA
		35	39	55		Tj=150°C, Id=10mA
Vih (3)	High level Input threshold voltage	4.5	5.4	6.2		Id=20mA
Vil (3)	Low level Input threshold voltage	4	5	5.8		
Rds(on) rev	Reverse On state resistance Tj=25°C	—	4	7	mΩ	Isd=10A, Vin-Vcc>8V
Vf	Forward body diode voltage Tj=25°C	—	0.8	0.9	V	If=10A
	Forward body diode voltage Tj=125°C	—	0.6	0.8		
Rin	Input resistor	115	200	300	Ω	Built-in

(2) Guaranteed by design

(3) Input thresholds are measured directly between the input pin and the tab.

Switching Electrical Characteristics

Vcc=14V, Resistive load=1Ω, Tj=25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
tdon	Turn on delay time	5	40	150	µs	See fig. 1
Tr	Rise time from 20% to 80% of Vcc	5	15	45		
tdoff	Turn off delay time	20	110	200		
Tf	Fall time from 80% to 20% of Vcc	5	15	45		

Protection Characteristics

Tj=-40°C..150°C, Vcc=6..18V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Tsd	Over temperature threshold(2)	150	165	—	°C	See fig. 3
Isd	Over-current shutdown	60	90	120	A	See fig. 3 and page 6
I fault	Ifb after an over-current or an over-temperature (latched)	9	20	27	mA	See fig. 3, Vcc-Vifb>4V
Psd_rst	Time to reset Psd	—	26	—	ms	See page 8
Psd_UV	Time to shut down when Vcc-Vin<Vil	0.01	0.06	0.2		
I in rst	Input current to reset the protection	40	—	—	µA	
Vin reset	Input voltage between Vcc and Vin to Reset the latch	0.8	1.8	3	V	
T reset		6	—	200	µs	See figure 3

(2) Guaranteed by design

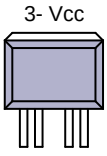
Current Sensing Characteristics

Tj=-40°C..150°C, Vcc=6..18V (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ratio	I load / Ifb current ratio	5000	6200	7600		Iload=60A at Vcc=14V / Vcc-Vifb>5V Iload=30A at Vcc=6V/ Vcc-Vifb>3.5V After 2ms, See page 7
Ratio_Cold	Ratio drift between 25°C to -40°C	-3	-0.8	1	%	Ratio@-40°/Ratio@25°
Ratio_Hot	Ratio drift between 25°C to 125°C	-0.5	2.3	5		Ratio@125°/Ratio@25°
I offset	Load current offset	-0.15	0	0.15	A	After 2ms

Lead Assignments

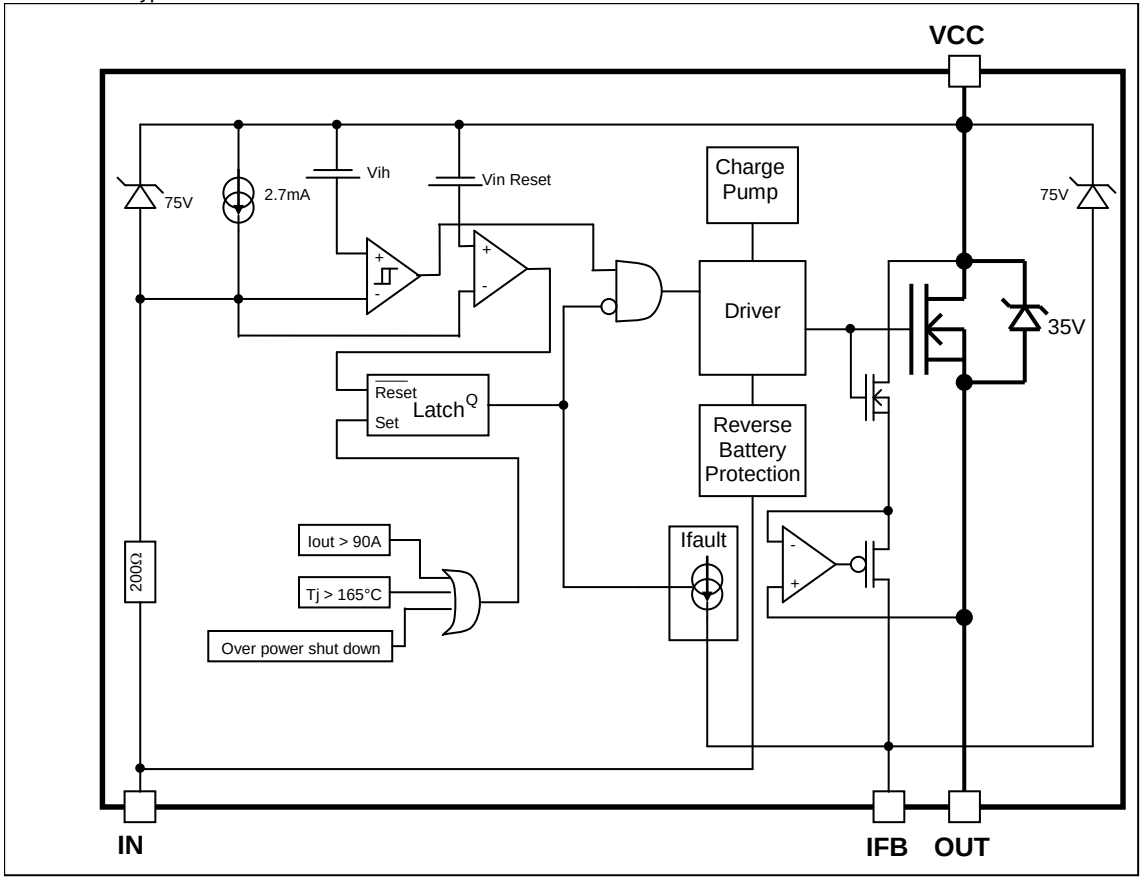
1- In
2- Ifb
3- Vcc
4- Out
5- Out



DPak

Functional Block Diagram

All values are typical



Truth Table

Op. Conditions	Input	Output	Ifb pin voltage
Normal mode	H	L	0V
Normal mode	L	H	I load x Rfb / Ratio
Open load	H	L	0V
Open load	L	H	Ifb leakage x Rifb
Short circuit to GND	H	L	0V
Short circuit to GND	L	L	I fault x Rifb(latched)
Over temperature	H	L	0V
Over temperature	L	L	I fault x Rifb (latched)

Operating voltage

Maximum Vcc voltage : this is the maximum voltage before the breakdown of the IC process.
Operating voltage : This is the Vcc range in which the functionality of the part is guaranteed. The AEC-Q100 qualification is run at the maximum operating voltage specified in the datasheet.

Reverse battery

During the reverse battery the Mosfet is turned on if the input pin is powered with a diode in parallel of the input transistor.
Power dissipation in the IPS : P = Rdson rev * I load² + Vcc² / 200ohm (internal input resistor).
If the power dissipation is too high in Rifb, a diode in serial can be added to block the current.

Repetitive Avalanche

The AUIR6125R demagnetizes inductive load energy by clamping the output voltage into the body diode of the Power Mosfet.
The temperature increase during Avalanche clamp can be estimated as follows:

$$\Delta_{Tj} = P \cdot Z_{TH}(t_{AVALANCHE})$$

Where: $Z_{TH}(t_{AVALANCHE})$ is the thermal impedance at t_{CLAMP} and can be read from the thermal impedance curves given in the data sheets.

$P = Vbr \cdot I$: Power dissipation during avalanche clamp

$I_{CLAMP_AVERAGE} = \frac{I_{CLAMP}}{2}$: Average current during avalanche clamp

$t_{CL} = \frac{I_{CL}}{\left|\frac{di}{dt}\right|}$: Avalanche clamp duration

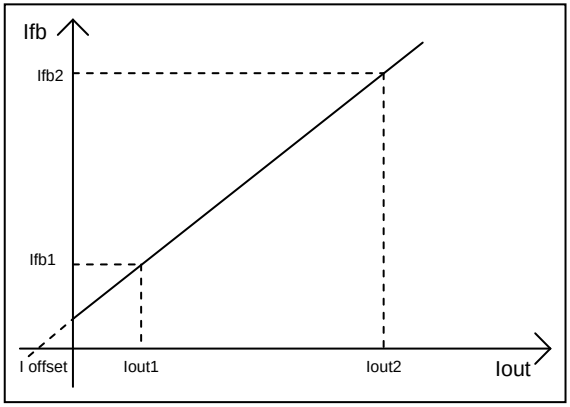
$\frac{di}{dt} = \frac{V_{Battery} - VBR}{L}$: Demagnetization current

Figure 9 gives the maximum inductance versus the load current in the worst case: the part switches off after an over temperature detection. If the load inductance exceeds the curve, a freewheeling diode is required.

Over-current protection

The threshold of the over-current protection is set in order to guarantee that the device is able to turn on a load with an inrush current lower than the minimum of Isd. Nevertheless for high current and high temperature the device may switch off for a lower current due to the over-temperature protection. This behavior is shown in Figure 10.

Current sensing accuracy



The current sensing is specified by measuring 3 points :
- Ifb1 for Iout1
- Ifb2 for Iout2
- Ifb leakage for Iout=0

The parameters in the datasheet are computed with the following formula :
Ratio = (Iout2 – Iout1)/(Ifb2 – Ifb1)
I offset = Ifb1 x Ratio – Iout1

This allows the designer to evaluate the Ifb for any Iout value using :
Ifb = (Iout + I offset) / Ratio if Iout > I Offset

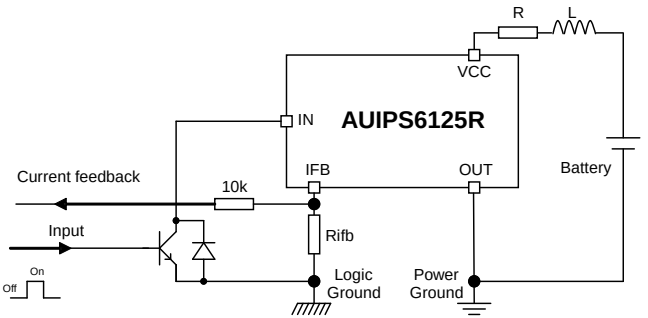
For some applications, a calibration is required. In that case, the accuracy of the system will depends on the variation of the I offset and the ratio over the temperature range. The ratio variation is given by Ratio_Hot and Ratio_Cold specified in page 4.
The Ioffset variation depends directly on the Rdson:
I offset@-40°C= I offset@25°C / 0.73
I offset@150°C= I offset@25°C / 1.6

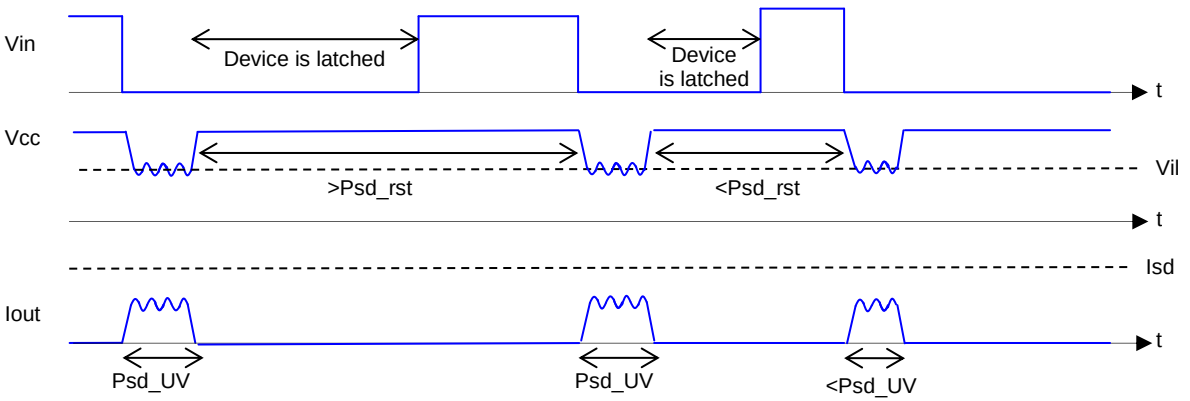
Over Power Shut Down protection

The AUIPS6125R integrates an over-power protection in order to limit the thermal stress in the Mosfet during certain conditions like under voltage or high frequency. This protection is activated only when the part turns ON.
The internal capacitor is discharge with an internal constant (Psd_rst).

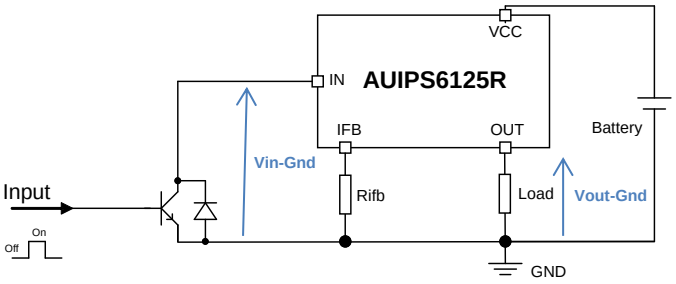
Case 1:

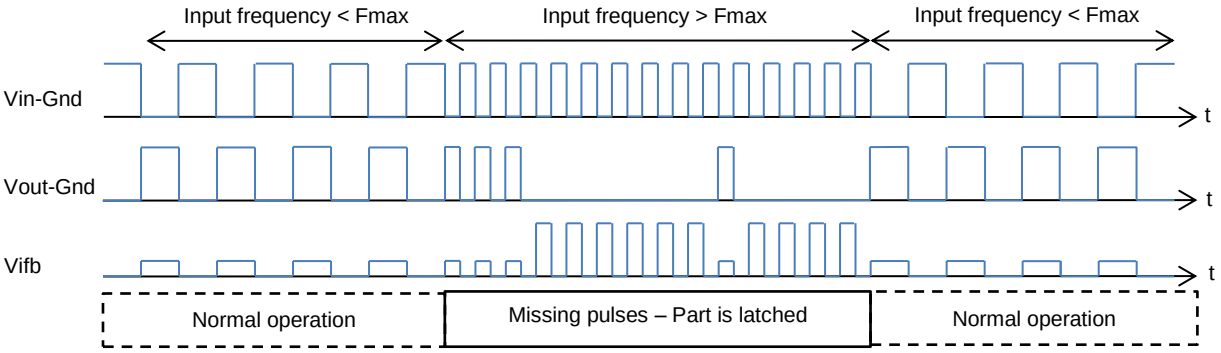
Typical in low voltage condition with a short circuit on the output, the voltage on the Vcc pin will oscillate around the under voltage protection and the output current may not reach the 'over-current shut down' threshold.
To prevent thermal stress of the device, the 'Over power shut down' protection will turn off the part after the time 'Psd_UV' and the part is latched off.





Case 2:
If the input frequency is larger of the parameter ‘Fmax’, the 'Over power shut down' protection will limit numbers of switching to limit power dissipation.





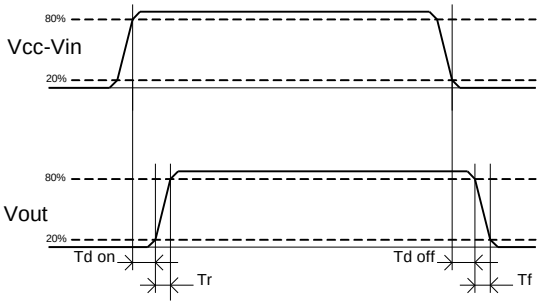


Figure 1 – IN rise time & switching definitions

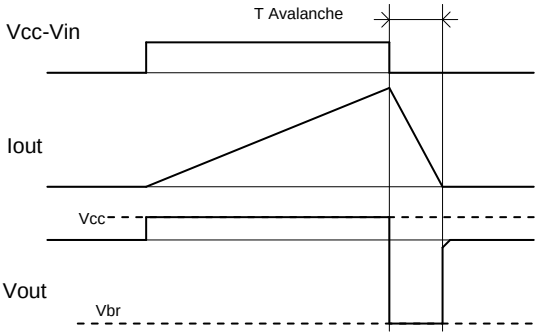


Figure 2 – Avalanche waveforms

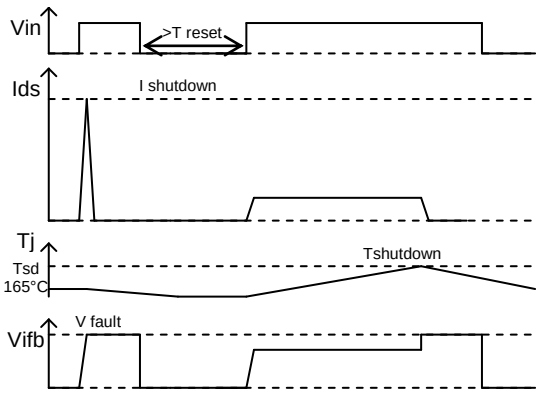


Figure 3 – Protection timing diagram

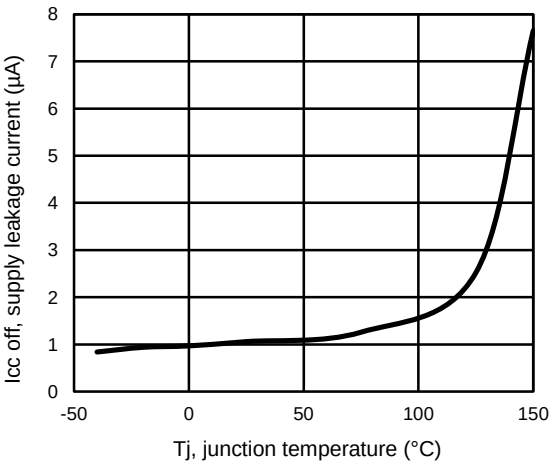


Figure 4 – Icc off (µA) Vs Tj (°C)

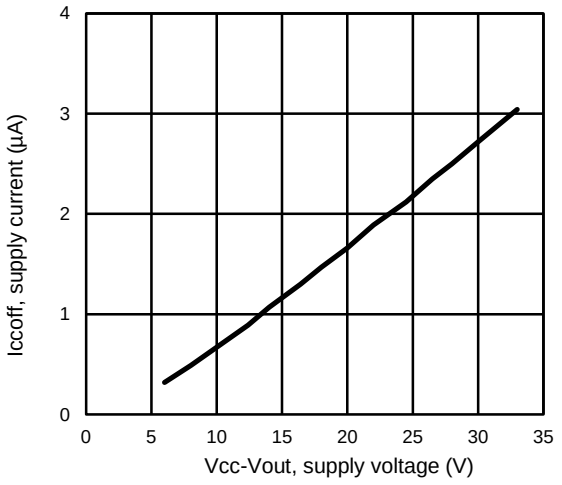


Figure 5 – Icc off(µA) Vs Vcc-Vout (V)

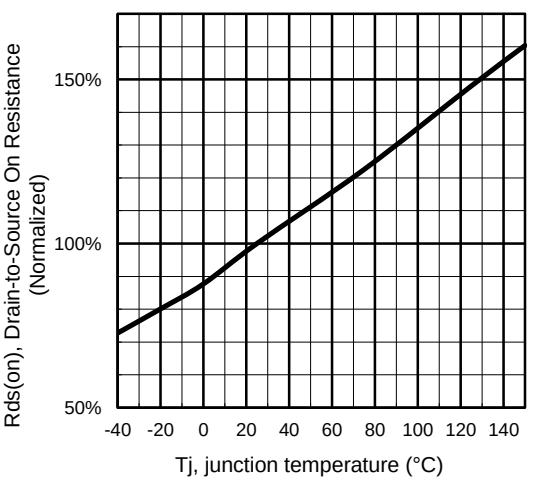


Figure 6 - Normalized Rds(on) (%) Vs Tj (°C)

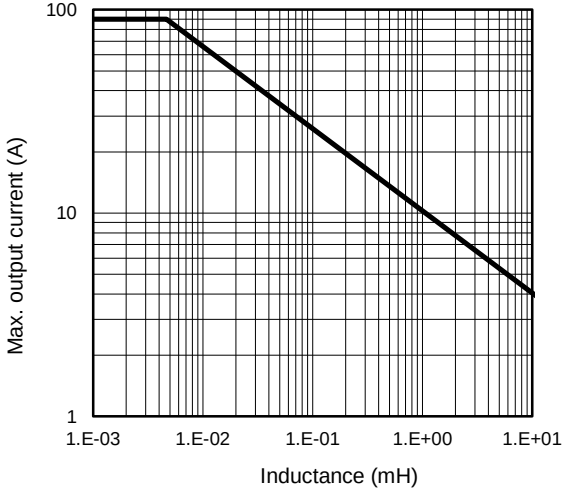


Figure 7 – Max. Iout (A) Vs inductance (mH)

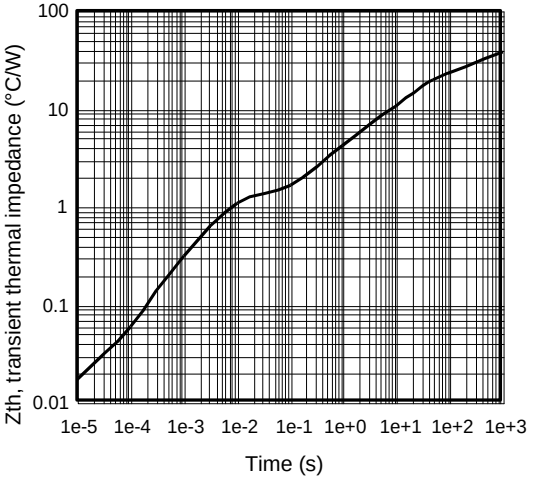


Figure 8 – Transient thermal impedance (°C/W) Vs time (s)

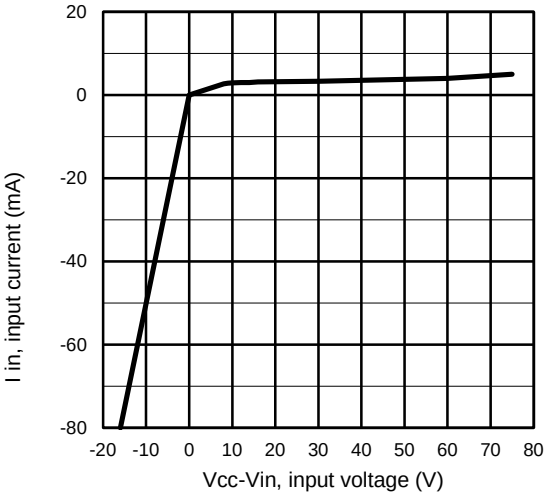


Figure 9 – I in Vs Vcc-Vin

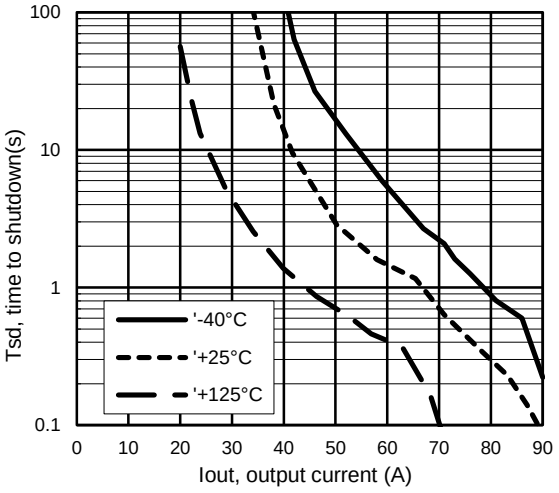
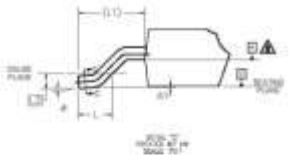
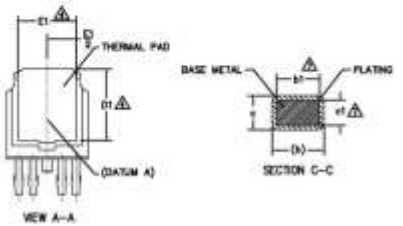
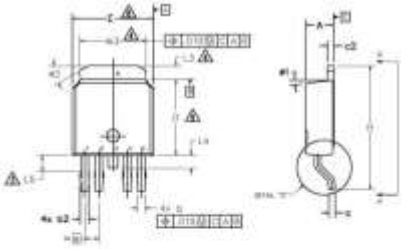


Figure 10 – Tsd (s) Vs I out (A)
SMD with 6cm²

Case Outline 5 Lead – DPAK







SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.56	0.79	.022	.031	
b1	.056	0.74	.022	.029	2
b2	0.65	0.89	.026	.035	
b3	4.95	5.46	.195	.215	2
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	2
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	–	.205	–	
E	6.35	6.73	.250	.265	3
E1	4.32	–	.170	–	
e	1.14 BSC		.045 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	28°	32°	28°	32°	

NOTES:

1.– DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.– LEAD DIMENSION UNCONTROLLED IN L5.

4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.

6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

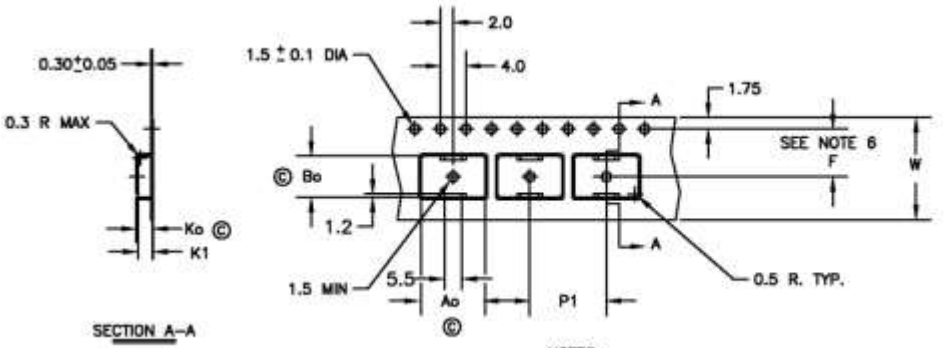
7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.

8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252.

10. LEADS AND DRAIN ARE PLATED WITH 100% Sn

Tape & Reel 5 Lead – DPAK

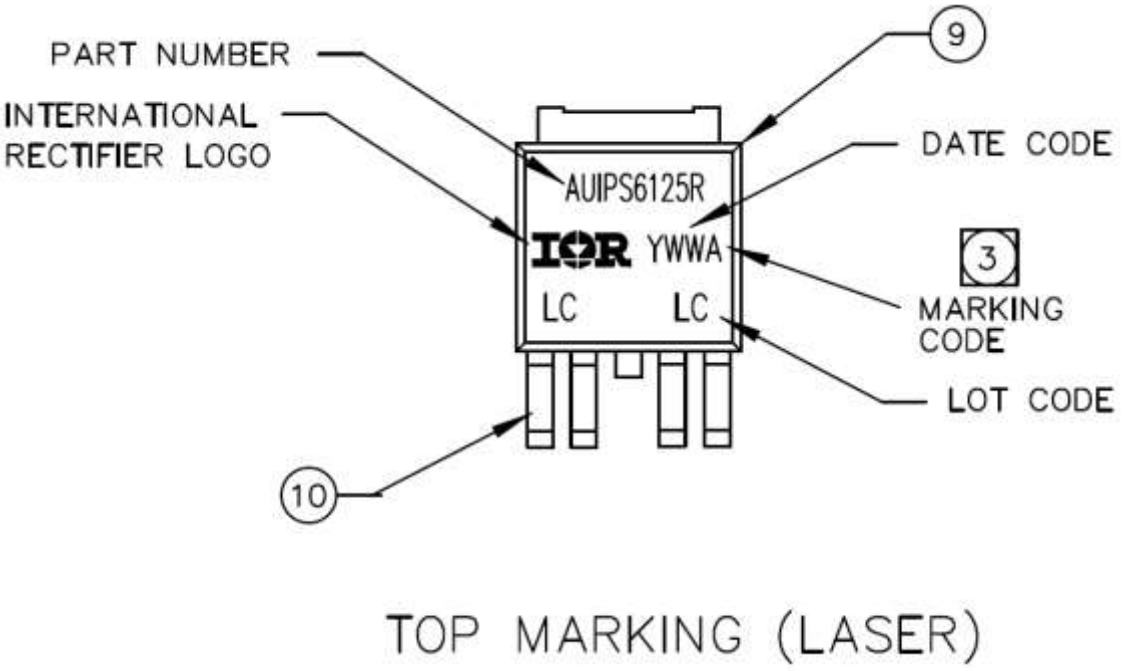


Ao = 10.5 mm
Bo = 7.0 mm
Ko = 2.8 mm
K1 = 2.4 mm
F = 7.5 mm
P1 = 12.0 mm
W = 16.0 ± .3 mm

NOTES:

1. 10 SPROCKET HOLE PUNCH CUMULATIVE TOLERANCE ±.02
2. CAMBER NOT TO EXCEED 1mm IN 100mm
3. MATERIAL: CONDUCTIVE BLACK POLYSTYRENE
4. Ao AND Bo MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
5. Ko MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
6. POCKET POSITION RELATIVE TO THE SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
7. VENDOR: (OPTIONAL)
8. MUST ALSO MEET REQUIREMENTS OF EIA STANDARD #EIA–481A, TAPING OF SURFACE–MOUNT COMPONENTS FOR AUTOMATIC PLACEMENT.
9. TOLERANCE TO BE MANUFACTURER STANDARD
10. SURFACE RESISTIVITY OF MOLDED MATL: MUST MEASURE LESS THAN OR EQUAL TO 10^{8} OHMS PER SQUARE. MEASURED IN ACCORDANCE TO PROCEDURE GIVEN IN ASTM D–257 & ASTM D–991 (REF. C–9000 SPEC.)
11. TOTAL LENGTH PER REEL MUST BE 79 METERS
12. © CRITICAL DIMENSION

Part Marking Information



Qualification Information

Qualification Level		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		DPAK-5L	MSL3, 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M3 (+/-300V) (per AEC-Q100-003)	
	Human Body Model	Class 2 (+/-3500V) (per AEC-Q100-002)	
	Charged Device Model	Class C6 (+/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II Level A (per AEC-Q100-004)	
RoHS Compliant		Yes	

Published by
Infineon Technologies AG
81726 München, Germany
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Revision History

Revision	Date	Notes/Changes
A	April 6, 2016	Initial release
Rev 1.1	June 8, 2016	Add treset min page 4 Add Ratio vs temp page 4 Change Psd diagram page 8 Add part marking
Rev 1.2	July 28, 2016	Remove 'Tube' in Ordering information
Rev 1.3	November 8, 2016	Update page 'Current sensing accuracy': I offset@-40°C= I offset@25°C / 0.73 I offset@150°C= I offset@25°C / 1.6