

S73WS-P based MCP Products

**1.8 Volt-only x16 Simultaneous Read/Write,
Burst Mode Flash
Mobile SDRAM on Shared Bus**



***Data Sheet** (Advance Information)*

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When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spanion LLC applies the following conditions to documents in this category:

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S73WS-P based MCP Products

1.8 Volt-only x16 Simultaneous Read/Write, Burst Mode Flash Mobile SDRAM on Shared Bus



Data Sheet (Advance Information)

Features

- Power supply voltage of 1.7 to 1.95V
- Flash access time: 80 ns for NOR Flash
- Flash burst frequencies: 66 MHz, 80 MHz, 108 MHz
- Mobile SDRAM burst frequency: 104 MHz (SDR)
- Package:
 - 9.0 x 12.0 mm MCP
- Operating Temperature
 - –25°C to +85°C (wireless)

The S73WS series is a product line of stacked packages and consists of:

- One NOR flash memory die
- One Mobile SDRAM die on shared bus

The products covered by this document are listed in the table below.

Device	DRAM Density
	128Mb
S29WS256P	S73WS256PD0 (MCP) (SDR)

Note:

For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

For detailed specifications, please refer to the individual data sheets.

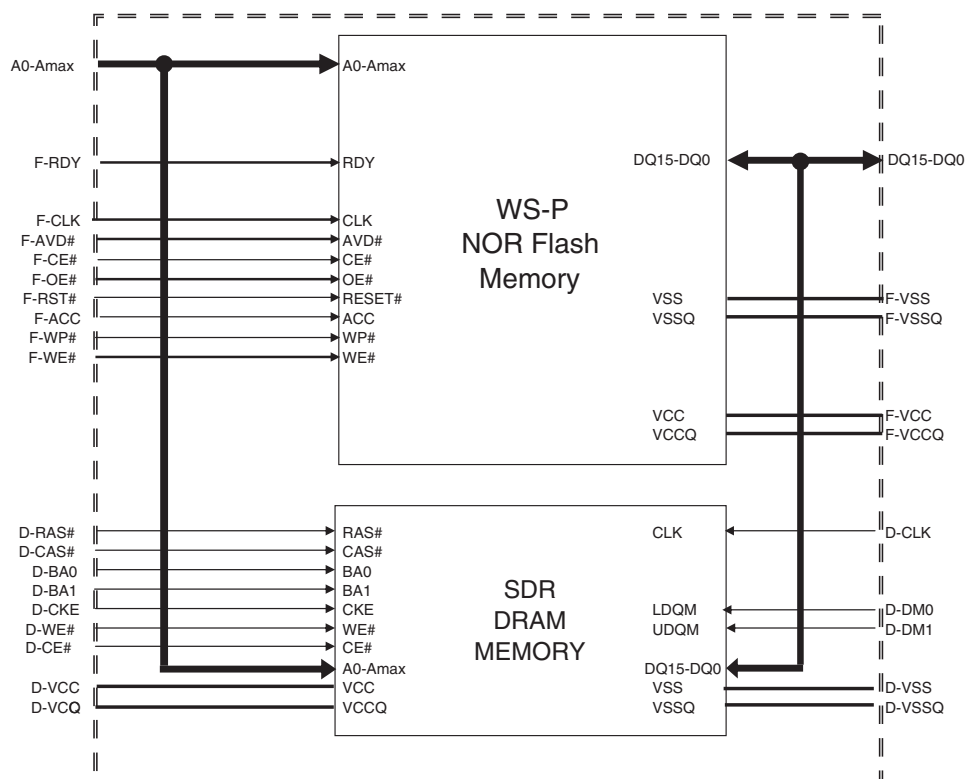
Document	Publication Identification Number (PID)
S29WS-P	S29WS-P_00
128 Mb Mobile SDR-DRAM Type 5	SDRAM_08

1. Product Selector Guide

Device	NOR Flash Density	NOR Flash Speed	DRAM Density	DRAM Speed	DRAM Supplier	Package
S73WS512PD0HF64V	512 Mb	66 MHz	128 Mb	104 MHz (SDR)	Type 5	MCP 9 x 12 mm

2. MCP Block Diagram

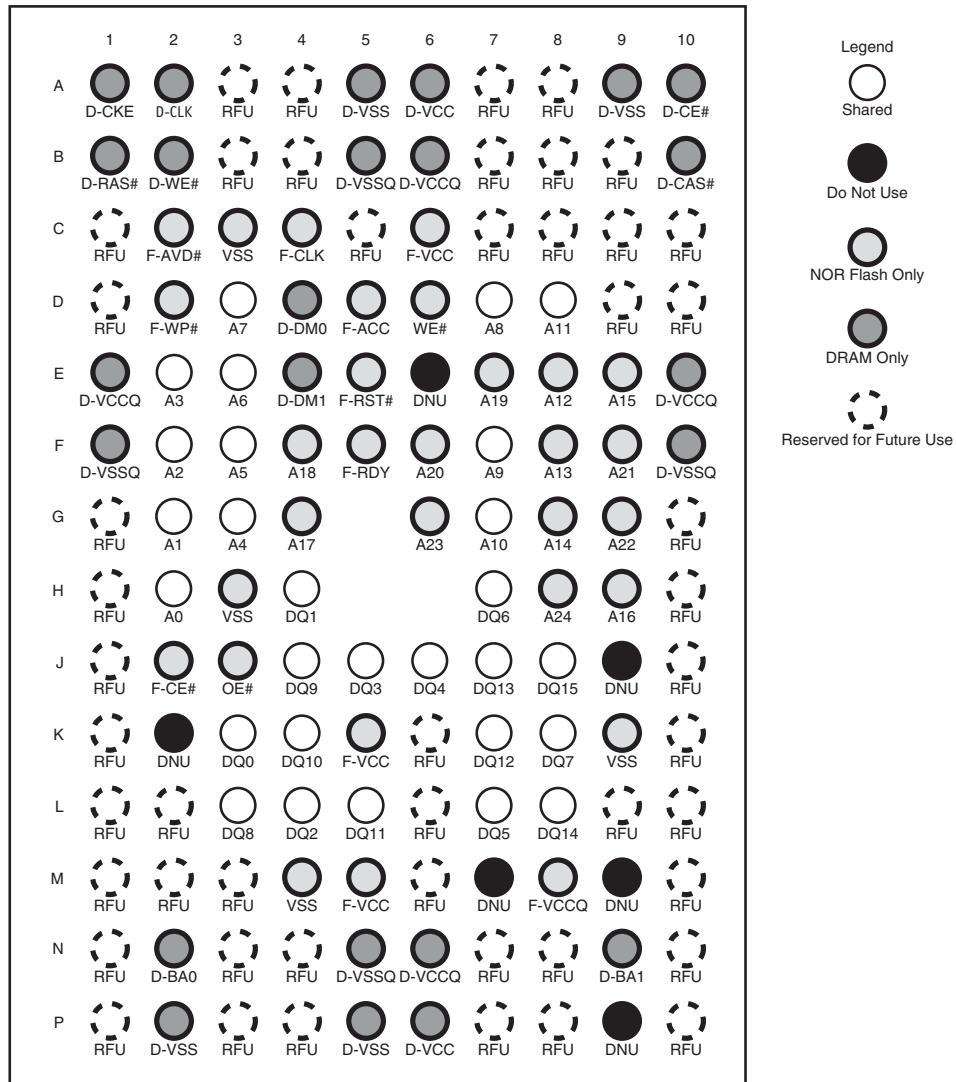
2.1 NOR Flash + DRAM MCPs



3. Connection Diagrams

3.1 512 Mb NOR Flash with 128 Mb SDR-DRAM

137-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Note: DDR-only signals are RFUs in the case of the SDR DRAM-based solutions.

3.1.0.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

3.2 NOR Flash and DRAM Input/Output Descriptions

Amax-A0	=	Address inputs, shared between NOR Flash and DRAM
DQ15-DQ0	=	Data input/output, shared between NOR Flash and DRAM
F-CE#	=	NOR Flash Chip-enable input. Asynchronous relative to CLK for Burst Mode.
F-OE#	=	NOR Flash Output Enable input. Asynchronous relative to CLK for Burst mode.
F-WE#	=	NOR Flash Write Enable input.
F-V _{CC}	=	NOR Flash device power supply (1.7 V - 1.95V).
F-V _{CCQ}	=	Input/Output Buffer power supply.
V _{SS}	=	Ground
RFU	=	Reserved for Future Use
F-RDY	=	Flash ready output. Indicates the status of the Burst read. VOL = data valid.
F-CLK	=	NOR Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
F-AVD#	=	NOR Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. VIL = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. VIH = device ignores address inputs
F-RST#	=	NOR Flash hardware reset input. VIL = device resets and returns to reading array data
F-WP#	=	NOR Flash hardware write protect input. VIL = disables program and erase functions in the four outermost sectors.
F-ACC	=	NOR Flash accelerated input. At VHH, accelerates programming; automatically places device in unlock bypass mode. At VIL, disables all program and erase functions. Should be at VIH for all other conditions.
D-CE#	=	SDRAM Chip Select
D-CKE	=	SDRAM Clock Enable
D-BA1-BA0	=	SDRAM Bank Select
D-RAS#	=	SDRAM Row Address Strobe
D-CAS#	=	SDRAM Column Address Strobe
D-DM1-D-DM0	=	SDRAM Data Input/Output Mask
D-WE#	=	SDRAM Write Enable input
D-V _{SS}	=	SDRAM Ground
D-V _{SSQ}	=	SDRAM Input/Output Buffer ground
D-V _{CCQ}	=	SDRAM Input/Output Buffer power supply
D-V _{CC}	=	SDRAM device power supply

4. Ordering Information

The order number is formed by a valid combinations of the following:

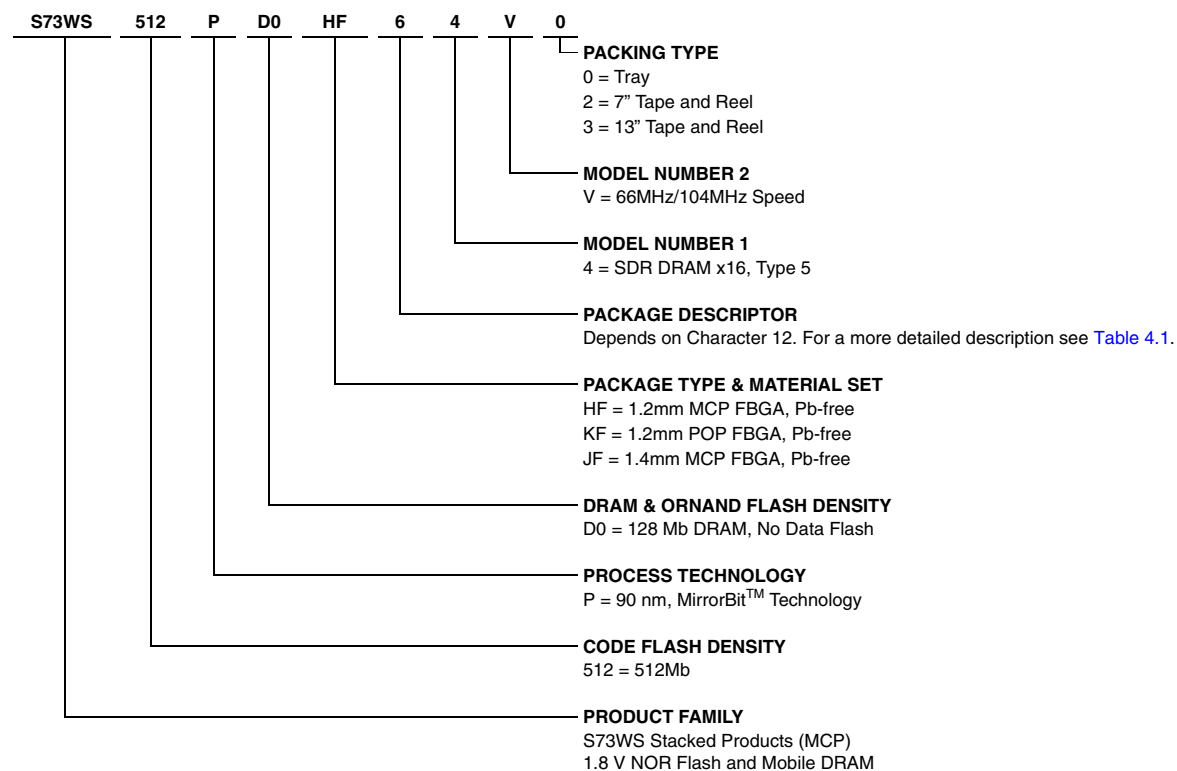


Table 4.1 Character Position Descriptions (Sheet 1 of 2)

Character 12	Character 13	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
H, J, or G	0	7x9 mm	56	0.35 mm
	1	7x9 mm	80	
	2	8x11.6 mm	64	
	3	8x11.6 mm	84	
	4	9x12 mm	84	
	5	9x12 mm	115	
	6	9x12 mm	137	
	7	11x13 mm	84	
	8	11x13 mm	115	
	9	11x13 mm	137	

Table 4.1 Character Position Descriptions (Sheet 2 of 2)

Character 12	Character 13	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
K	A	11x11 mm	112	0.45 mm
	B	11x11 mm	112	0.50 mm
	D	12x12 mm	128	0.45 mm
	F	12x12 mm	128	0.50 mm
	G	14x14 mm	152	0.45 mm
	H	14x14 mm	152	0.50 mm
	J	15x15 mm	160	0.45 mm
	K	15x15 mm	160	0.50 mm
	L	17x17 mm	192	0.45 mm
	M	17x17 mm	192	0.50 mm

4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

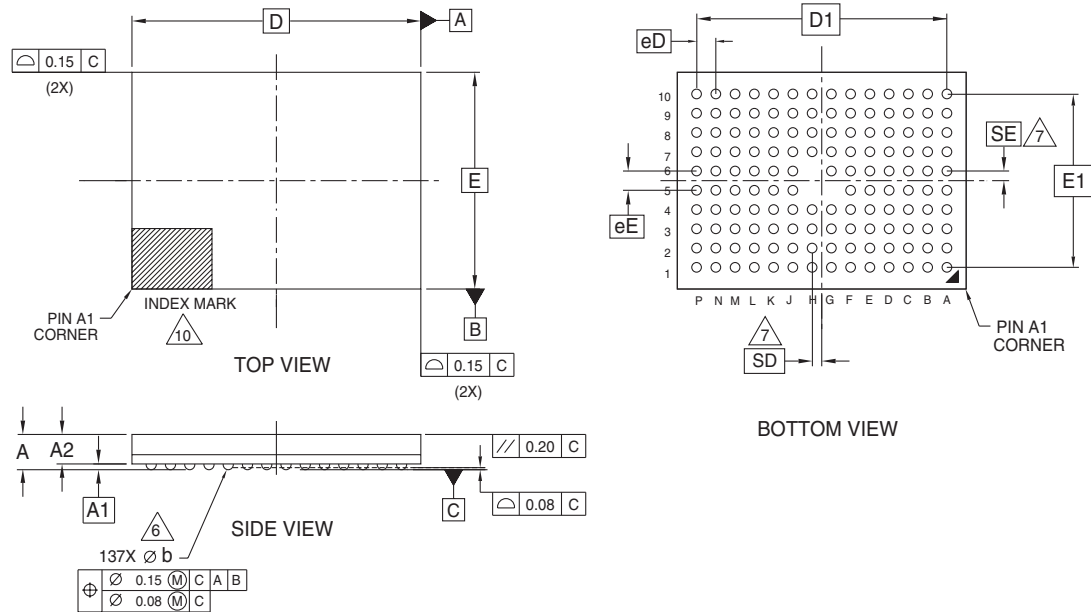
S72WS-P Valid Combinations					NOR Flash Speed	DRAM Supplier	DRAM Speed	Package Type	Package Markings
Base Ordering Number	Package & Material Set	Package Descriptor	Model Number	Packing Type					
S73WS512PD0	HF	6	4V	0, 2, 3 (Note 1)	66 MHz	Type 5	104 MHz	9x12 mm (MCP)	(Note 2)

Notes:

- Packing Type 0 is standard. Specify other options as required.
- BGA package marking omits leading S and packing type designator from ordering part number.

5. Physical Dimensions

5.1 TLD137—137-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 12.0 mm Package



PACKAGE	TLD 137			
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	12.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	10.40 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	137			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	G5,H5,H6			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. N/A

10 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3393; 16-038.22a

6. Revision History

6.1 Revision A (March 16, 2006)

Initial release.

Colophon

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