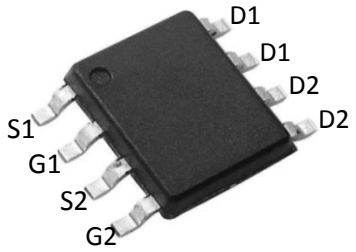
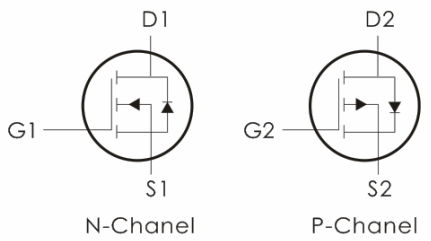
Description：

This N-Chanel and P-Channel MOSFET use advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. This device may be used to form a level shifted high side switch, and for a host of other application.





Features：

N-Channel: V_{DS}=60V,I_D=4.5A,$R_{DS(ON)}$<40mΩ @V_{GS}=10V

P-Channel: V_{DS}=-60V,I_D=-4.1A,$R_{DS(ON)}$<90mΩ @V_{GS}=-10V

1) High Power and current handing capability.
2) Lead free product is acquired.
3) Surface Mount Package.

Absolute Maximum Ratings： (T_C=25℃ unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DS}	Drain-Source Voltage	60	-60	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D	Drain Current-Continuous @T_A=25℃[1]	4.5	-4.1	A
	Drain Current-Continuous @T_A=70℃[1]	3.5	-3.2	
I_{DM}	Pulsed Drain Current-[2]	18	-14	
EAS	Single Pulse Avalanche Energy[3]	22	29.7	mJ
I_{AS}	Avalanche Current	21	24.2	A
P_D	Power Dissipation[4]	1.5	1.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	-55 to +150	℃

Thermal Characteristics：

Symbol	Parameter	N-Channel Max	P-Channel Max	Units
$R_{\Theta JA}$	Thermal Resistance,Junction to Ambient[1]	85	85	℃/W
$R_{\Theta JAC}$	Thermal Resistance,Junction Case[1]	25	25	

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N-Channel Electrical Characteristics: (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ON/Off Characteristics						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=250μA	60	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=48V	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics						
$V_{GS(th)}$	GATE-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=250μA	1	---	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[2]	V_{GS}=10V,I_D=4A	---	---	40	mΩ
		V_{GS}=4.5V,I_D=3A	---	---	50	
G_{FS}	Forward Transconductance	V_{DS}=5V, I_D=4A	---	28.3	---	S
Rg	Gate Resistance	V_{DS}=0V , V_{GS}=0V, f=1MHz	---	2.5	---	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	---	1027	---	pF
C_{oss}	Output Capacitance		---	65	---	
C_{rss}	Reverse Transfer Capacitance		---	46	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, I_D=4A, R_G=3.3Ω V_{GS}=10V	---	3	---	ns
t_r	Rise Time		---	34	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	23	---	ns
t_f	Fall Time		---	6	---	ns
Q_g	Total Gate Charge（4.5V）	V_{GS}=10V, V_{DS}=48V, I_D=4A	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	2.6	---	nC
Q_{gd}	Gate-Drain “Miller” Charge		---	4.1	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage[2]	V_{GS}=0V,I_S=1A , T_J=25℃	---	---	1.2	V

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I_S	Continuous Source Current[1,5]	$V_G=V_D=0V$,Force Current	---	---	4.5	A
I_{SM}	Pulsed Source Current[2,5]		---	---	18	
trr	Reverse Recovery Time	$I_F=4A$, dI/dt=100A/μs , $T_J=25℃$	---	12.1	---	nS
Qrr	Reverse Recovery Charge		---	6.7	---	nC

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=21A
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics: (T_C=25℃ unless otherwise noted)

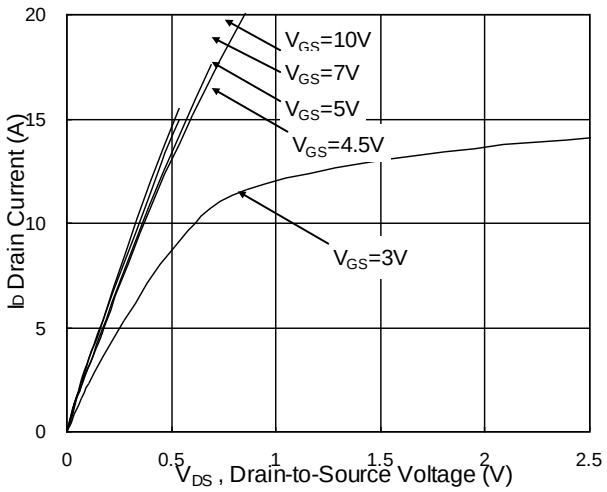

Fig.1 Typical Output Characteristics

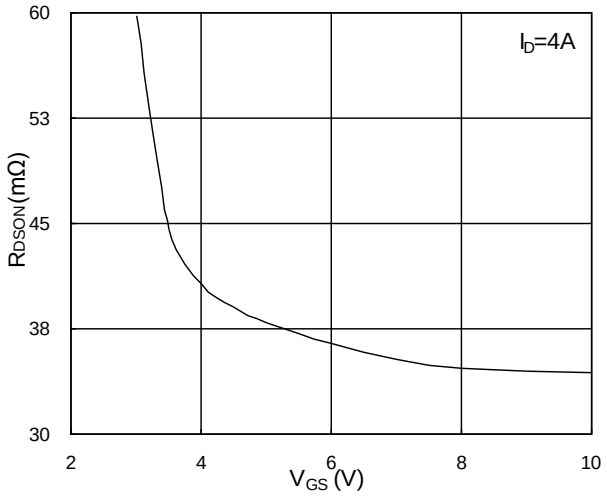

Fig.2 On-Resistance vs. Gate-Source

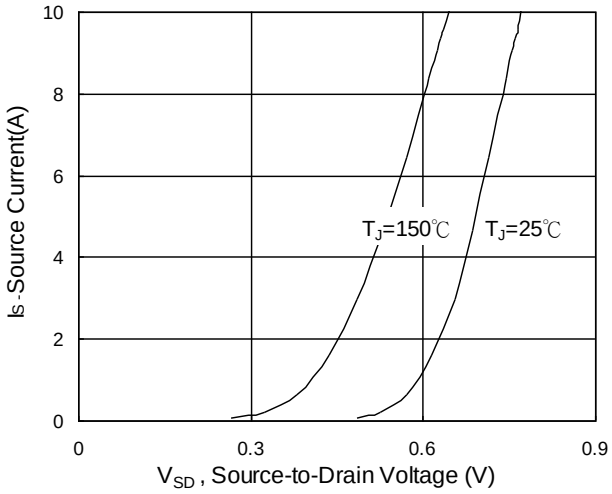

Fig.3 Forward Characteristics Of Reverse

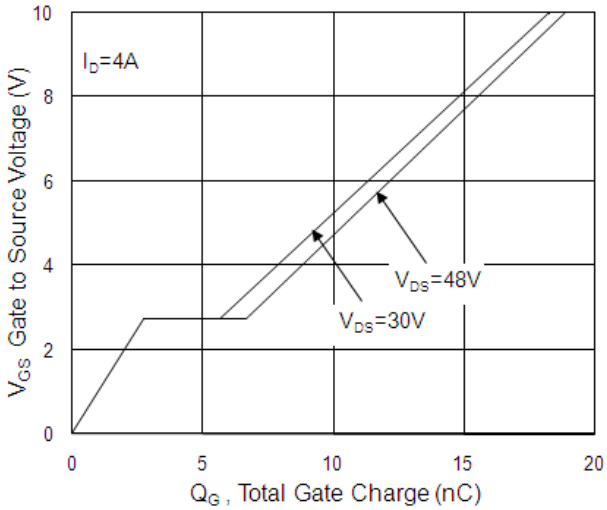

Fig.4 Gate-Charge Characteristics

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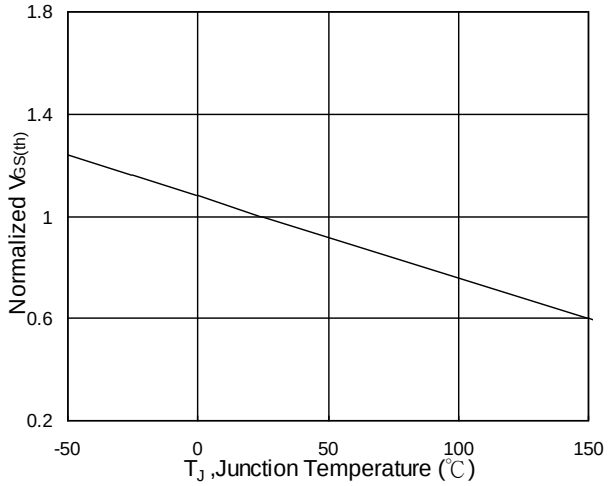

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

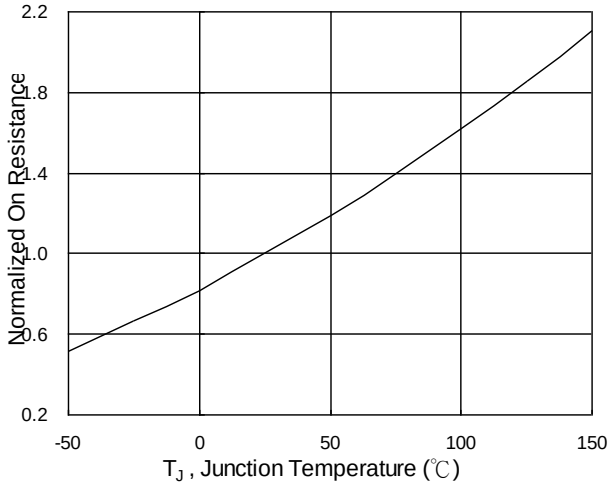

Fig.6 Normalized R_{DSON} vs. T_J

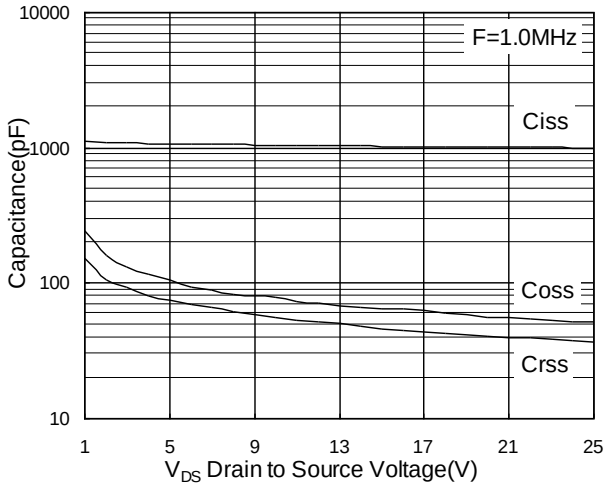

Fig.7 Capacitance

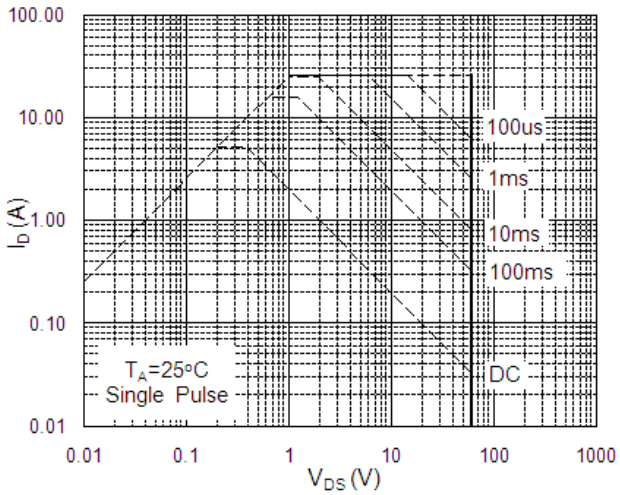

Fig.8 Safe Operating Area

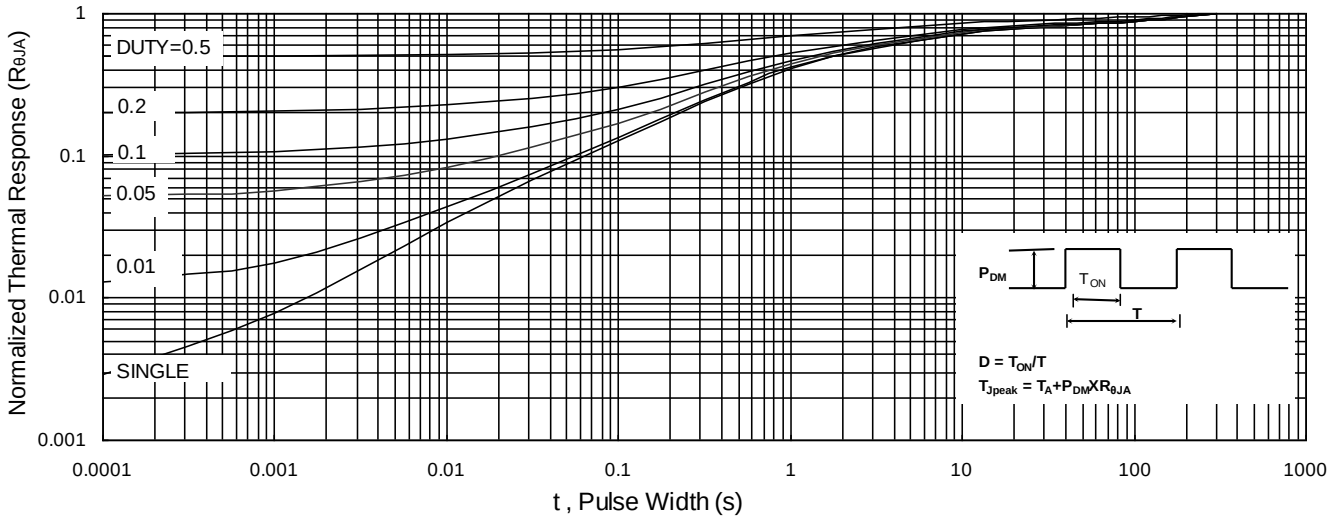

Fig.9 Normalized Maximum Transient Thermal Impedance

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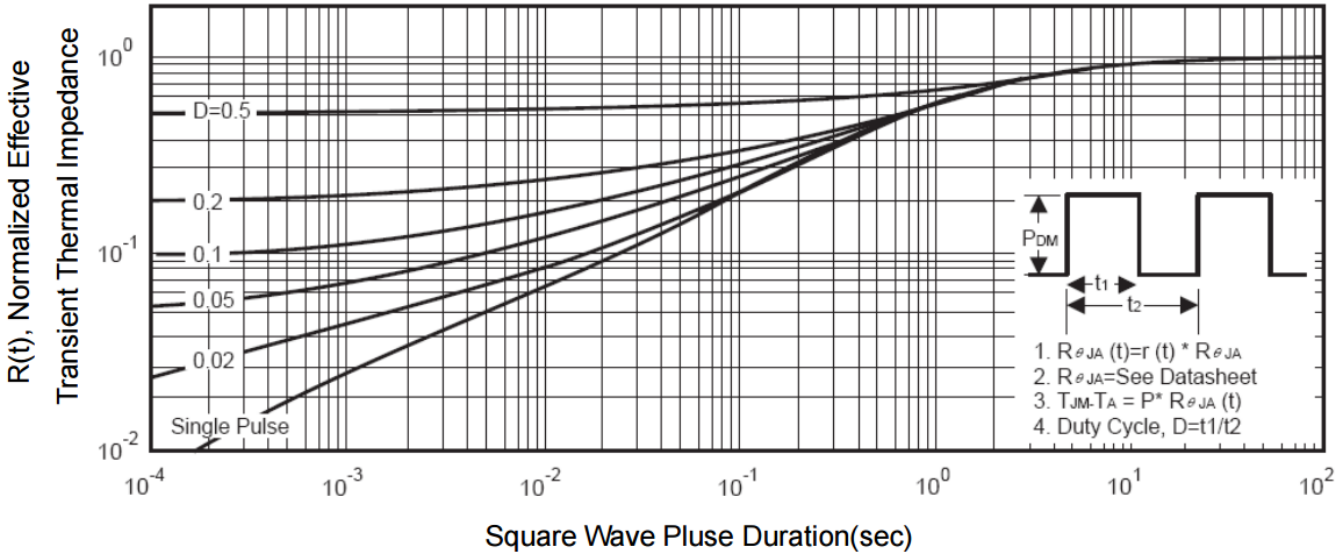

Figure11. Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics: (T_C=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ON/Off States						
BV_{DSS}	Drain-Sourtce Breakdown Voltage	V_{GS}=0V,I_D=-250 μ A	-60	---	---	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=-48V	---	---	1	μ A
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0A	---	---	±100	nA
On Characteristics[3]						
$V_{GS(th)}$	GATE-Source Threshold Voltage	V_{GS}=V_{DS}, I_D=-250 μ A	-1.2	---	-2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance[2]	V_{GS}=-10V,I_D=-3A	---	---	90	m Ω
		V_{GS}=-4.5V,I_D=-2A	---	---	115	
G_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-3A	---	8.7	---	S
Rg	Gate Resistance	VDS= 0 V , VGS =0V, f=1MHz	---	15	---	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz	---	1080	---	pF
C_{oss}	Output Capacitance		---	73	---	
C_{rss}	Reverse Transfer Capacitance		---	50	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, $_{GS}$=-10V,	---	8.8	---	ns

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t_r	Rise Time	R_{GEN}=3.3Ω ,I_D=-1A	---	19.6	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	47.2	---	ns
t_f	Fall Time		---	9.6	---	ns
Q_g	Total Gate Charge（-4.5V）	V_{GS}=-4.5V, V_{DS}=-48V, I_D=-3A	---	11.8	---	nC
Q_{gs}	Gate-Source Charge		---	1.9	---	nC
Q_{gd}	Gate-Drain "Miller" Charge		---	6.5	---	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage[3]	V_{GS}=0V,I_S=-6.5A	---	---	-1.2	V
I_S	Continuous Source Current[1,5]	VG=VD=0v, , Force Current	---	---	-4.1	A
I_{SM}	Diode Forward Voltage[2]		---	---	-14	

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-24.4A
4.The power dissipation is limited by 150℃ junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics: (T_C=25℃ unless otherwise noted)

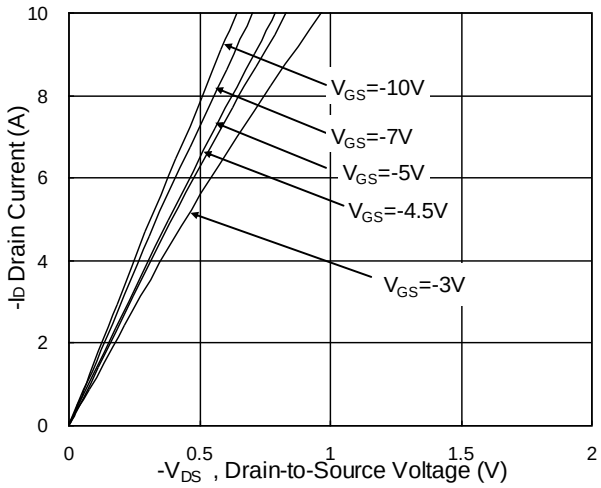

Fig.1 Typical Output Characteristics

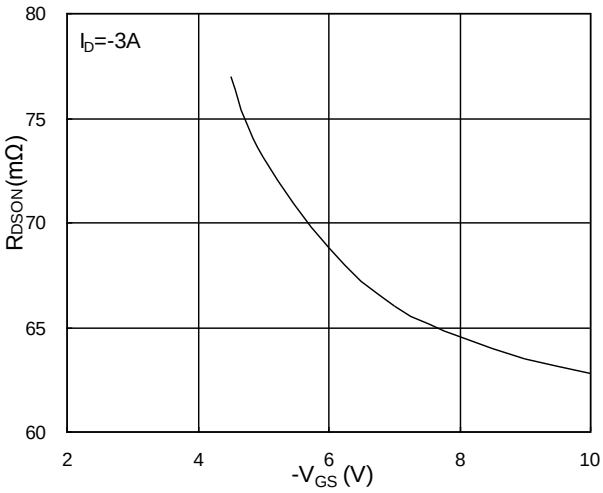

Fig.2 On-Resistance v.s Gate-Source

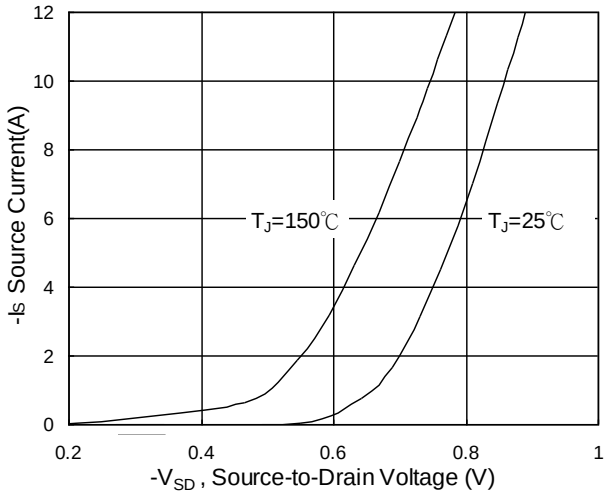

Fig.3 Forward Characteristics of Reverse

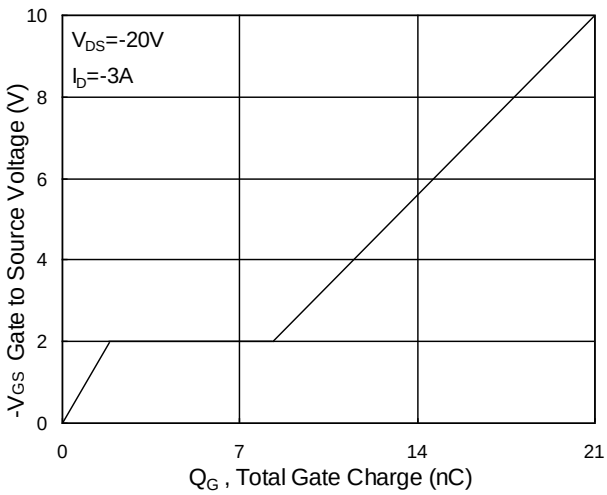

Fig.4 Gate-Charge Characteristics

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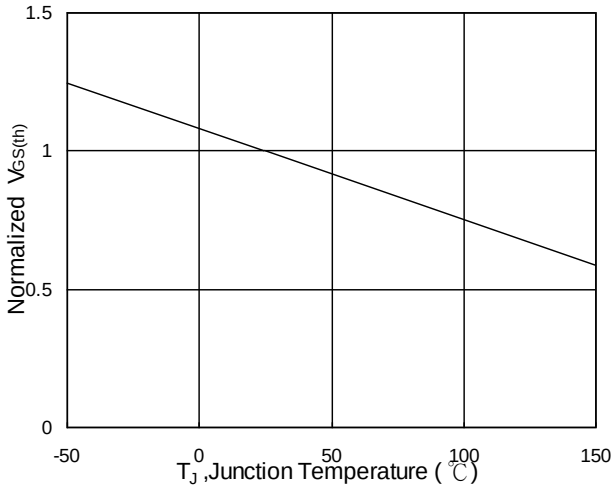

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

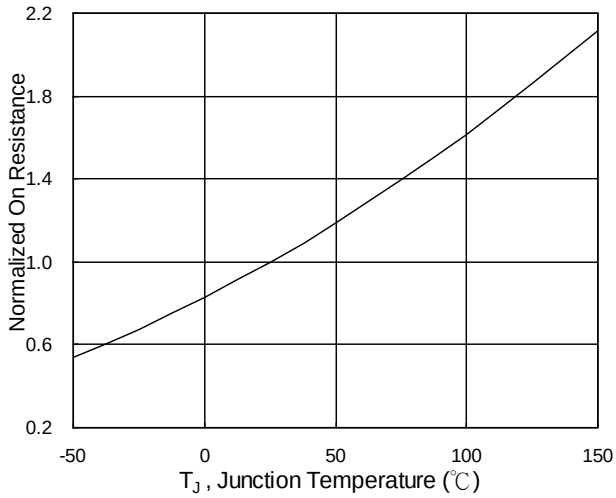

Fig.6 Normalized R_{DSON} vs. T_J

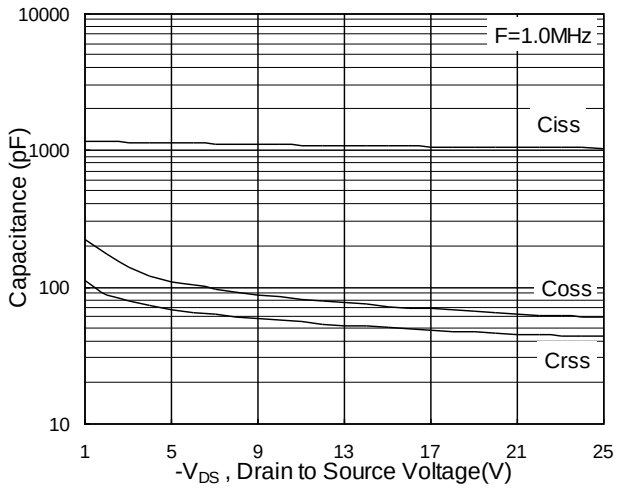

Fig.7 Capacitance

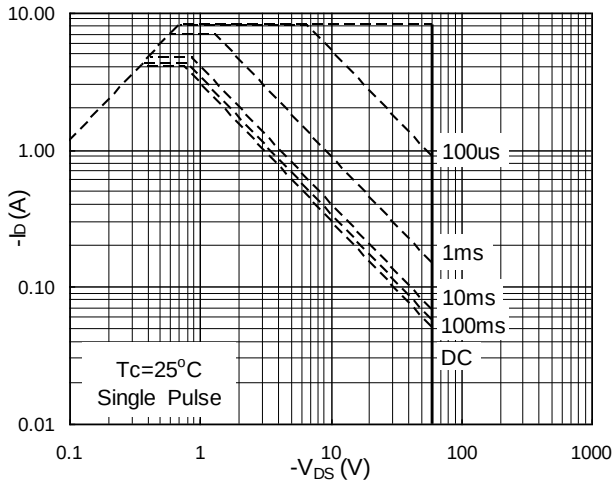

Fig.8 Safe Operating Area

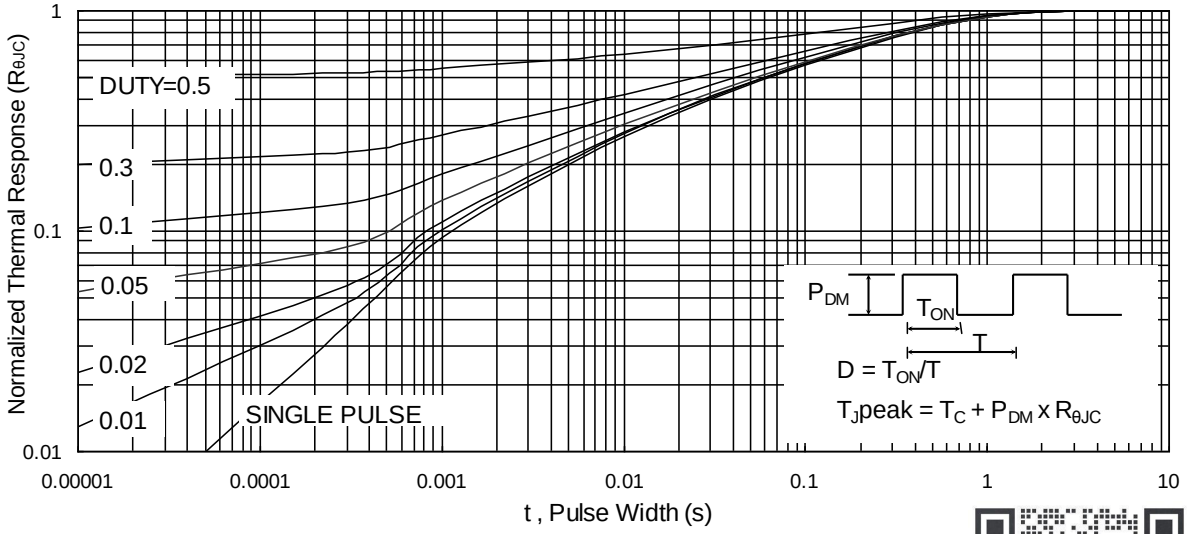

Fig.9 Normalized Maximum Transient Thermal Impedance

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