TISP61089AS
DUAL FORWARD-CONDUCTING P-GATE THYRISTORS
PROGRAMMABLE OVERVOLTAGE PROTECTORS

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OCTOBER 1999

RINGING SLIC OVERVOLTAGE PROTECTION FOR LSSGR ‘1089

- **Dual Voltage-Programmable Protectors**
  - **— High Voltage Rating.....-120 V**
  - **— Wide Programming Range..... 0 to -100 V**
  - **— Low Gate Triggering Current .....< 5 mA**
  - **— High Holding Current .....> 150 mA**
- **Increased Gound Pin Clearance Version of TISP61089AD**
  - **— Ground Lead Creepage .....> 3 mm**
  - **— Small Outline Surface Mount Package**
- **Rated for LSSGR ‘1089 Conditions**

WAVE SHAPE	‘1089 TEST CLAUSE AND TEST #	I_{TSP} A
2/10 µs	4.5.8 Second-Level 1	120
10/1000 µs	4.5.7 First-Level 3	30

60 Hz POWER FAULT TIME	‘1089 TEST CLAUSE AND TEST #	I_{TSM} A
100 ms	4.5.13 Second-Level 2	11
1 s	4.5.13 Second-Level 2	4.8
5 s	4.5.13 Second-Level 2	2.7
300 s	4.5.13 Second-Level 1	0.95
900 s	4.5.13 Second-Level 1	0.92

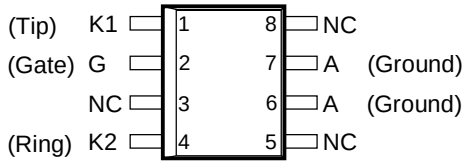
- **2/10 Protection Voltage Specified**

ELEMENT	FIRST-LEVEL V @ 56 A	SECOND-LEVEL V @ 100 A
Diode	6	8
Crowbar V_{GG} = -48 V	-57	-60

- **Rated for ITU-T K20 & K21 impulses**

WAVE SHAPE		I_{TSP} A
VOLTAGE	CURRENT	
10/700 µs	5/320	40

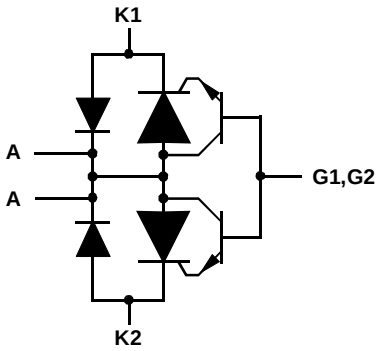
D PACKAGE
(TOP VIEW)



MD6XBA

NC - No internal connection
Terminal typical application names shown in parenthesis

device symbol



Terminals K1, K2 and A correspond to the alternative line designators of T, R and G or A, B and C. The negative protection voltage is controlled by the voltage, $V_{GG,}$ applied to the G terminal.

SD6XAP

description

The TISP61089AS is a dual forward-conducting buffered p-gate overvoltage protector. It is designed to protect ringing SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISP61089AS limits voltages that exceed the SLIC supply rail voltage. The TISP61089AS parameters are specified to allow equipment compliance with Bellcore GR-1089-CORE, Issue 1.

AVAILABLE OPTIONS

CARRIER	ORDER #
Tube	TISP61089ASD
Taped and reeled	TISP61089ASDR

PRODUCT INFORMATION

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage in the region of -10 V to -100 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. As the protection voltage will then track the negative supply voltage the overvoltage stress on the SLIC is minimised.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector will crowbar into a low voltage on-state condition. As the overvoltage subsides the high holding current of the crowbar prevents d.c. latchup.

The TISP61089AS is intended to be used with a series combination of a 25 Ω or higher resistance and a suitable overcurrent protector. Power fault compliance requires the series overcurrent element to open-circuit or become high impedance (see Applications Information). For equipment compliant to ITU-T recommendations K20 or K21 only, the series resistor value is set by the power cross requirements. For K20 and K21, a minimum series resistor value of 10 Ω is recommended.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The TISP61089AS buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction.

The TISP61089AS is the TISP61089AD with a different pinout. The feed-through Ring (leads 4 — 5) and Tip (leads 1 — 8) connections have been replaced by single Ring (lead 4) and Tip (lead 1) connections. This increases package creepage distance of the biased to ground connections from about 0.7 mm to over 3 mm. This increased spacing eases the design task of compliance with various safety standards, such as UL 1950.

absolute maximum ratings

RATING	SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, I_G = 0, -40°C ≤ T_J ≤ 85°C	V_{DRM}	-120	V
Repetitive peak gate-cathode voltage, V_{KA} = 0, -40°C ≤ T_J ≤ 85°C	V_{GKRM}	-120	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)			
10/1000 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)	I_{TSP}	30	A
5/320 µs (ITU-T recommendation K20 & K21, open-circuit voltage wave shape 10/700)		40	
1.2/50 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4, Alternative)		100	
2/10 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)		120	
Non-repetitive peak on-state current, V_{GG} = -80 V, 50 Hz to 60 Hz (see Notes 1 and 2)			
100 ms	I_{TSM}	11	A
1 s		4.8	
5 s		2.7	
300 s		0.95	
900 s		0.92	
Non-repetitive peak gate current, 1/2 µs pulse, cathodes commoned (see Notes 1 and 2)	I_{GSM}	40	A
Operating free-air temperature range	T_A	-40 to +85	°C
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.
2. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above 25 °C ambient temperature, derate linearly at -0.6 %/°C. Current values for other times and gate voltages are shown in Figure 2.

recommended operating conditions

		MIN	TYP	MAX	UNIT
C_G	Gate decoupling capacitor	100	220		nF
R_S	TISP61089AS series resistor for first-level and second-level surge survival TISP61089AS series resistor for first-level surge survival	40 25			Ω

electrical characteristics, T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_D	Off-state current	$V_D = V_{DRM}$, I_G = 0	T_J = 25°C			-5	µA
			T_J = 85°C			-50	µA
$V_{(BO)}$	Breakover voltage	2/10 µs, I_T = -56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			-57		V
		2/10 µs, I_T = -100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			-60		
		1.2/50 µs, I_T = -53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			-60		
		1.2/50 µs, I_T = -96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			-64		
V_F	Forward voltage	I_F = 5 A, t_w = 200 µs				3	V
V_{FRM}	Peak forward recovery voltage	2/10 µs, I_F = 56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			6		V
		2/10 µs, I_F = 100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			8		
		1.2/50 µs, I_F = 53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			8		
		1.2/50 µs, I_F = 96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			12		
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -48 V		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GK} = V_{GKRM}$, V_{KA} = 0	T_J = 25°C			-5	µA
			T_J = 85°C			-50	µA
I_{GT}	Gate trigger current	I_T = 3 A, $t_{p(g)} \geq$ 20 µs, V_{GG} = -48 V				5	mA
V_{GT}	Gate trigger voltage	I_T = 3 A, $t_{p(g)} \geq$ 20 µs, V_{GG} = -48 V				2.5	V
Q_{GS}	Gate switching charge	1.2/50 µs, I_T = 53 A, R_S = 47 Ω, V_{GG} = -48 V C_G = 220 nF			0.1		µC
C_{AK}	Anode-cathode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 3)	V_D = -3 V			100	pF
			V_D = -48 V			50	pF

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	T_A = 25 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, $I_T = I_{TSM(900)}$			105	°C/W

PARAMETER MEASUREMENT INFORMATION

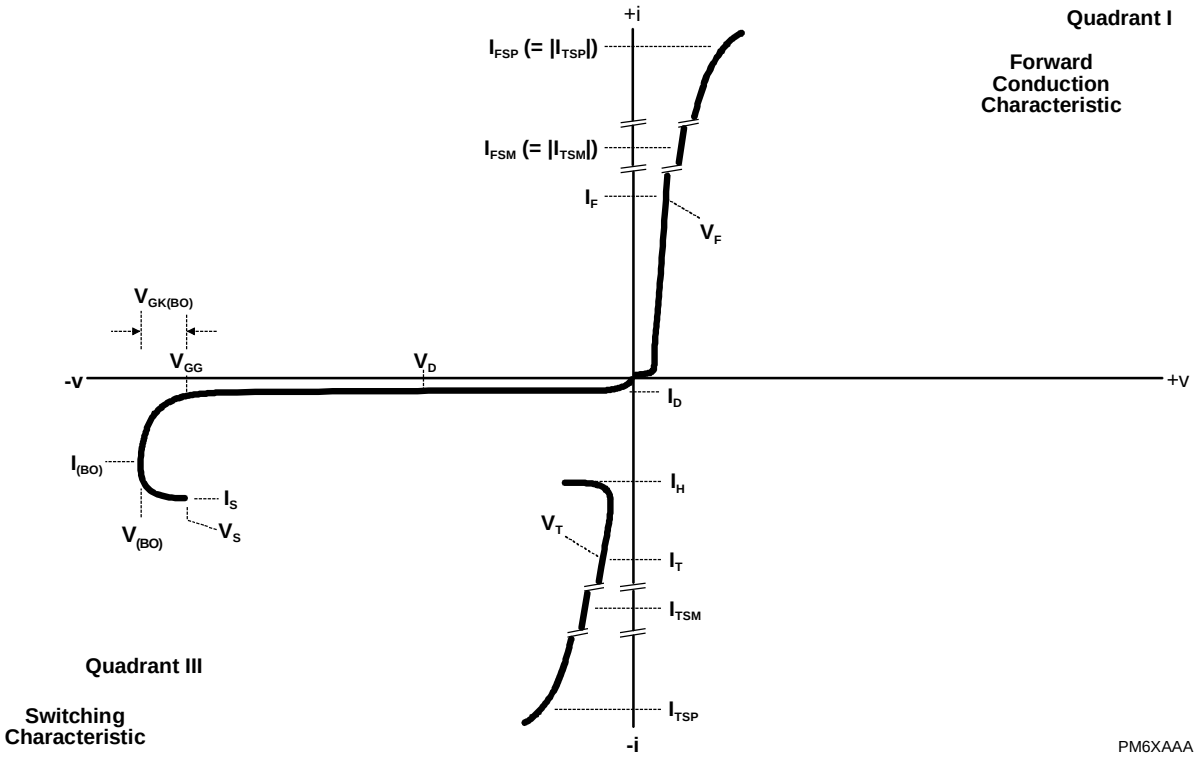


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC

THERMAL INFORMATION

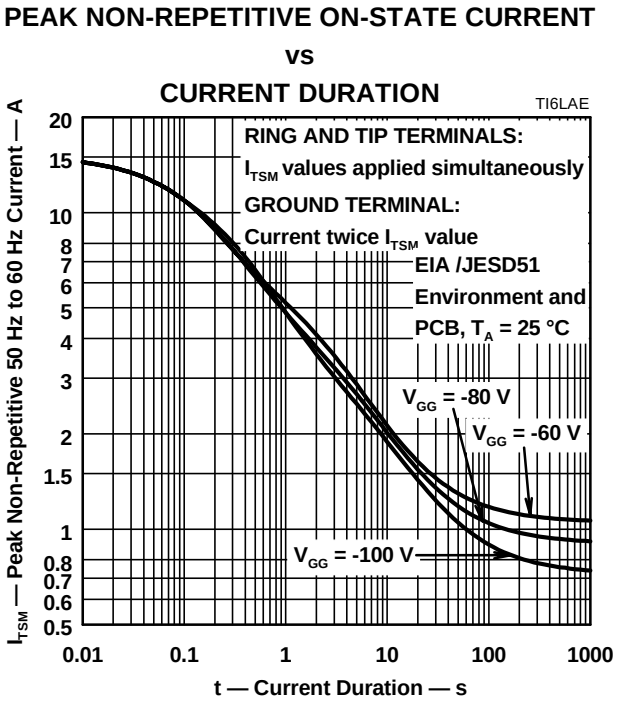


Figure 2. NON-REPETITIVE PEAK ON-STATE CURRENT AGAINST DURATION

APPLICATIONS INFORMATION

gated protectors

This section covers three topics. Firstly, it is explained why gated protectors are needed. Second, the voltage limiting action of the protector is described. Third, an example application circuit is described.

purpose of gated protectors

Fixed voltage thyristor overvoltage protectors have been used since the early 1980s to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. As the SLIC was usually powered from a fixed voltage negative supply rail, the limiting voltage of the protector could also be a fixed value. The TISP1072F3 is a typical example of a fixed voltage SLIC protector.

SLICs have become more sophisticated. To minimise power consumption, some designs automatically adjust the supply voltage, V_{BAT}, to a value that is just sufficient to drive the required line current. For short lines the supply voltage would be set low, but for long lines, a higher supply voltage would be generated to drive sufficient line current. The optimum protection for this type of SLIC would be given by a protection voltage which tracks the SLIC supply voltage. This can be achieved by connecting the protection thyristor gate to the SLIC supply, Figure 3. This gated (programmable) protection arrangement minimises the voltage stress on the SLIC, no matter what value of supply voltage.

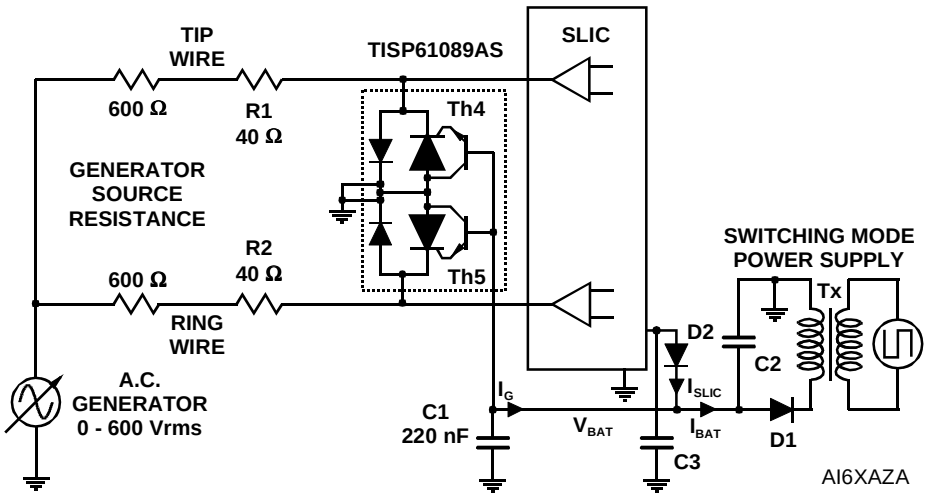


Figure 3. TISP61089AS BUFFERED GATE PROTECTOR (SECTION 4.5.12 TESTING CONDITION)

In the mid-1990s ringing SLICs were introduced. These integrated the ringing fuction by using the SLIC line driver stage as a differential power amplifier. Operating on negative supply voltages down to -75 V, these ringing SLICs produced ring voltage levels sufficient for short loop applications (e.g. ISDN terminal adaptors). With an -85 V rating, the TISP61089 was used to protect these SLICs. The need for higher ringing voltage levels has led to the introduction of ringing SLICs with supply voltages approaching -100 V (e.g. the Am79R241). To protect this new class of ringing SLIC, the -120 V rated TISP61089A has been developed.

operation of gated protectors

Figures 4. and 5. show how the TISP61089AS limits negative and positive overvoltages. Positive overvoltages (Figure 5) are clipped by the antiparallel diodes in the TISP61089AS and the resulting current is diverted to ground. Negative overvoltages (Figure 4.) are initially clipped close to the SLIC negative supply rail value (V_{BAT}). If sufficient current is available from the overvoltage, then the protector (Th5) will crowbar into a low voltage on-state condition. As the overvoltage subsides the high holding current of the crowbar prevents d.c. latchup. The protection voltage will be the sum of the gate supply (V_{BAT}) and the peak gate-cathode voltage ($V_{GK(BO)}$). The protection voltage will be increased if there is a long connection between the gate decoupling capacitor, C1, and the gate terminal. During the initial rise of a fast impulse, the gate current (I_G) is the same as the cathode current (I_K). Rates of 70 A/µs can cause inductive voltages of 0.7 V in 2.5 cm of printed wiring track. To minimise this inductive voltage increase of protection voltage, the length of the capacitor to gate terminal tracking should be minimised. Inductive voltages in the protector cathode wiring will also increase the protection voltage. These voltages can be minimised by routing the line to SLIC connection via the protector.

In Figure 6, the positive gate charge (Q_{GS}) is about 0.1 µC which, with the 0.1 µF gate decoupling capacitor used, increased the gate supply by about 1 V (= Q_{GS}/C1). This change is just visible on the -72 V gate voltage, V_{BAT}. This increase does not directly add to the protection voltage as the supply voltage change reaches a maximum at 0.4 µs when the gate current reverses polarity; whereas the protection voltage peaks at 0.3 µs. In Figure 6, the peak clamping voltage ($V_{(BO)}$) is -77.5 V, an increase of 5.5 V on the nominal gate supply voltage. This 5.5 V increase is the sum of the supply rail increase at that time, (0.5 V), and the protection circuits cathode diode to supply rail breakover voltage (5 V). In practice, use of the recommended 220 nF gate decoupling capacitor would give a supply rail increase of 0.25 V and a $V_{(BO)}$ value of about -77.25 V.

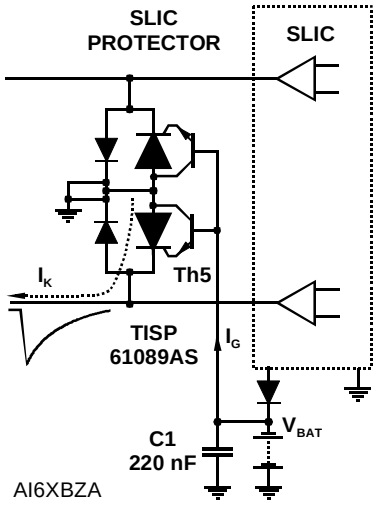


Figure 4. NEGATIVE OVERVOLTAGE CONDITION

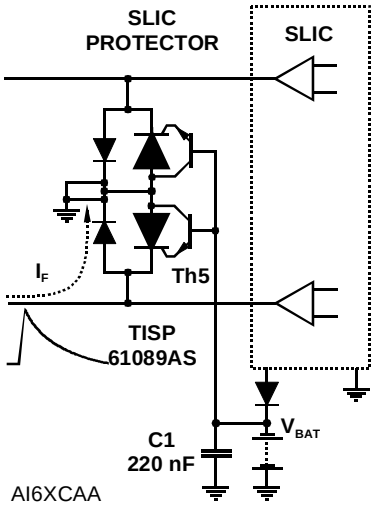


Figure 5. POSITIVE OVERVOLTAGE CONDITION

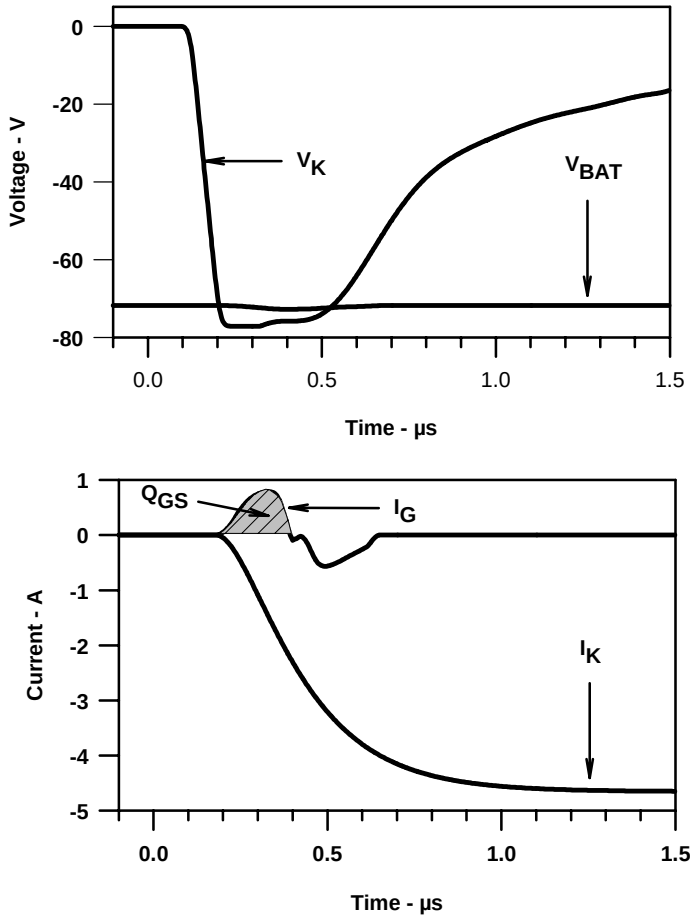


Figure 6. PROTECTOR FAST IMPULSE CLAMPING AND SWITCHING WAVEFORMS

application circuit

Figure 7 shows a typical TISP61089AS SLIC card protection circuit. The incoming line conductors, Ring (R) and Tip (T), connect to the relay matrix via the series overcurrent protection. Fusible resistors, fuses and positive temperature coefficient (PTC) resistors can be used for overcurrent protection. Resistors will reduce the prospective current from the surge generator for both the TISP61089AS and the ring/test protector. The TISP7xxxF3 protector has the same protection voltage for any terminal pair. This protector is used when the ring generator configuration may be ground or battery-backed. For dedicated ground-backed ringing generators, the TISP3xxxF3 gives better protection as its inter-conductor protection voltage is twice the conductor to ground value.

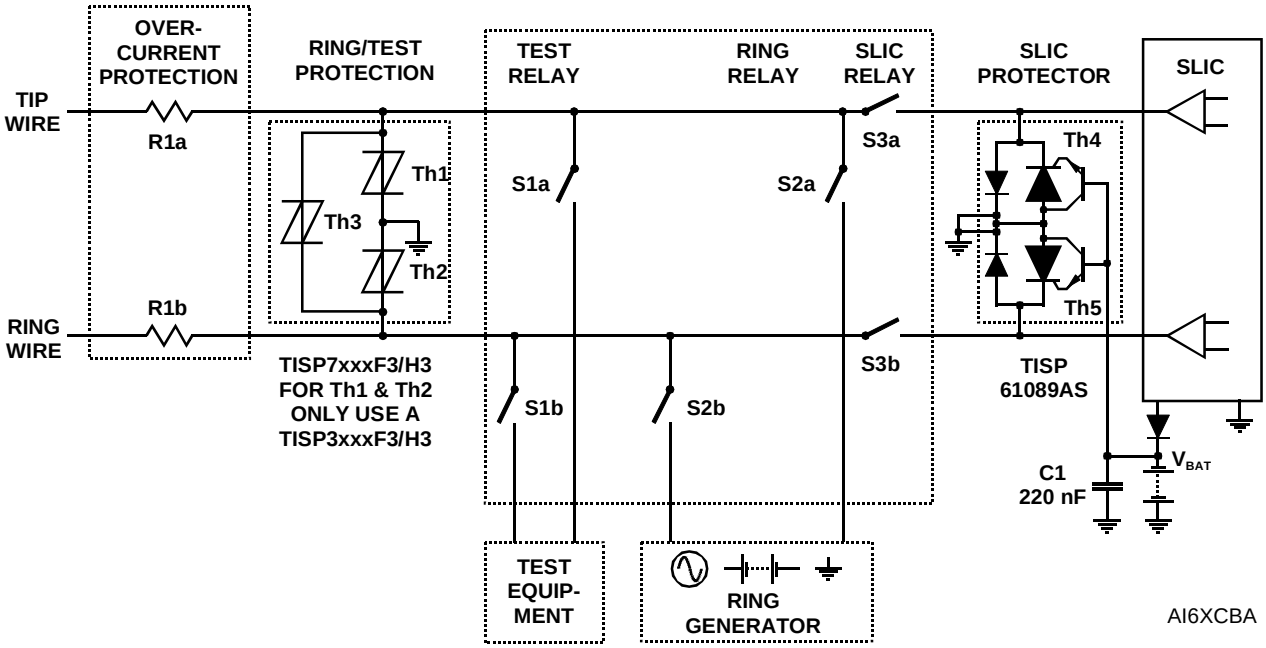


Figure 7. TYPICAL APPLICATION CIRCUIT

Relay contacts 3a and 3b connect the line conductors to the SLIC via the TISP61089AS protector. The protector gate reference voltage comes from the SLIC negative supply (V_{BAT}). A 220 nF gate capacitor sources the high gate current pulses caused by fast rising impulses.

LSSGR 1089

GR-1089-CORE, “1089”, covers electromagnetic compatibility and electrical safety generic criteria for US network telecommunication equipment. It is a module in Volume 3 of LSSGR (LATA (Local Access Transport Area) Switching Systems Generic Requirements, FR-NWT-000064). In 1089 surge and power fault immunity tests are done at two levels. After first-level testing the equipment shall not be damaged and shall continue to operate correctly. Under second level testing the equipment shall not become a safety hazard. The equipment is permitted to fail as a result of second-level testing. When the equipment is to be located on customer premises, second-level testing includes a wiring simulator test, which requires the equipment to reduce the power fault current below certain values.

The following clauses reference the 1089 section and calculate the protector stress levels. The TISP61089AS is specified for use with a 40 Ω series resistor. This resistor value will ensure that the TISP61089AS survives second level surge testing. Values down to 25 Ω may be used if some second level surge failure is acceptable. All the tabulated values are for a series resistance of 40 Ω. Peak current values for a 25 Ω series resistor are covered in the clause text.

The values of protector current are calculated from the open circuit generator voltage divided by the sum of the total circuit resistance. The total circuit resistance is the sum of the generator fictive source resistance and the TISP61089AS series resistor value. Most generators have multiple outputs and each output connects to an individual line conductor. For those generators that have a single output, each conductor will have an effective generator fictive source resistance of n times the generator fictive source resistance, where n is the number of conductors simultaneously tested.

GR-1089-CORE section 4.5.7 - first-level surge testing

The two most significant test wave shapes in this section are the high energy 10/1000 and the high current 2/10. As shown in table 1, the peak currents for these surges are 2x20 A and 2x56 A respectively. The protector must survive the 2x20 A 10/1000 surge and the TISP61089AS will do this as its rating is 2x30 A. When both conductors are surged simultaneously the return (anode) current will be 40 A, again the TISP61089AS will survive this as its rating for this condition will be 60 A. Similarly the TISP61089AS will survive the 2x56 A 2/10 as its rating is 2x120 A.

table 1. first-level surge currents

WAVE SHAPE	OPEN-CIRCUIT VOLTAGE V	SHORT-CIRCUIT CURRENT A	GENERATOR FICTIVE SOURCE RESISTANCE Ω	TOTAL CIRCUIT RESISTANCE Ω	I_T A
2/10	2500	500	5	45	2x56
1.2/50, 8/20 (See Text)	2500	360	4 + 3	47	2x53
10/360	1000	100	10	50	2x20
10/1000	600	100	6	46	2x13
10/1000	1000	100	10	50	2x20

The highest protection voltage will be for the 56 A 2/10 wave shape. Under this condition the average rate of current rise will be 56/2 = 28 A/µs. The value of diode and thyristor voltage under this condition is specified in the electrical characteristics.

Compared to TR-NWT-001089, Issue 1, October 1991, GR-1089-CORE, Issue 1, November 1994, adds the alternative of using the IEEE C62.41 1.2/50-8/20 combination wave generator for the 2/10 test. This generator usually has a single output and a fictive resistance of 2 Ω. The 2/10 generator has a fictive output resistance 5 Ω, (2500/500), and GR-1089-CORE compensates for this by adding an extra 3 Ω in the output of the 1.2/50-8/20 generator. In practice, the extra 3 Ω causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The TISP61089AS will survive the 2x53 A 1.2/50 as its rating is 2x100 A.

Using a 25 Ω series resistor will result in table 1. I_T column values of 2x83, 2x78, 2x29, 2x19 and 2x29. The TISP61089AS will survive these peak current values as they are lower than the TISP61089AS ratings.

GR-1089-CORE section 4.5.8 - second-level surge testing

This is a 2/10 wave shape test. As shown in table 2, the peak current for this surge is 2x100 A. The TISP61089AS will survive the 2x100 A 2/10 surge as its rating is 2x120 A.

table 2. second-level surge current

WAVE SHAPE	OPEN-CIRCUIT VOLTAGE V	SHORT-CIRCUIT CURRENT A	GENERATOR FICTIVE SOURCE RESISTANCE Ω	TOTAL CIRCUIT RESISTANCE Ω	I_T A
2/10	5000	500	10	50	2x100
1.2/50, 8/20 (See Text)	5000	420	4 + 8/conductor	52	2x96

Under this condition the average rate of current rise will be 100/2 = 50 A/µs. The value of diode and thyristor voltage under this condition is specified in the electrical characteristics.

Compared to TR-NWT-001089, Issue 1, October 1991, GR-1089-CORE, Issue 1, November 1994, adds the alternative of using the IEEE C62.41 1.2/50-8/20 combination wave generator for the 2/10 test. The 2/10 generator has a fictive output resistance 10 Ω, (5000/500), and GR-1089-CORE compensates for this by adding an extra 8 Ω in the output of the 1.2/50-8/20 generator. In practice, the extra 8 Ω causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The TISP61089AS will survive the 2x96 A 1.2/50 as its rating is 2x100 A.

Using a 25 Ω series resistor will result in table 2. I_T column values of 2x143 and 2x135. The TISP61089AS may fail at these peak current values as they are higher than the TISP61089AS ratings.

GR-1089-CORE section 4.5.9 - Intra-building surge testing

These tests use a 2/10 wave shape. As shown in table 3, the peak currents for this test are 2x27 A and 17 A. The TISP61089AS can survive both these levels as its rating is 2x120 A.

table 3. intra-building surge currents

WAVE SHAPE	OPEN-CIRCUIT VOLTAGE V	SHORT-CIRCUIT CURRENT A	GENERATOR FICTIVE SOURCE RESISTANCE Ω	TOTAL CIRCUIT RESISTANCE Ω	I_T A
2/10	1500	100	15	55	2x27
	800	100	8	48	17
1.2/50, 8/20 (See Text)	1500	94	4 + 12/conductor	56	2x27
	800	100	2 + 6	48	17

Compared to TR-NWT-001089, Issue 1, October 1991, GR-1089-CORE, Issue 1, November 1994, the 2/10 alternative of using a CCITT Recommendation K.22 1.2/50-8/20 combination wave generator has been changed to an IEEE C62.41 1.2/50-8/20 generator. This generator usually has a single output and a fictive resistance of 2 Ω. The 2/10 generator has fictive output resistances of 15 Ω and 8 Ω. GR-1089-CORE compensates for this by adding an extra resistances of 12 Ω and 6 Ω in the output of the 1.2/50-8/20 generator. In practice, this extra resistance causes the prospective short-circuit current wave shape to be similar to the 1.2/50 open-circuit voltage wave shape. The TISP61089AS will survive the 2x27 A 1.2/50 as its rating is 2x100 A.

Using a 25 Ω series resistor will result in table 3. I_T column values of 2x38, 24, 2x37 and 24. The TISP61089AS will survive these peak current values as they are lower than the TISP61089AS ratings.

GR-1089-CORE section 4.5.12 - first-level power fault testing

The most significant tests are a long duration (900 s) medium current test and a higher current tests of 60 one second power applications. As shown in table 4, the peak currents for these tests are 2x0.37 A and 2x1.3 A respectively. At a gate voltage of -80 V, the TISP61089AS will survive both these conditions as its ratings are 2x0.92 A and 2x4.8 A for these time periods

table 4. first-level power fault currents

A.C. DURATION s	OPEN-CIRCUIT RMS VOLTAGE V	SHORT-CIRCUIT RMS CURRENT A	SOURCE RESISTANCE Ω	TOTAL CIRCUIT RESISTANCE Ω	I_{TRMS} A	I_{TM} A
1	200	0.33	600	640	2x0.31	2x0.44
1	400	0.67	600	640	2x0.63	2x0.88
1	600	1	600	640	2x0.94	2x1.3
1	1000	1	1000	1040	2x0.96	2x1.3
900	50	0.33	150	190	2x0.26	2x0.37
900	100	0.17	590	630	2x0.16	2x0.22

Using a 25 Ω series resistor will result in table 4. I_{TM} column values of 2x0.45, 2x0.9, 2x1.4, 2x1.4, 2x0.4 and 2x0.23. The TISP61089AS will survive these peak current values as they are lower than the TISP61089AS ratings.

GR-1089-CORE section 4.5.13 - second-level power fault testing

The two most significant tests are a long duration (900 s) medium current test and a higher current 5 s test. .

table 5. second-level power fault currents

A.C. DURATION s	OPEN-CIRCUIT RMS VOLTAGE V	SHORT-CIRCUIT CURRENT A	SOURCE RESISTANCE Ω	TOTAL CIRCUIT RESISTANCE Ω	I_{TRMS} A	I_{TM} A
5	600	60	10	50	2x12	2x17
5	600	7	86	126	2x4.8	2x6.8
900	120	25	5	45	2x2.7	2x3.8
900	277	25	11	51	2x5.4	2x7.7
900	100	0.37	273	313	2x0.32	2x0.45
900	300	1.1	273	313	2x0.96	2x1.4
900	600	2.2	273	313	2x1.9	2x2.7

As shown in table 5, the peak currents for these tests are 2x17 A and 2x7.7 A respectively. For the TISP61089AS to survive the 2x7.7 A, the series current limiting element must operate within 0.3 s. At 2x17.7 A, the series current limiting element must operate within 0.01 s.

Using a 25 Ω series resistor will result in table 5. I_{TM} column values of 2x24, 2x7.7, 2x5.7, 2x11, 2x0.47, 2x1.4 and 2x2.9. The TISP61089AS will probably fail for a peak current level of 2x24 A and the series current limiting element must operate in under 0.01 s to prevent exceeding the TISP61089AS package limit. For 2x7.7 A, the series current limiting element must operate within 0.3 s for TISP61089AS survival.

GR-1089-CORE section 4.5.15 - second-level power fault testing with wiring simulator

The purpose of this test is to ensure that the telephone cable does not become a hazard due to excessive current. A series fuse, type MDQ 1-6/10A, simulates the safe current levels of a telephone cable. If this fuse opens the equipment fails the test. For the equipment to pass, the equipment series overcurrent element must reduce the current to below the MDQ 1-6/10A fusing level to prevent the simulator operating. The a.c. test voltage can range from zero to 600 V, which gives a maximum conductor current of 10 A. Table 6 shows the simulator fusing times for three current levels.

table 6. second-level power fault currents with MDQ 1-6/10A fuse

A.C. DURATION s	OPEN-CIRCUIT RMS VOLTAGE V	SHORT-CIRCUIT CURRENT A	SOURCE RESISTANCE Ω	TOTAL CIRCUIT RESISTANCE Ω	I_{TRMS} A	I_{TM} A	TIME TO OPEN s
1000	100	5	20	60	1.7	2.4	∞
1000	300	15	20	60	5.0	7.1	30
1000	600	30	20	60	10	14	0.7

Using a 25 Ω series resistor will result in table 6. I_{TM} column values of 2x3.1, 2x9.4 and 2x19. Simulator operating times will be ∞, 12 s and 0.4 s respectively

For the equipment to pass this test, the TISP61089AS series current limiting element must operate before the MDQ 1-6/10A fusing times shown in table 7.

table 7. operating times of MDQ 1-6/10A fuse

TIME TO OPERATE s	I_{RMS} A
0.2	17
0.5	12
1	9
5	7
10	6.8
1000	2.5

overcurrent protection

To meet ‘1089, the overcurrent protection must be coordinated with the requirements of sections 4.5.7, 4.5.8, 4.5.9, 4.5.12, 4.5.13, 4.5.15 and the TISP61089AS. The overcurrent protection must not fail in the first level tests of sections 4.5.7, 4.5.9 and 4.5.12. Recoverable overcurrent protectors (e.g. Positive Temperature Coefficient Resistors) may operate during first level testing, but normal equipment working must be restored after the test has ended. The test current levels and their duration are shown in Figure 8. First level tests have a high source resistance and the current levels are not strongly dependent on the TISP61089AS series resistor value.

Second level tests have a low source resistance and the current levels are dependent on the TISP61089AS series resistor value. The two stepped lines at the top of Figure 8 are for the 25 Ω and 40 Ω series resistor cases. If the full current-time durations occur the equipment will fail the wiring simulator test. The MDQ 1-6/10A fusing characteristic is also shown in Figure 8. The TISP61089AS series overcurrent protection must operate before the MDQ 1-6/10A fuses, so this represents another boundary condition in the selection of the overcurrent protector.

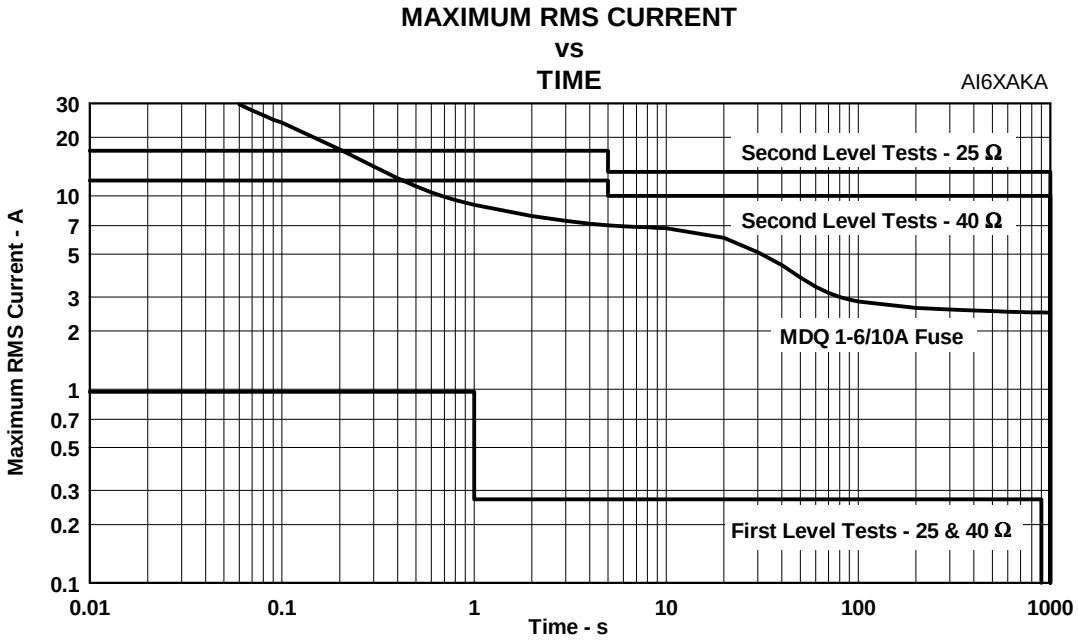


Figure 8. ‘1089 MAXIMUM TEST CURRENT LEVEL

Figure 9 summarises these boundary conditions. The highest current levels that can flow are influenced by the TISP61089AS series resistance. After one second the maximum current-time boundary becomes set by the MDQ 1-6/10A fusing characteristic. Fusible overcurrent protectors cannot operate at first level current levels.

Figure 9 shows two other curves. One is the TISP61089AS rated current at gate voltage of -100 V and the other for a gate voltage of -60 V. The overcurrent protector should not allow current-time durations greater than this otherwise the TISP61089AS may fail.

The TISP61089AS a.c. ratings are worse case values when the device is mounted on high thermal resistance EIA/JESD 51 PCB. Typical PCBs would give a 25% increase in the rated currents for periods above 0.1 s.

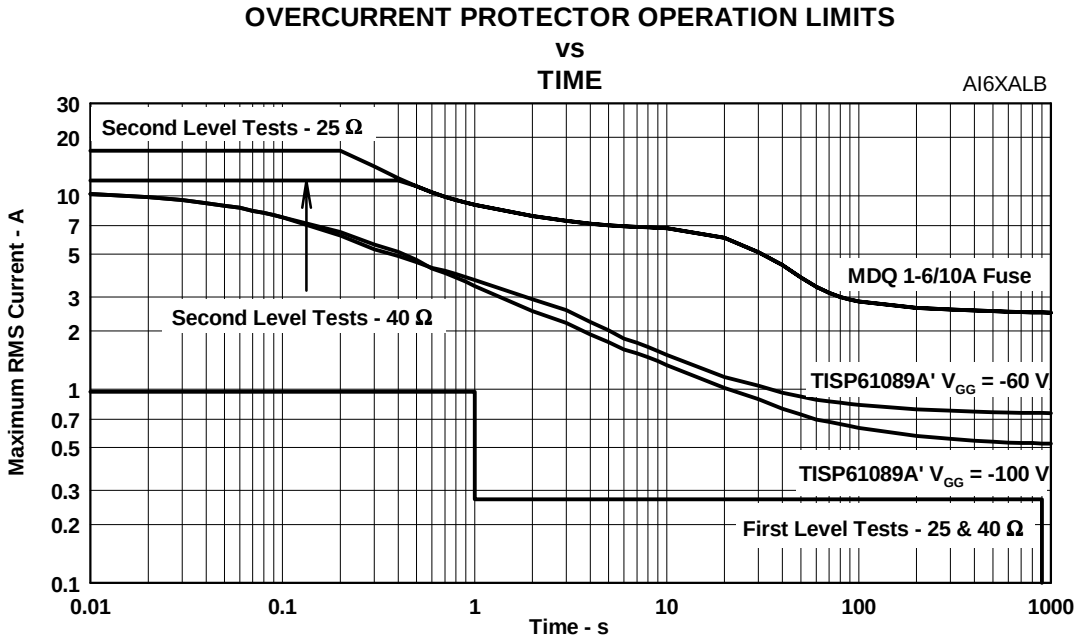


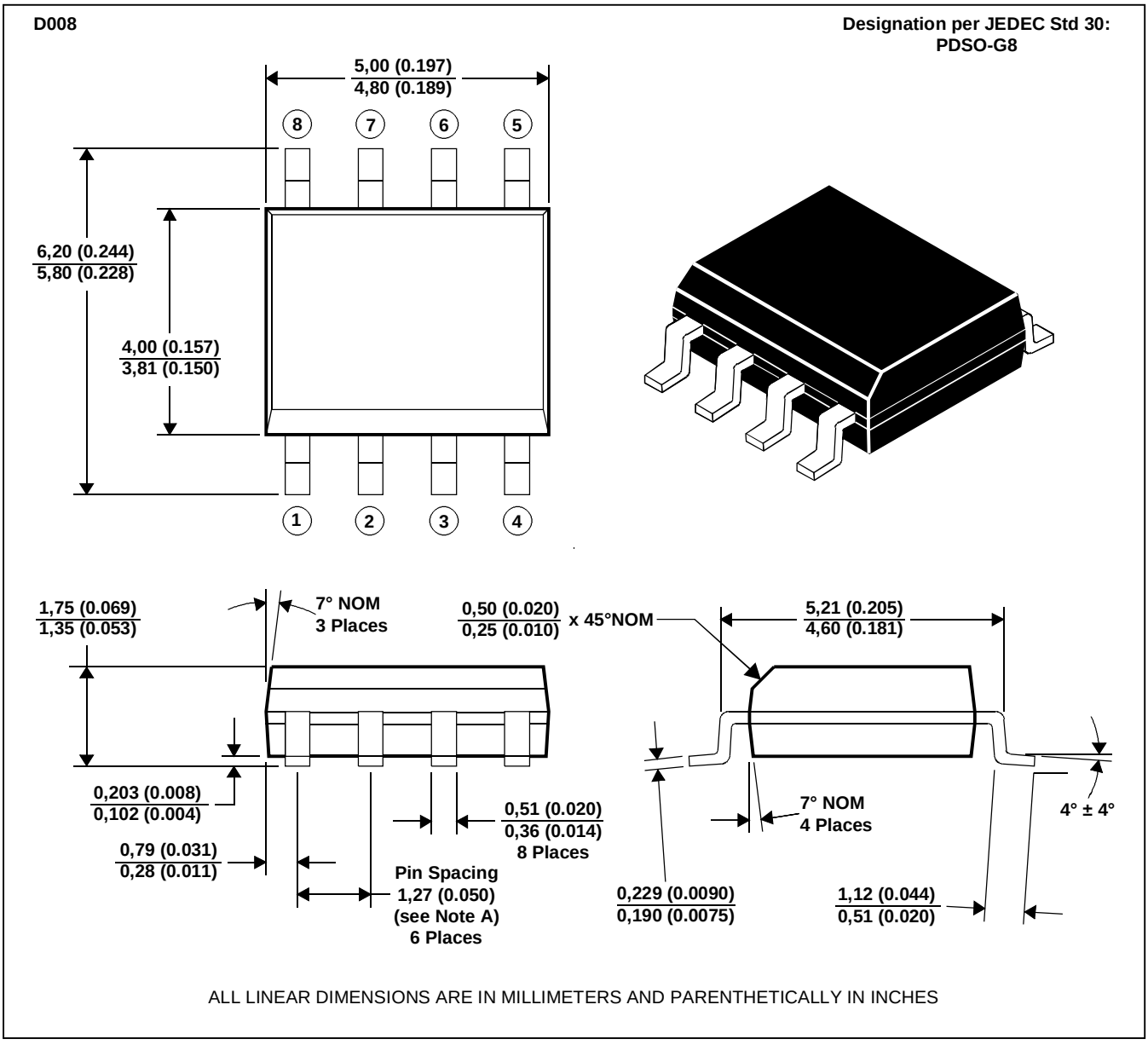
Figure 9. OVERCURRENT PROTECTOR REQUIREMENTS

MECHANICAL DATA

D008

plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



MDXXAA

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

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