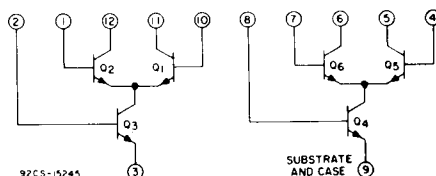


High-Reliability

Transistor Array

Dual Independent Differential Amplifier

The CA3026 (/) Series type is supplied in the 12-lead TO-5 style package.



Schematic Diagram

TABLE A. POST BURN-IN, FINAL ELECTRICAL AND GROUP A SAMPLING TESTS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS FOR INDICATED TEMPERATURES (°C)						UNITS	
			MINIMUM			MAXIMUM				
			-55	+25	+125	-55	+25	+125		
For Each Transistor :										
Collector Cutoff Current	ICBO	VCB = 10 V, IE = 0	—	—	—	0.1	0.1	20	μA	
Collector To-Base Breakdown Voltage	V(BR)CBO	IC = 10μA, IE = 0	—	20	—	—	—	—	V	
Emitter-To-Base Breakdown Voltage	V(BR)EBO	IE = 10μA, IC = 0	—	5	—	—	—	—	V	
Collector-To-Substrate Breakdown Voltage	V(BR)CIO	IC = 10μA, IC1 = 0	—	20	—	—	—	—	V	
Collector-To-Emitter Breakdown Voltage	V(BR)CEO	IC = 1mA, IB = 0	—	15	—	—	—	—	V	
Input Bias Current For Transistors Q3 and Q4	II	VCE = 3 V, IE = 2mA	—	—	—	100	50	40	μA	
Input Bias Current For Transistors Q1, Q2, Q5, and Q6	II	VCE = 3 V, IE = 1mA	—	—	—	50	25	20	μA	
Base-To-Emitter Voltage For Transistors Q3 and Q4	VBE	VCE = 3 V, IE = 1mA	0.7	0.7	0.4	1.05	0.8	0.75	V	
For Each Differential Amplifier										
Input Offset Current	IIO	VCE = 3 V, IE = 2mA	—	—	—	—	2	—	μA	
Input Offset Voltage	VIO	VCE = 3 V, IE = 2mA	—	—	—	—	5	—	mV	

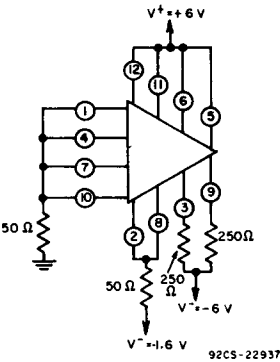
CA3026/...

TABLE B. DELTA LIMITS at $T_A = 25^{\circ}\text{C}$ (/1 only)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS	UNITS
			MAX. Δ	
Input Bias Current For Each Transistor Q1, Q2, Q5, and Q6	I_I	$V_{CE} = 3\text{V}, I_E = 2\text{mA}$	± 6.0	μA
Base-to-Emitter Voltage For Each Transistor Q3 and Q4	V_{BE}	$V_{CE} = 3\text{V}, I_E = 1\text{mA}$	± 0.1	V
Input Offset Voltage For Each Differential Amplifier	V_{IO}	$V_{CE} = 3\text{V}, I_E = 2\text{mA}$	± 2	mV

TABLE C. GROUPS C AND D END-POINT TESTS at $T_A = 25^{\circ}\text{C}$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN.	MAX.	
For Each Transistor : Collector Cutoff Current	I_{CBO}	$V_{CB} = 10\text{V}, I_E = 0$	—	0.2	μA
Input Bias Current For Transistors Q1, Q2, Q5, & Q6	I_I	$V_{CE} = 3\text{V}, I_E = 2\text{mA}$	—	28	μA
Base-to-Emitter Voltage For Transistors Q3 and Q4	V_{BE}	$V_{CE} = 3\text{V}, I_E = 1\text{mA}$	0.65	0.85	V
For Each Differential Amplifier : Input Offset Voltage	V_{IO}	$V_{CE} = 3\text{V}, I_E = 2\text{mA}$	—	6	mV



Burn-in and operating life test circuit.