Micropower No R_{SENSE} Constant Frequency Step-Down DC/DC Controller

FEATURES

- **No Current Sense Resistor Required**
- **High Output Currents Easily Achieved**
- **Internal Soft-Start Ramps V_{OUT}**
- **Wide V_{IN} Range: 2.75V to 9.8V**
- Low Dropout: 100% Duty Cycle
- Constant Frequency 550kHz Operation
- Low Ripple Pulse Skipping Operation at Light Load
- Output Voltage as Low as 0.8V
- ±1.5% Voltage Reference Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Only 8µA Supply Current in Shutdown
- Low Profile 8-Lead SOT-23 (1mm) and (3mm × 2mm) DFN (0.75mm) Packages

APPLICATIONS

- 1- or 2-Cell Li-Ion Battery-Powered Applications
- Wireless Devices
- Portable Computers
- Distributed Power Systems

DESCRIPTION

The LTC®3772B is a constant frequency current mode step-down DC/DC controller in a low profile 8-lead SOT-23 (ThinSOT™) and a 3mm × 2mm DFN package. The No R_{SENSE}™ architecture eliminates the need for a current sense resistor, improving efficiency and saving board space.

The LTC3772B automatically switches into pulse skipping operation at light loads. It consumes only 200µA of quiescent current under a no-load condition.

The LTC3772B incorporates an undervoltage lockout feature that shuts down the device when the input voltage falls below 2V. To maximize the runtime from a battery source, the external P-channel MOSFET is turned on continuously in dropout (100% duty cycle). High switching frequency of 550kHz allows the use of a small inductor and capacitors. An internal soft-start smoothly ramps the output voltage from zero to its regulation point.

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ThinSOT and No R_{SENSE} are trademarks of Linear Technology Corporation.
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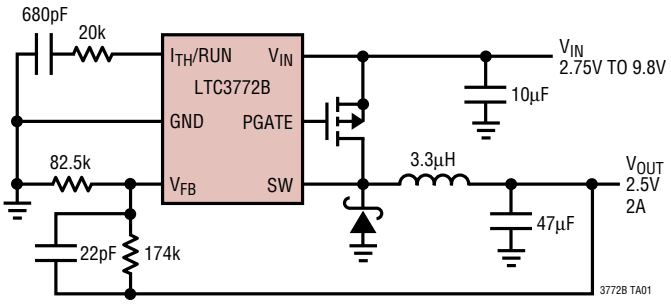
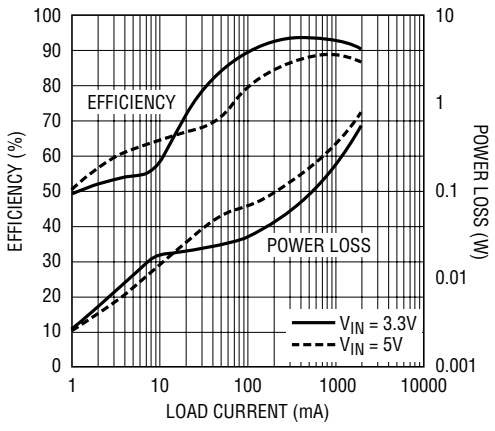
TYPICAL APPLICATION

550kHz Micropower Step-Down DC/DC Converter



Efficiency and Power Loss vs Load Current (Figure 5 Circuit)

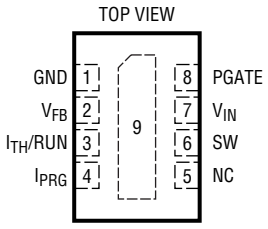


ABSOLUTE MAXIMUM RATINGS (Note 1)

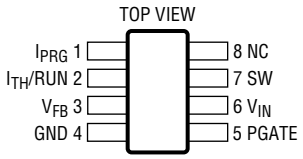
Input Supply Voltage (V_{IN}) ..... –0.3V to 10V
IPRG Voltage ..... –0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH}/RUN Voltages ..... –0.3V to 2.4V
SW Voltage ..... –2V to (V_{IN} + 1V) or 10V Maximum
PGATE Peak Output Current (<10µs) 1A

Operating Temperature Range (Note 2) .. –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
TSOT-23 ..... 300°C

PACKAGE/ORDER INFORMATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 125°C, θ_{JA} = 230°C/W

ORDER PART NUMBER	DDB PART MARKING	ORDER PART NUMBER	TS8 PART MARKING
LTC3772BEDDB	LBWP	LTC3772BETS8	LTBWN

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		●	2.75		9.8	V
Input DC Supply Current	(Note 4)					
No Load	V_{FB} = 0.83V			200	325	µA
Shutdown	V_{ITH}/RUN = 0V			8	20	µA
UVLO	V_{IN} < UVLO Threshold – 100mV			1	5	µA
Undervoltage Lockout (UVLO) Threshold	V_{IN} Rising	●		2.0	2.75	V
	V_{IN} Falling	●		1.85	2.60	V
Start-Up Current Source	V_{ITH}/RUN = 0V		0.7	1.2	1.7	µA
Shutdown Threshold (at I_{TH}/RUN)	V_{ITH}/RUN Rising	●	0.3	0.6	0.95	V
Regulated Feedback Voltage	0°C ≤ T_A ≤ 85°C (Note 5)		0.788	0.800	0.812	V
	–40°C ≤ T_A ≤ 85°C (Note 5)	●	0.780	0.800	0.812	V
Feedback Voltage Line Regulation	2.75V ≤ V_{IN} ≤ 9V (Note 5)			0.08	0.2	mV/V
Feedback Voltage Load Regulation	I_{TH}/RUN = 1.6V (Note 5)			0.5	0.2	%
	I_{TH}/RUN = 1V (Note 5)			–0.5	–0.2	%

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB} Input Current	(Note 5)		–10	2	10	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.850	0.880	0.910	V
Overvoltage Protect Hysteresis				40		mV
Oscillator Frequency Normal Operation Output Short Circuit	 V_{FB} = 0.8V V_{FB} = 0V		 500	 550 200	 650	 kHz kHz
Gate Drive Rise Time	C_{LOAD} = 3000pF			40		ns
Gate Drive Fall Time	C_{LOAD} = 3000pF			40		ns
Peak Current Sense Voltage	I_{PRG} = GND (Note 6) I_{PRG} = Floating I_{PRG} = V_{IN}	● ● ●	55 120 190	70 138 208	85 155 225	mV mV mV
Default Soft-Start Time	Time for V_{FB} to Ramp from 0.05V to 0.75V			0.8		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3772BETS8/LTC3772BEDDB are guaranteed to meet specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$

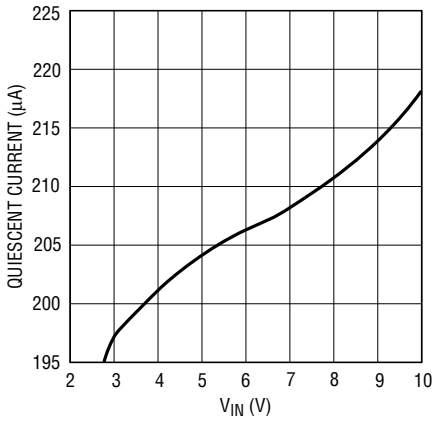
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: The LTC3772B is tested in a feedback loop that servos V_{FB} to the output of the error amplifier while maintaining I_{TH}/RUN at the midpoint of the current limit range.

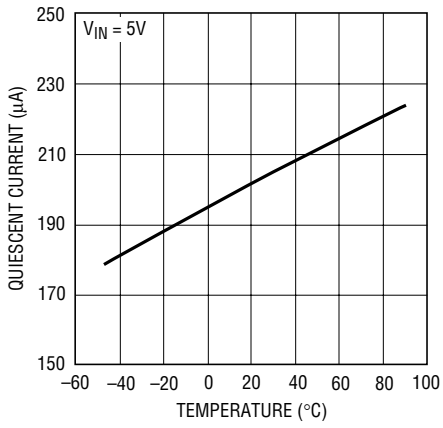
Note 6: Peak current sense voltage is reduced dependent on duty cycle as given in Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS

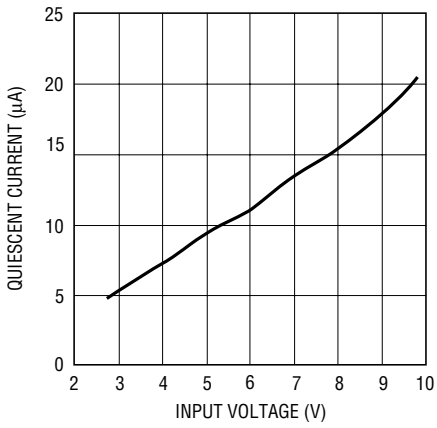
Quiescent Current (No Load) vs Input Voltage



Quiescent Current (No Load) vs Temperature

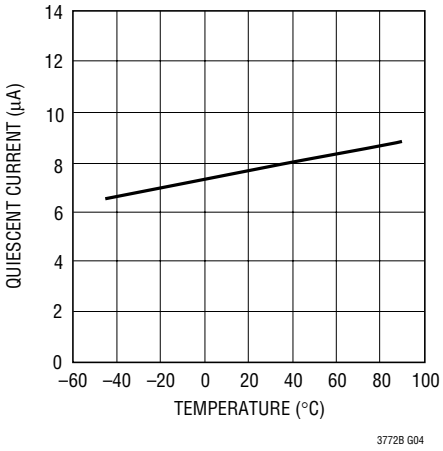


Quiescent Current (Shutdown) vs Input Voltage



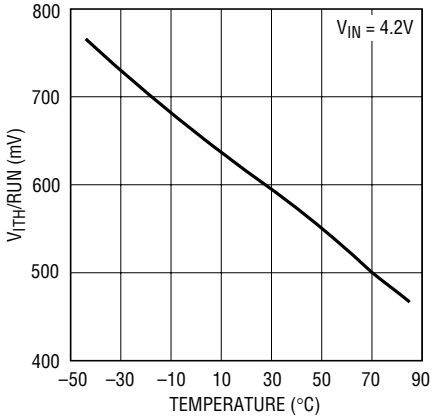
TYPICAL PERFORMANCE CHARACTERISTICS

Quiescent Current (Shutdown) vs Temperature



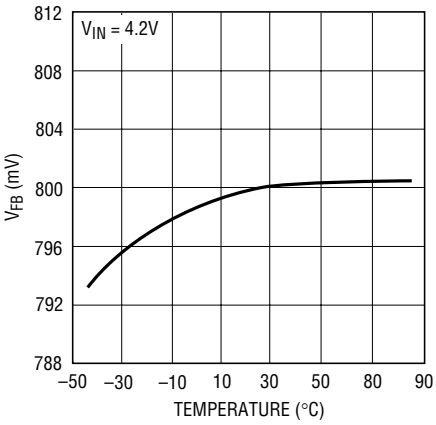
3772B G04

Shutdown Threshold vs Temperature



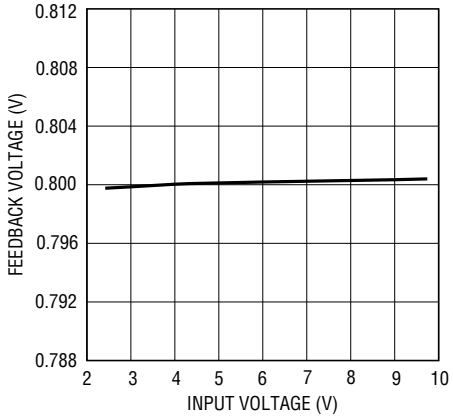
3772B G05

Regulated Feedback Voltage vs Temperature



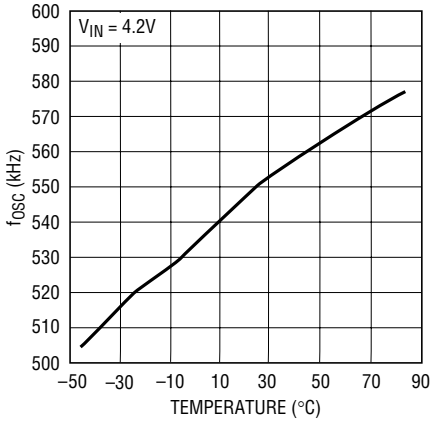
3772B G06

Regulated Feedback Voltage vs Input Voltage



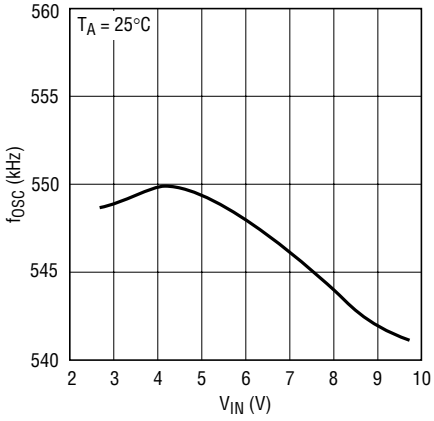
3772B G07

Oscillator Frequency vs Temperature



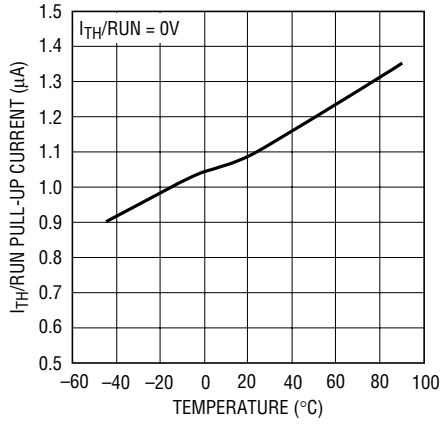
3772B G08

Oscillator Frequency vs Input Voltage



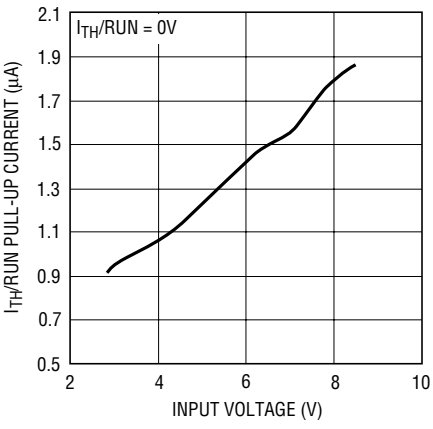
3772B G09

I_{TH}/RUN Start-Up Current vs Temperature



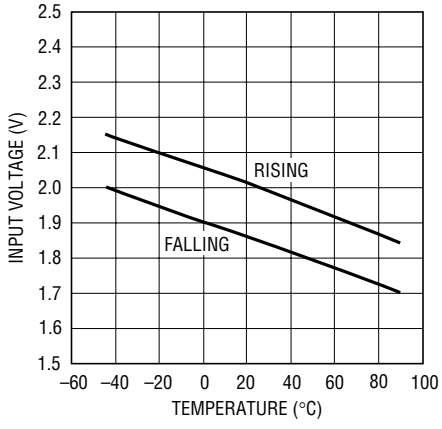
3772B FG10

I_{TH}/RUN Start-Up Current vs Input Voltage



3772B G11

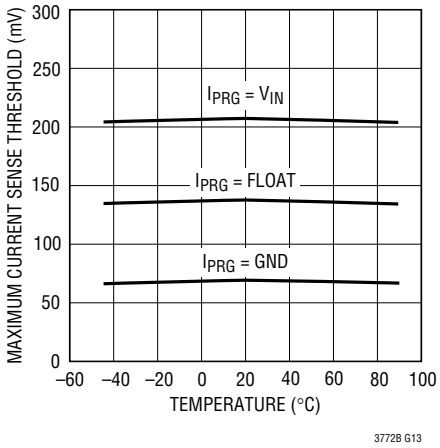
Undervoltage Lockout Thresholds vs Temperature



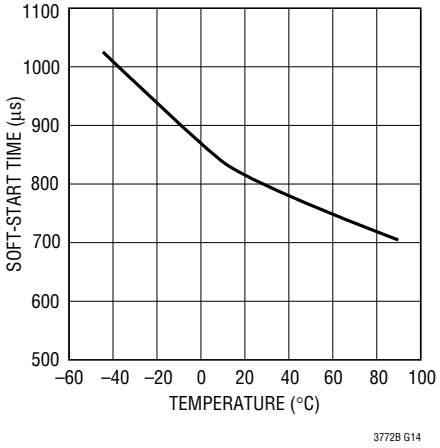
3772B G12

TYPICAL PERFORMANCE CHARACTERISTICS

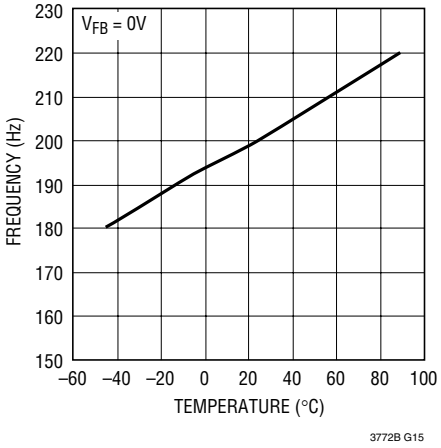
Maximum Current Sense Threshold vs Temperature



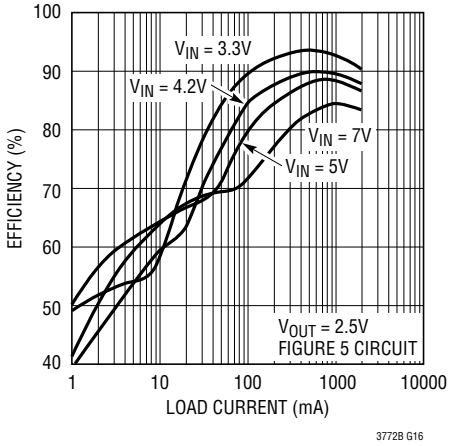
Soft-Start Time vs Temperature



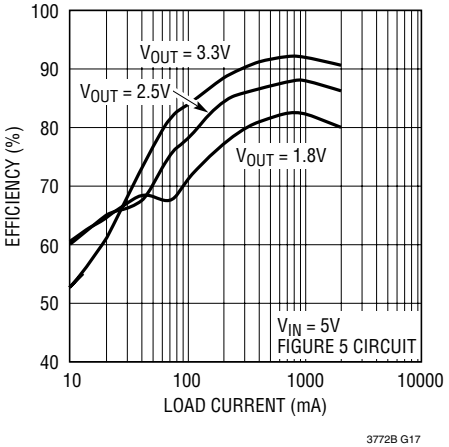
Foldback Frequency vs Temperature



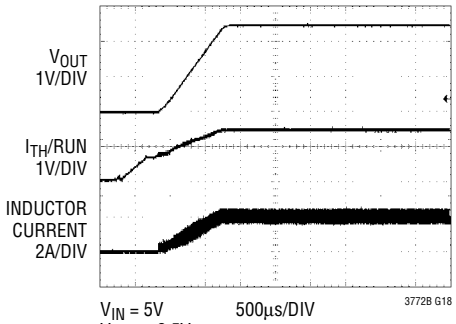
Efficiency vs Load Current



Efficiency vs Load Current

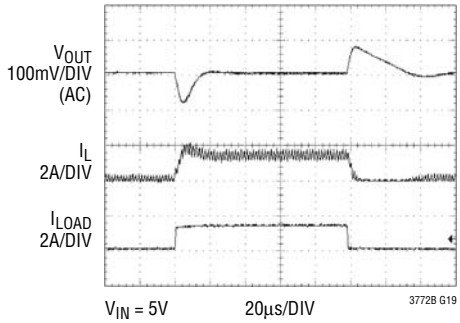


Start-Up



VIN = 5V 500µs/DIV
VOUT = 2.5V
RLOAD = 1.5Ω
FIGURE 5 CIRCUIT

Load Step



VIN = 5V 20µs/DIV
VOUT = 2.5V
ILOAD = 100mA TO 1.5A
FIGURE 5 CIRCUIT

PIN FUNCTIONS (DDB/TS8)

GND (Pin 1/Pin 4): Ground Pin.

V_{FB} (Pin 2/Pin 3): Receives the feedback voltage from an external resistor divider across the output.

I_{TH}/RUN (Pin 3/Pin 2): This pin performs two functions. It serves as the error amplifier compensation point as well as the run control input. Nominal voltage range for this pin is 0.7V to 1.9V. Forcing this pin below 0.6V causes the device to be shut down. In shutdown, all functions are disabled and the PGATE pin is held high.

I_{PRG} (Pin 4/Pin 1): Current Sense Limit Pin. Three-state pin selects maximum peak sense voltage threshold. The pin selects the maximum voltage drop across the external P-channel MOSFET. Tie to V_{IN}, GND or float to select 208mV, 70mV or 138mV respectively.

NC (Pin 5/Pin 8): No Connection Required.

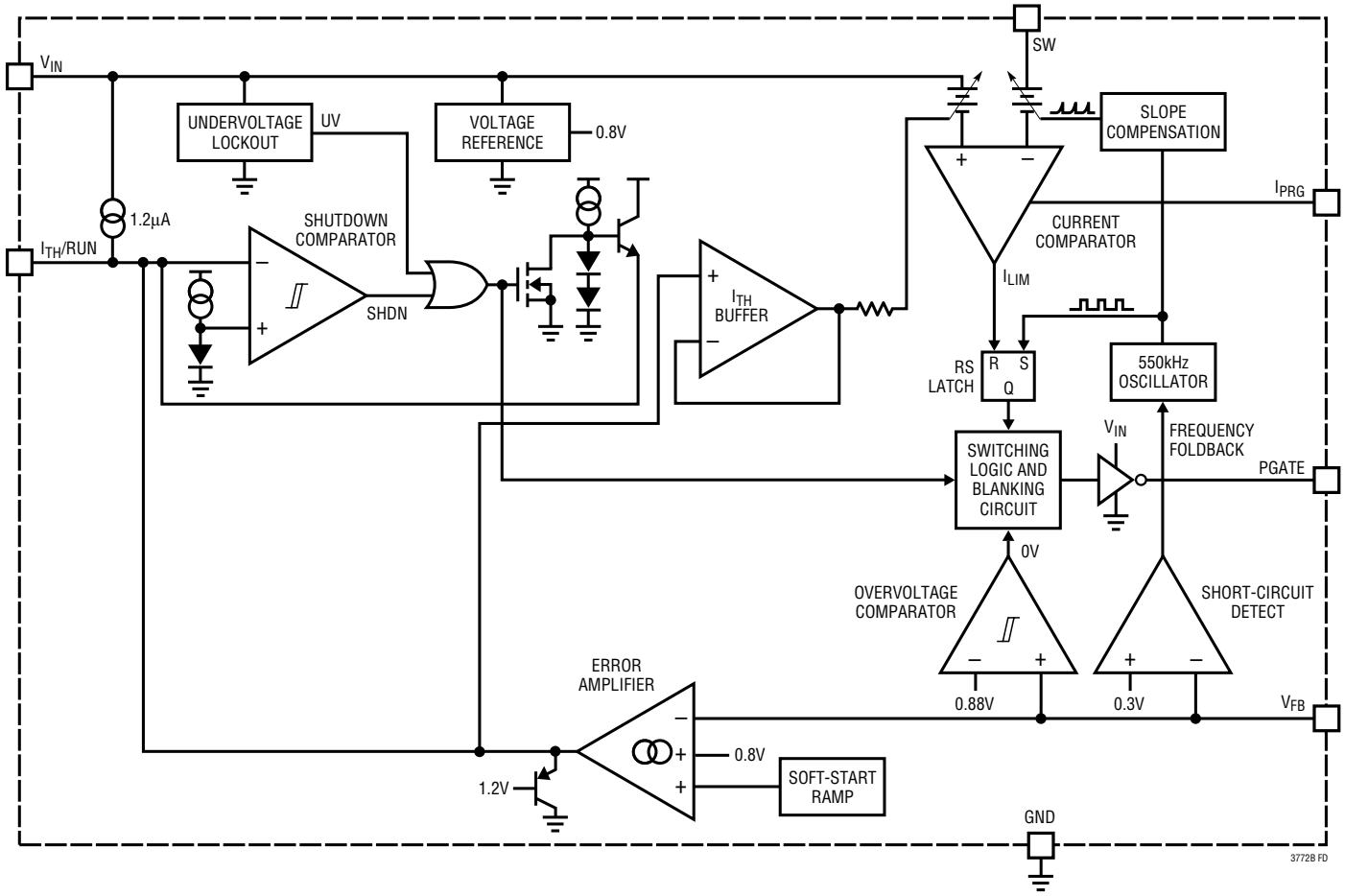
SW (Pin 6/Pin 7): Switch Node Connection to Inductor and Current Sense Input Pin. Normally, the external P-channel MOSFET's drain is connected to this pin.

V_{IN} (Pin 7/Pin 6): Supply and Current Sense Input Pin. This pin must be closely decoupled to GND (Pin 4). Normally the external P-channel MOSFET's source is connected to this pin.

PGATE (Pin 8/Pin 5): Gate Drive for the External P-Channel MOSFET. This pin swings from 0V to V_{IN}.

Exposed Pad (Pin 9, DDB Only): The Exposed Pad is ground and must be soldered to the PCB for electrical connection and optimum thermal performance.

FUNCTIONAL DIAGRAM



OPERATION (Refer to the Functional Diagram)

Main Control Loop (Normal Operation)

The LTC3772B is a constant frequency current mode step-down switching regulator controller. During normal operation, the external P-channel MOSFET is turned on each cycle when the oscillator sets the RS latch and turned off when the current comparator resets the latch. The peak inductor current at which the current comparator trips is controlled by the voltage on the I_{TH}/RUN pin, which is the output of the error amplifier. The negative input to the error amplifier is the output feedback voltage V_{FB}, which is generated by an external resistor divider connected between V_{OUT} and ground. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH}/RUN voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling the I_{TH}/RUN pin to ground. Releasing the I_{TH}/RUN pin allows an internal 1μA current source to charge up the external compensation network. When the I_{TH}/RUN pin voltage reaches approximately 0.6V, the main control loop is enabled and the I_{TH}/RUN voltage is pulled up by a clamp to its zero current level of approximately one diode voltage drop (0.7V). As the external compensation network continues to charge up, the corresponding peak inductor current level follows, allowing normal operation. The maximum peak inductor current attainable is set by a clamp on the I_{TH}/RUN pin at 1.2V above the zero current level (approximately 1.9V).

Dropout Operation

When the input supply voltage decreases towards the output voltage, the rate of change of inductor current during the on cycle decreases. This reduction means that at some input-output differential, the external P-channel MOSFET will remain on for more than one oscillator cycle (start dropping off-cycles) since the inductor current has not ramped up to the threshold set by the error amplifier. Further reduction in input supply voltage will eventually cause the external P-channel MOSFET to be turned on 100%; i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the sense resistor, the MOSFET and the inductor.

Undervoltage Lockout Protection

To prevent operation of the external P-channel MOSFET with insufficient gate drive, an undervoltage lockout circuit is incorporated into the LTC3772B. When the input supply voltage drops below approximately 2V, the P-channel MOSFET and all internal circuitry other than the undervoltage block itself are turned off. Input supply current in undervoltage is approximately 1μA.

Short-Circuit Protection

If the output is shorted to ground, the frequency of the oscillator is folded back from 550kHz to approximately 200kHz while maintaining the same minimum on time. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. After the short is removed, the oscillator frequency will gradually increase back to 550kHz as V_{FB} rises through 0.3V on its way back to 0.8V.

Overvoltage Protection

If V_{FB} exceeds its regulation point of 0.8V by more than 10% for any reason, such as an output short-circuit to a higher voltage, the overvoltage comparator will hold the external P-channel MOSFET off. This comparator has a typical hysteresis of 40mV.

Peak Current Sense Voltage Selection and Slope Compensation (I_{PRG} Pins)

When a controller is operating below 20% duty cycle, the maximum sense voltage allowed across the external P-channel MOSFET is 138mV, 70mV or 208mV for the three respective states of the I_{PRG} pin.

OPERATION (Refer to the Functional Diagram)

However, once the controller's duty cycle exceeds 20%, slope compensation begins and effectively reduces the peak sense voltage by an amount given by the curve in Figure 1.

The peak inductor current is determined by the peak sense voltage and the on-resistance of the external P-channel MOSFET:

$$I_{PEAK} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}}$$

Soft-Start

The start-up of V_{OUT} is controlled by the LTC3772B internal soft-start. During soft-start, the error amplifier compares the feedback signal V_{FB} to the internal soft-start ramp (instead of the 0.8V reference), which rises linearly from 0V to 0.8V in about 0.6ms. This allows the output voltage to rise smoothly from 0V to its final value, while maintaining control of the inductor current. After the soft-start is timed out, it is disabled until the part is put in shutdown again or the input supply is cycled.

Light Load Current Operation

Under very light load current conditions, the I_{TH}/RUN pin voltage will be very close to the zero current level of 0.85V. As the load current decreases further, an internal offset at the current comparator input will assure that the current comparator remains tripped (even at zero load current) and the regulator will start to skip cycles, as it must, in order to maintain regulation. This behavior allows the regulator to maintain constant frequency down to very light loads, resulting in low output ripple as well as low audio noise and reduced RF interference, while providing high light load efficiency.

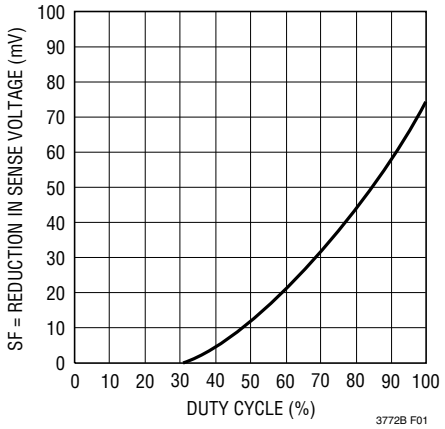


Figure 1. Reduction in Sense Voltage Due to Slope Compensation vs Duty Cycle

APPLICATIONS INFORMATION

The basic LTC3772B application circuit is shown on the front page of this data sheet. The load requirement drives the selection of external components: the power MOSFET, inductor and output diode, as well as the input bypass capacitor C_{IN} and output bypass capacitor C_{OUT}.

Power MOSFET Selection

An external P-channel power MOSFET must be selected for use with the LTC3772B. The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$, the "on" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and total gate charge.

Since the LTC3772B is designed for operation down to low input voltages, a sublogic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at V_{GS} = 2.5V) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the LTC3772B is less than the absolute maximum V_{GS} rating.

The P-channel MOSFET's on-resistance is chosen based on the required load current. The maximum average output load current $I_{OUT(MAX)}$ is equal to the peak inductor current minus half the peak-to-peak ripple current I_{RIPPLE}. The LTC3772B's current comparator monitors the drain-to-source voltage V_{DS} of the P-channel MOSFET, which is sensed between the V_{IN} and SW pins. The peak inductor current is limited by the current threshold, set by the voltage on the I_{TH} pin of the current comparator. The voltage on the I_{TH} pin is internally clamped, which limits the maximum current sense threshold $\Delta V_{SENSE(MAX)}$ to approximately 138mV when I_{PRG} is floating (70mV when I_{PRG} is tied low; 208mV when I_{PRG} is tied high).

The output current that the LTC3772B can provide is given by:

$$I_{OUT(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{DS(ON)}} - \frac{I_{RIPPLE}}{2}$$

A reasonable starting point is setting ripple current I_{RIPPLE} to be 40% of $I_{OUT(MAX)}$. Rearranging the above equation yields:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet \frac{\Delta V_{SENSE(MAX)}}{I_{OUT(MAX)}}$$

for Duty Cycle < 20%.

However, for operation above 20% duty cycle, slope compensation has to be taken into consideration to select the appropriate value of $R_{DS(ON)}$ for the required amount of load current:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet \frac{\Delta V_{SENSE(MAX)} - SF}{I_{OUT(MAX)}}$$

where SF is a factor whose value is obtained from the curve in Figure 1.

These must be further derated to take into account the significant variation in on-resistance with temperature. The following equation is a good guide for determining the required $R_{DS(ON)MAX}$ at 25°C (manufacturer's specification), allowing some margin for variations in the LTC3772B and external component values:

$$R_{DS(ON)(MAX)} = \frac{5}{6} \bullet 0.9 \bullet \frac{\Delta V_{SENSE(MAX)} - SF}{I_{OUT(MAX)} \bullet \rho_T}$$

The ρ_T is a normalizing term accounting for the temperature variation in on-resistance, which is typically about 0.4%/°C, as shown in Figure 2. Junction to case temperature T_{JC} is about 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80°C} \cong 1.3$ in the above equation is a reasonable choice.

The required minimum $R_{DS(ON)}$ of the MOSFET is also governed by its allowable power dissipation. For applications that may operate the LTC3772B in dropout–i.e., 100%

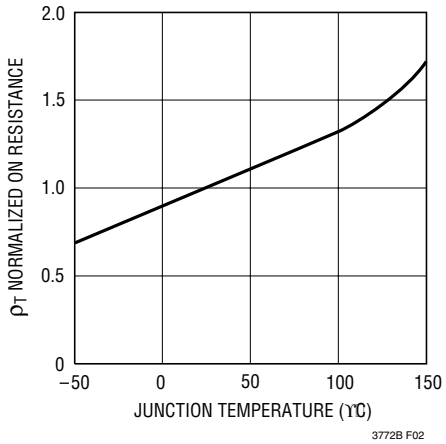


Figure 2. $R_{DS(ON)}$ vs Temperature

APPLICATIONS INFORMATION

duty cycle–at its worst case the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)(DC=100\%)} = \frac{P_P}{(I_{OUT(MAX)})^2(1+\delta_P)}$$

where P_P is the allowable power dissipation and δ_P is the temperature dependency of $R_{DS(ON)}$. $(1 + \delta_P)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta_P = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

In applications where the maximum duty cycle is less than 100% and the LTC3772B is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} \cong \frac{P_P}{(DC)I_{OUT}^2(1+\delta_P)}$$

where DC is the maximum operating duty cycle of the LTC3772B.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses.

The inductance value also has a direct effect on ripple current. In normal operation, the ripple current, I_{RIPPLE}, decreases with higher inductance or frequency and increases with higher V_{IN} or as V_{OUT} approaches 1/2 V_{IN}. The inductor's peak-to-peak ripple current is given by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f(L)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

where f is the operating frequency. V_D is the forward voltage drop of the catch diode, 0.5V typical. Accepting larger values of I_{RIPPLE} allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $I_{RIPPLE} = 0.4(I_{OUT(MAX)})$. Remember, the maximum I_{RIPPLE} occurs at the maximum input voltage.

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko and Sumida.

Output Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel switch duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Under this condition the diode must safely handle I_{PEAK} at close to 100% duty cycle. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

APPLICATIONS INFORMATION

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) I_{OUT}$$

The allowable forward voltage drop in the diode is calculated from the maximum short-circuit current as:

$$V_F \cong \frac{P_D}{I_{PEAK}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements.

A fast switching diode must also be used to optimize efficiency. Schottky diodes are a good choice for low forward drop and fast switching times. Remember to keep lead length short and observe proper grounding to avoid ringing and increased dissipation.

An additional consideration in applications where low no-load quiescent current is critical is the reverse leakage current of the diode at the regulated output voltage. A leakage greater than several microamperes can represent a significant percentage of the total input current.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The output filtering capacitor C smooths out current flow from the inductor to the load, help maintain a steady output voltage during transient load changes and reduce output voltage ripple. The capacitors must be selected with sufficiently low ESR to minimize voltage ripple and load step transients and sufficiently bulk capacitance to ensure the control loop stability.

The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

APPLICATIONS INFORMATION

For ceramic capacitors, use X7R or X5R types: do not use Y5V. Manufacturers include AVX, Kemet, Murata, Taiyo Yuden and TDK.

Setting Output Voltage

The LTC3772B output voltages are each set by an external feedback resistor divider carefully placed across the output as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feed-forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

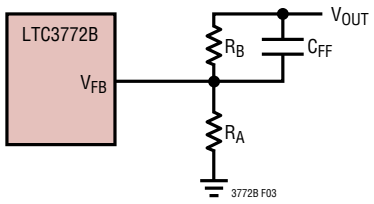


Figure 3. Setting Output Voltage

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (\eta 1 + \eta 2 + \eta 3 + ...)$$

where $\eta 1$, $\eta 2$, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3772B circuits: 1) LTC3772B DC bias current, 2) MOSFET gate charge current, 3) I^2R losses, 4) voltage drop of the output diode and 5) external MOSFET transition losses.

1. The V_{IN} current is the DC supply current, given in the electrical characteristics, that excludes MOSFET driver and control currents. V_{IN} current results in a small loss which increases with V_{IN}.
2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = (f)(dQ)$.
3. I^2R losses are predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L but is "chopped" between the P-channel MOSFET (in series with R_{SENSE}) and the output diode. The MOSFET $R_{DS(ON)}$ plus R_{SENSE} multiplied by duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses.
4. The output diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage times the diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of 0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A.
5. Transition losses apply to the external MOSFET and increase at higher operating frequencies and input voltages. Transition losses can be estimated from:

   $$\text{Transition Loss} = 2(V_{IN})^2 I_{O(MAX)} C_{RSS} (f)$$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Foldback Current Limiting

As described in the Output Diode Selection, the worst-case dissipation occurs with a short-circuited output when the diode conducts the current limit value almost continuously.

APPLICATIONS INFORMATION

To prevent excessive heating in the diode, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH}/RUN pin as shown in Figure 4. In a hard short (V_{OUT} = 0V), the current will be reduced to approximately 50% of the maximum output current.

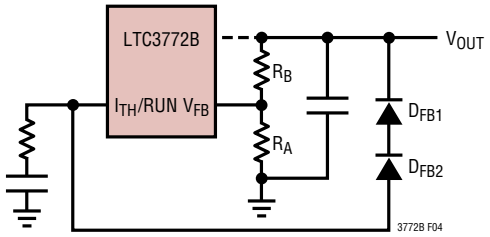


Figure 4. Foldback Current Limiting

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD})(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then returns V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values.

The I_{TH} series R_C-C_C filter (see Functional Diagram) sets the dominant pole-zero loop compensation. The I_{TH} external components shown in the Figure 5 circuit will provide an adequate starting point for most applications. The values can be modified slightly (from 0.2 to 5 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25)(C_{LOAD}). Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Minimum On-Time Considerations

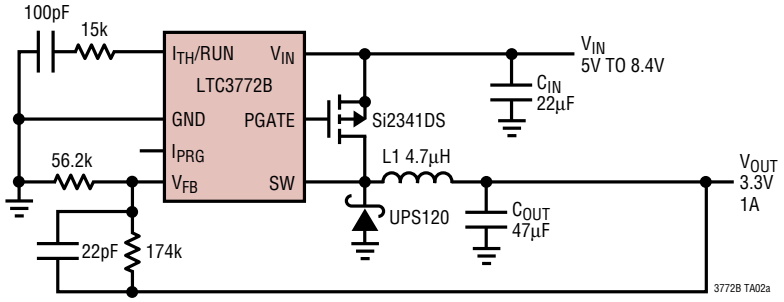
Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC3772B is capable of turning the top MOSFET on and then off. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. The minimum on-time for the LTC3772B is about 250ns. Low duty cycle and high frequency applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{f \bullet V_{IN}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3772B will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

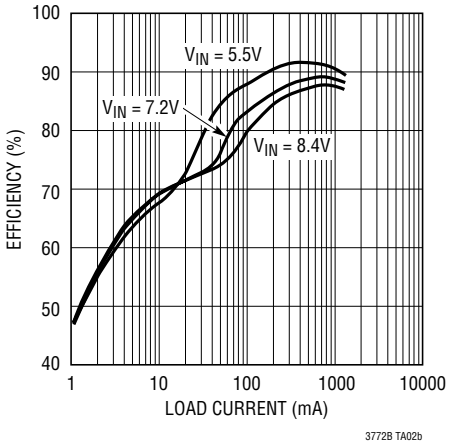
TYPICAL APPLICATIONS

550kHz Micropower, 1A, 2-Cell Li-Ion to 3.3V_{OUT} Step-Down DC/DC Converter

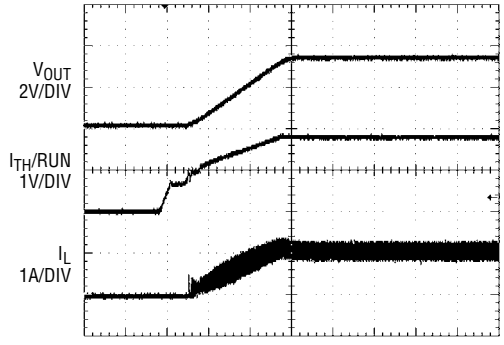


L1: SUMIDA CR43-4R7
C_{IN}: MURATA GRM32ER61C226KA65B
C_{OUT}: MURATA GRM32ER60J476ME20B

Efficiency vs Load Current

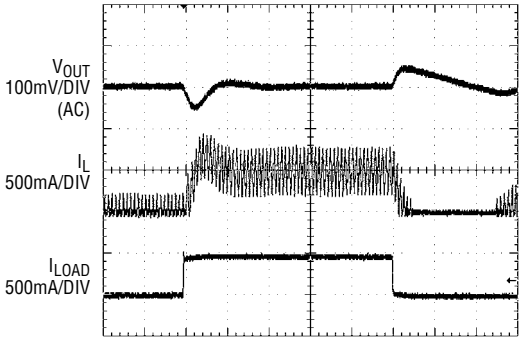


Start-Up



V_{IN} = 5.5V
V_{OUT} = 3.3V
R_{LOAD} = 3Ω
400µs/DIV

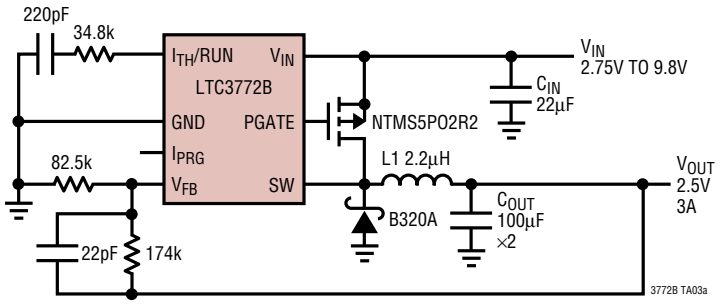
Load Step



V_{IN} = 5.5V
V_{OUT} = 3.3V
I_{LOAD} = 40mA TO 500mA
20µs/DIV

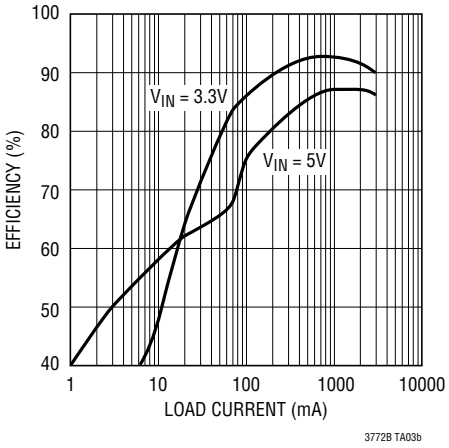
TYPICAL APPLICATIONS

550kHz Micropower 3A Step-Down DC/DC Converter

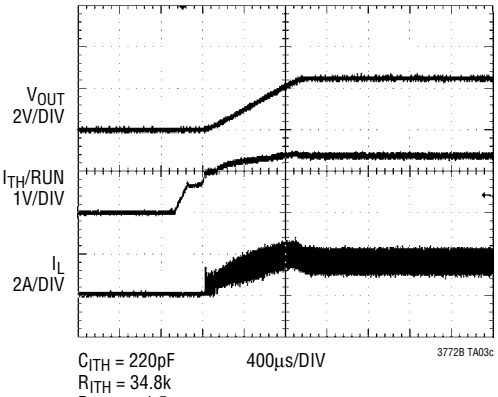


L1: VISHAY IHLP-2525CZ-01
C_{IN}: GRM32ER61A220KA65B
C_{OUT}: TAIYO YUDEN LDK375BJ107MM

Efficiency vs Load Current

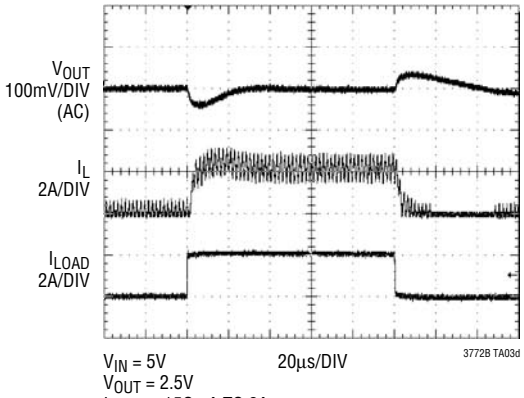


Start-Up



C_{ITH} = 220pF
R_{ITH} = 34.8k
R_{LOAD} = 1.5Ω
400µs/DIV

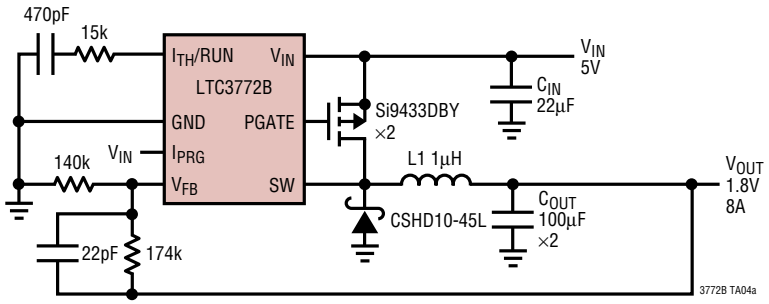
Load Step



V_{IN} = 5V
V_{OUT} = 2.5V
I_{LOAD} = 150mA TO 2A
20µs/DIV

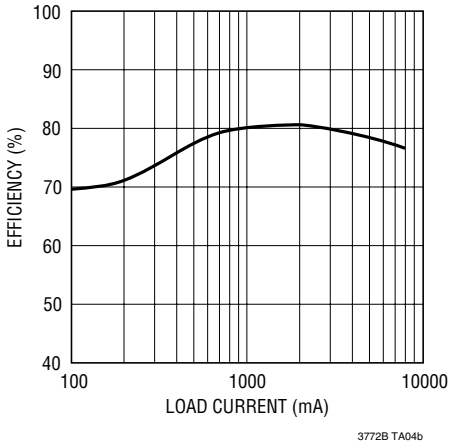
TYPICAL APPLICATIONS

550kHz Micropower 5V$_{IN}$ to 1.8V$_{OUT}$ at 8A DC/DC Converter

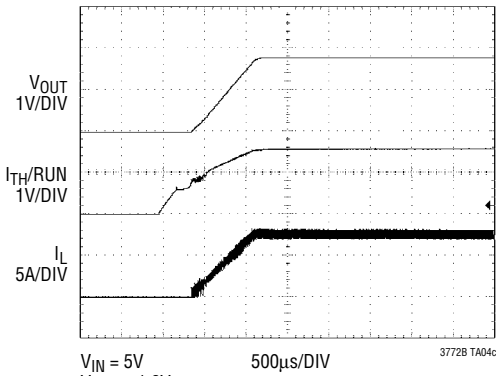


L1: TOKO FDV0630-1R0
C_{IN}: MURATA GRM32ER61C226K
C_{OUT}: MURATA GRM32ER60J107K

Efficiency vs Load Current

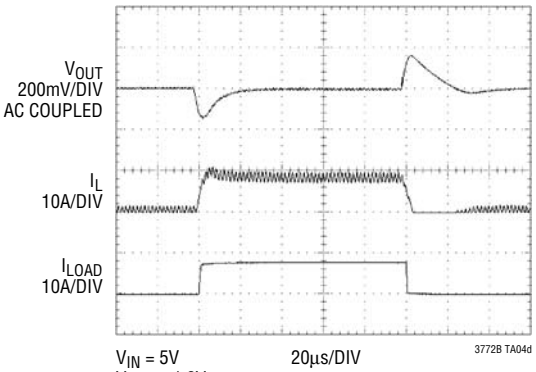


Start-Up



V_{IN} = 5V
V_{OUT} = 1.8V
R_{LOAD} = 0.25Ω
500µs/DIV

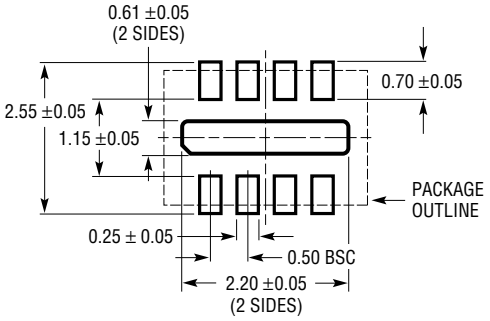
Load Step



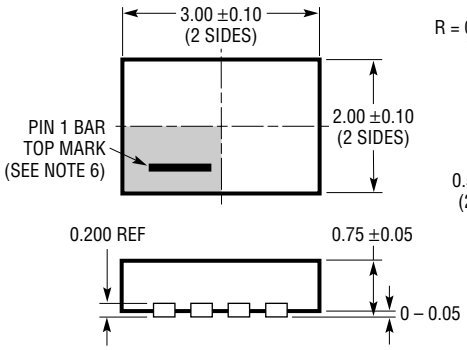
V_{IN} = 5V
V_{OUT} = 1.8V
I_{LOAD} = 800mA TO 8A
20µs/DIV

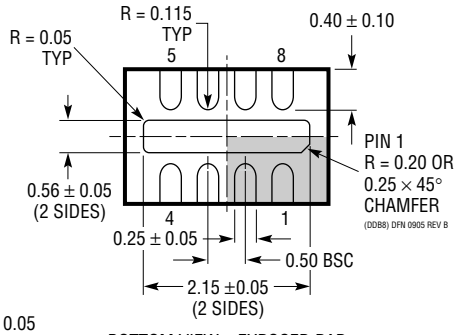
PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



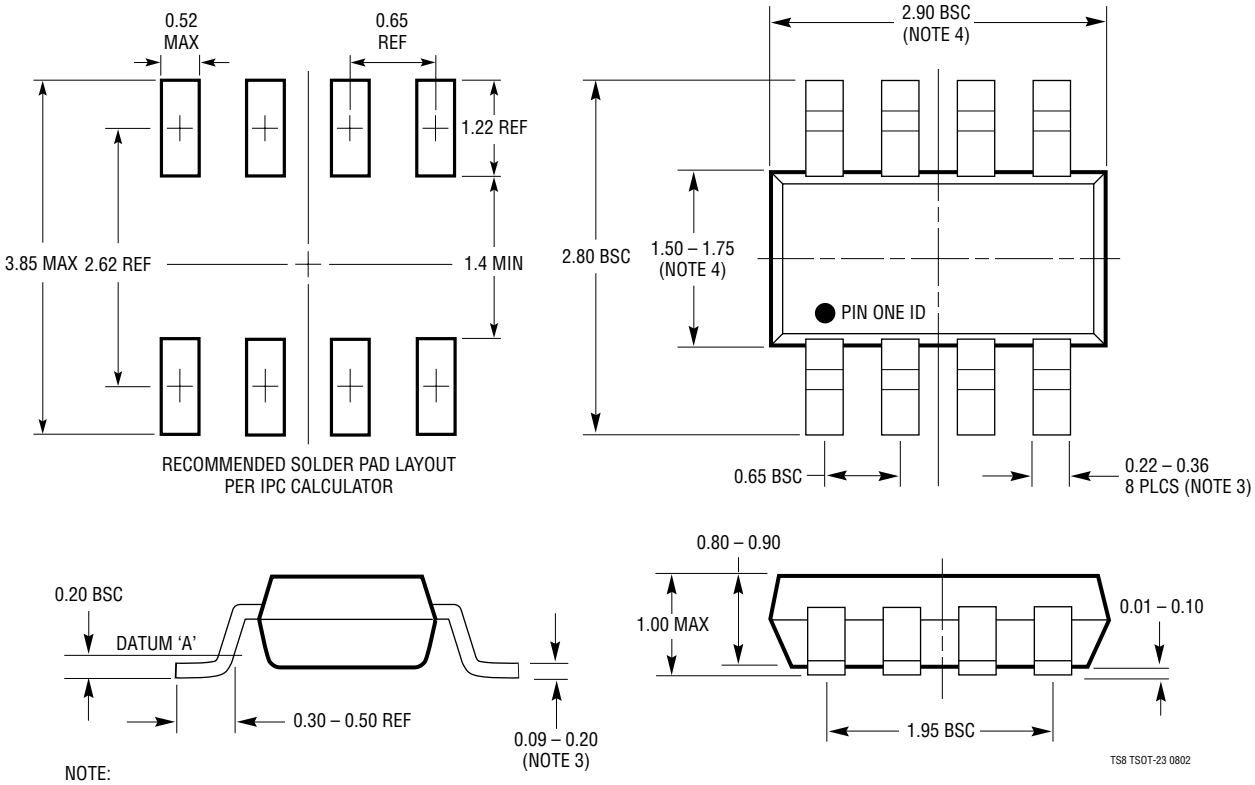


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

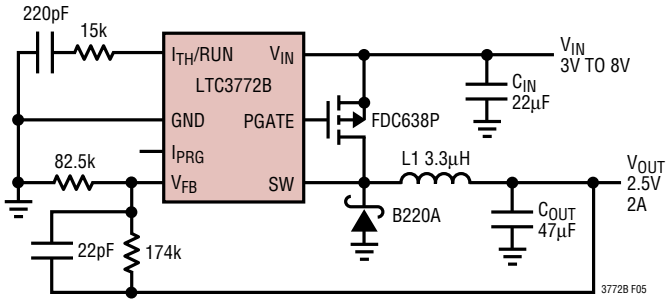
TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION



L1: TOKO D53LC #A915AY-3R3M
C_{IN}: TAIYO YUDEN LMK316BJ226ML
C_{OUT}: TAIYO YUDEN JMK325BJ476MM

Figure 5. 550kHz Micropower Step-Down DC/DC Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1624	High Efficiency SO-8 N-Channel Switching Regulator Controller	N-Channel Drive, $3.5V \le V_{IN} \le 36V$
LTC1625	No R_{SENSE}™ Synchronous Step-Down Regulator	97% Efficiency, No Sense Resistor
LTC1772/LTC1772B	550kHz ThinSOT Step-Down DC/DC Controllers	$2.5V \le V_{IN} \le 9.8V$, $V_{OUT} \ge 0.8V$, $I_{OUT} \le 6A$
LTC1778/LTC1778-1	No R_{SENSE} Current Mode Synchronous Step-Down Controllers	$4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)(V_{IN})$, I_{OUT} Up to 20A
LTC1872/LTC1872B	550kHz ThinSOT Step-Up DC/DC Controllers	$2.5V \le V_{IN} \le 9.8V$; 90% Efficiency
LTC3411/LTC3412	1.25A/2.5A, 4MHz Monolithic Synchronous Step-Down Converter	95% Efficiency, $2.5V \le V_{IN} \le 5.5V$, $V_{OUT} \ge 0.8V$, TSSOP16 Exposed Pad Package
LTC3414	4A, 4MHz Monolithic Synchronous Step-Down Converter	95% Efficiency, $2.5V \le V_{IN} \le 5.5V$, $V_{OUT} \ge 0.8V$, TSSOP20 Exposed Pad Package
LTC3418	8A, 4MHz Monolithic Synchronous Step-Down Converter	95% Efficiency, $2.5V \le V_{IN} \le 5.5V$, $V_{OUT} \ge 0.8V$, TSSOP20 Exposed Pad Package
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	$2.5V \le V_{IN} \le 5.5V$, Single Inductor
LTC3736/LTC3736-2	Dual, 2-Phase, No R_{SENSE} Synchronous Controller with Output Tracking	V_{IN}: 2.75V to 9.8V, I_{OUT} Up to 5A, 4mm × 4mm QFN Package
LTC3736-1	Dual, 2-Phase, No R_{SENSE} Synchronous Controller with Spread Spectrum	V_{IN}: 2.75V to 9.8V, Spread Spectrum Operation, Output Voltage Tracking, 4mm × 4mm QFN Package
LTC3737	Dual, 2-Phase, No R_{SENSE} Controller with Output Tracking	V_{IN}: 2.75V to 9.8V, I_{OUT} Up to 5A, 4mm × 4mm QFN Package
LTC3772	Micropower No R_{SENSE} Constant Frequency Controller	V_{IN}: 2.75V to 9.8V, I_{OUT} Up to 5A, ThinSOT, 3mm × 2mm DFN Package
LTC3776	Dual, 2-Phase, No R_{SENSE} Synchronous Controller for DDR/QDR Memory Termination	Provides V_{DDQ} and V_{TT} with one IC, $2.75V \le V_{IN} \le 9.8V$, Adjustable Constant Frequency with PLL Up to 850kHz, Spread Spectrum Operation, 4mm × 4mm QFN and 16-Lead SSOP Packages
LTC3808	No R_{SENSE}, Low EMI, Synchronous Step-Down Controller with Output Tracking	$2.75V \le V_{IN} \le 9.8V$, Spread Spectrum Operation, 3mm × 4mm DFN and 16-Lead SSOP Packages
LTC3809/LTC3809-1	No R_{SENSE}, Synchronous Step-Down Controller	$2.75V \le V_{IN} \le 9.8V$, 3mm × 4mm DFN and 10-Lead MSOP Packages

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