Product Specification

PE42451

SP5T Absorptive UltraCMOS™ High-Isolation RF Switch 450-4000 MHz, Vss_{EXT} option

Features

- HaRP™-enhanced UltraCMOS™ device
- Five symmetric, absorptive RF ports
- High Isolation:
  - 68 dB at 450 MHz
  - 62 dB at 900 MHz
  - 55 dB at 2100 MHz
  - 53 dB at 2600 MHz
  - 50 dB at 4000 MHz
- IIP2 of 95 dBm, IIP3 of 58 dBm
- High ESD tolerance of 3500 V HBM
- Optional External Vss Control (Vss_{EXT})
- Three pin CMOS logic control
- No blocking capacitors required
- Small RoHS-Compliant 24-lead 4x4 mm QFN package

Product Description

The PE42451 is a HaRP™-enhanced Absorptive SP5T RF Switch developed on the UltraCMOS™ process technology. This general purpose switch is comprised of five symmetric RF ports and has very high isolation. An on-chip CMOS decode logic facilitates a three-pin low voltage CMOS control interface and an optional external Vss feature (Vss_{EXT}). High ESD tolerance and no blocking capacitor requirements make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

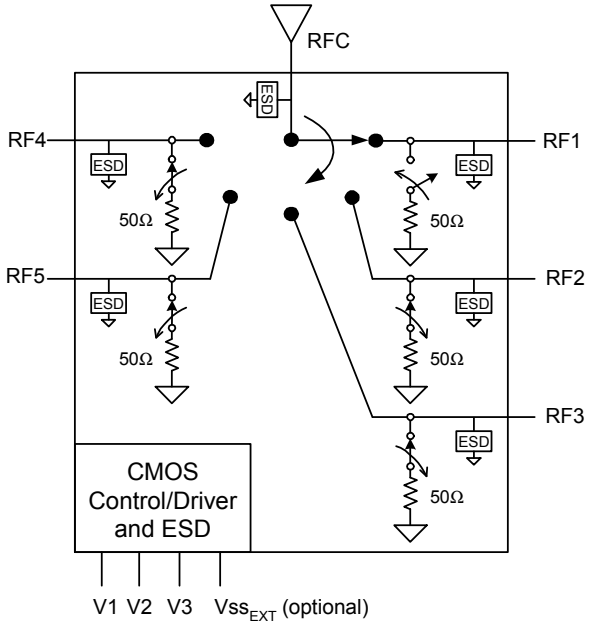
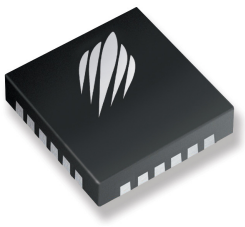


Figure 2. Package Photo

24-lead 4x4x0.85 mm QFN Package



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Table 1. Electrical Specifications @ 25 °C, V_{DD} = 3.0 V (Z_S = Z_L = 50 Ω)

Electrical Parameter	Path	Condition	Min	Typ	Max	Unit
Operating Frequency			450		4000	MHz
Insertion Loss, IL	RFC - RFX RFC - RFX RFC - RFX RFC - RFX RFC - RFX	450 MHz 900 MHz 2100 MHz 2600 MHz 4000 MHz		1.6 1.65 1.95 2.05 2.25	1.95 2.05 2.30 2.40 2.75	dB dB dB dB dB
Isolation, Iso	RFC/RFX - RFX RFC/RFX - RFX RFC/RFX - RFX RFC/RFX - RFX RFC/RFX - RFX	450 MHz 900 MHz 2100 MHz 2600 MHz 4000 MHz	58.5 53.0 46.5 46.5 41.5	68 62 55 53 50		dB dB dB dB dB
Return Loss, Active Port	RFX	450 - 4000 MHz		16		dB
Return Loss, Terminated Port	RFX	450 - 4000 MHz		15		dB
Input 1 dB compression[1], P1dB	RFX - RFC	All Bands,100% duty cycle		35		dBm
Input IP2	RFX - RFC	All Bands, 100% duty cycle		95		dBm
Input IP3	RFX - RFC	All Bands, 100% duty cycle		58		dBm
Switching Time, T_{SW}	"On" "Off"	50% Control to 90% RF 50% Control to 10% RF		200 200	500 500	ns ns

Notes: 1. Please refer to Maximum Operating Power in Table 2

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
V_{DD} Supply Voltage	V_{DD}	2.7	3.0	3.3	V
Vss_{EXT} Negative Power Supply Voltage[2]	Vss_{EXT}	-3.3	-3.0	-2.7	V
I_{DD} Power Supply Current V_{DD} = 3.0 V, P_{IN}= 0 dBm	I_{DD}		14		µA
I_{DD} Max Power Supply Current V_{DD} = 3.3 V, P_{MAX}= 33 dBm, Temperature = -40°C	I_{DD} (max)			50	µA
Control Voltage High	V_{IH}	0.7 x V_{DD}		V_{DD}	V
Control Voltage Low	V_{IL}	0		0.3 x V_{DD}	V
I_{CTRL} Control Current[3]	I_{CTRL}			1	µA
Maximum Operating Power (RFX-RFC, All Bands (50Ω), 100% duty cycle)	P_{MAX}			33	dBm
Maximum power into termination (RFX, All Bands (50Ω),100% duty cycle)	P_{MAX}			24	dBm
Operating temperature range	T_{OP}	-40		+85	°C

Note: 2. Applied only when external Vss power supply used. Pin 20 must be grounded when using internal Vss supply.
3. Pull-down resistor in EVK schematic may increase control current.

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Figure 3. Pin Configuration (Top View)

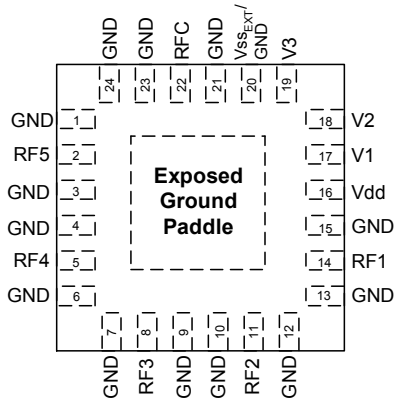


Table 3. Pin Descriptions

Pin #	Name	Description
1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24	GND	Ground
2	RF5[4]	RF I/O
5	RF4[4]	RF I/O
8	RF3[4]	RF I/O
11	RF2[4]	RF I/O
14	RF1[4]	RF I/O
16	V_{DD}	Supply
17	V1	Switch control input, CMOS logic level
18	V2	Switch control input, CMOS logic level
19	V3	Switch control input, CMOS logic level
20	Vss_{EXT} / GND[5]	External Vss Control / Ground
22	RFC[4]	RF Common
Paddle	GND	Ground for proper device operation

Note: 4. Blocking capacitors needed only when non-zero DC voltage present.
5. Pin 20 must be grounded when using internal Vss supply

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
T_{ST}	Storage temperature range	-60	+150	℃
P_{MAX}	Maximum Operating Power (RFX-RFC, All Bands (50Ω), 100% duty cycle)		33	dBm
P_{MAX}	Maximum power into termination (RFX, All Bands (50Ω),100% duty cycle)		24	dBm
V_{ESD}	ESD Voltage HBM[6], All Pins		3500	V
V_{ESD}	ESD Voltage MM[7], All Pins		150	V

Notes: 6. Human Body Model ESD Voltage (HBM, MIL_STD 883 Method 3015.7)
7. Machine Model ESD Voltage (JESD22-A115-A)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42451 in the 24-lead 4x4 QFN package is MSL1.

Optional External Vss Control (Vss_{EXT})

For proper operation, the Vss_{EXT} control must be grounded or at the Vss voltage specified in the Operating Ranges table (*Table 2*). When the Vss_{EXT} control pin on the package is grounded the switch FET's are biased with an internal low spur negative voltage generator. For applications that require the lowest possible spur performance, Vss_{EXT} can be applied to bypass the internal negative voltage generator to eliminate the spurs.

Switching Frequency

The PE42451 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 20=GND). The rate at which the PE42451 can be switched is only limited to the switching time if an external -3 V supply is provided (pin 20=Vss_{EXT}).

Table 5. Truth Table

Mode	V3	V2	V1
All off	0	0	0
RF1 on	0	0	1
RF2 on	0	1	0
RF3 on	0	1	1
RF4 on	1	0	0
RF5 on	1	0	1
All off	1	1	0
Unsupported	1	1	1

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Evaluation Kit

The SP5T switch EK Board was designed to ease customer evaluation of Peregrine's PE42451. The RF common port is connected through a 50 Ω transmission line via the top SMA connector. RF1, RF2, RF3 and RF4 are connected through 50 Ω transmission lines via side SMA connectors. A through 50 Ω transmission is available via SMA connectors RFCAL1 and RFCAL2. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The EVK board is constructed with four metal layers on dielectric materials of Rogers 4003C and 4450 with a total thickness of 32 mils. Layer 1 and layer 3 provide ground for the 50 ohm transmission lines. The 50 ohm transmission lines are designed in layer 2 for high isolation purpose and use a stripline waveguide design with a trace width of 9.4 mils and trace metal thickness of 1.8 mils. The board stack up for 50 ohm transmission lines has 8 mil thickness of Rogers 4003C between layer 1 and layer 2, and 10 mil thickness of Rogers 4450 between layer 2 and layer 3. Please consult manufacturer's guidelines for proper board material properties in your application. The PCB should be designed in such a way that RF transmission lines and sensitive DC i/o traces such as Vss_{EXT} are heavily isolated from one another, otherwise the true performance of the PE42451 will not be yielded.

Figure 4. Evaluation Board Layouts
Peregrine Specification 101/0479

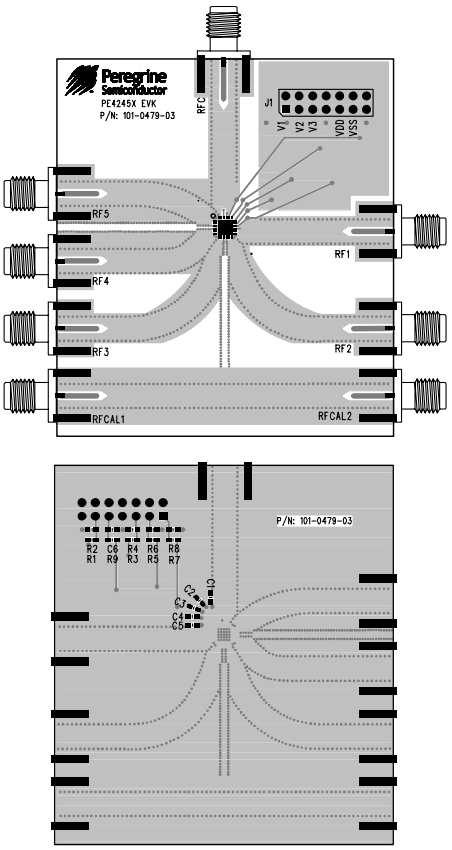
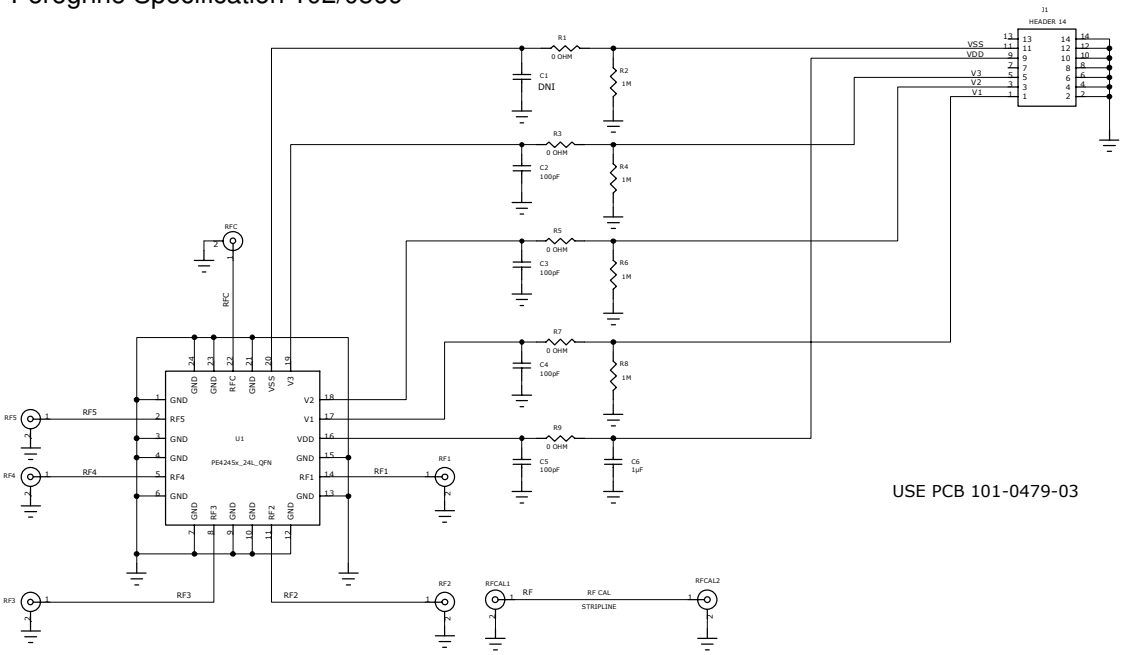


Figure 5. Evaluation Board Schematic
Peregrine Specification 102/0569



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Performance Plots @ 25 °C and 3.0 V unless otherwise specified

Figure 6. Insertion Loss: RFC-RFX @ 25 °C

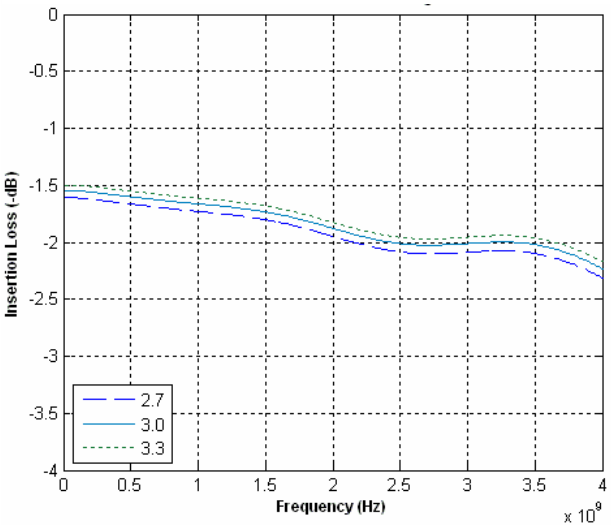


Figure 7. Insertion Loss: RFC-RFX @ 3.0 V

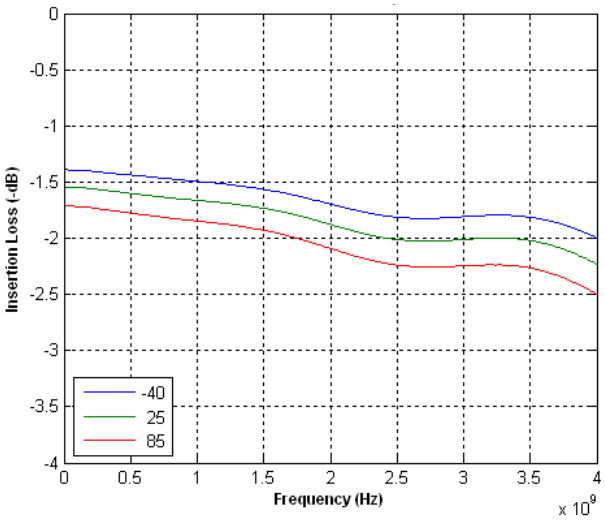
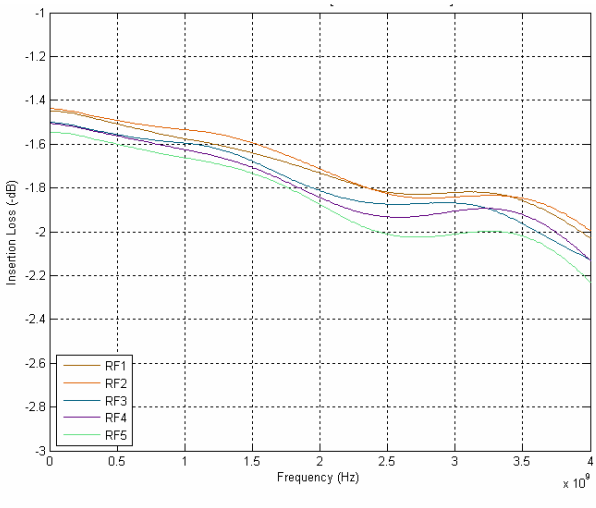


Figure 8. Insertion Loss: All Paths



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Performance Plots @ 25 °C and 3.0 V unless otherwise specified

Figure 9. Isolation: RFC-RFX @ 25 °C

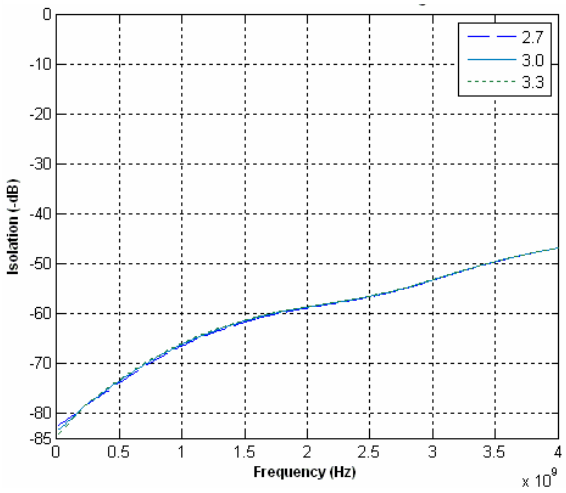


Figure 10. Isolation: RFC-RFX @ 3.0 V

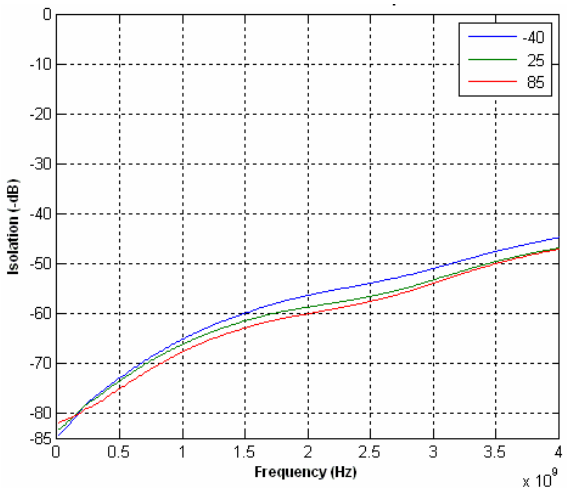


Figure 11. Isolation: RFX-RFX @ 25 °C

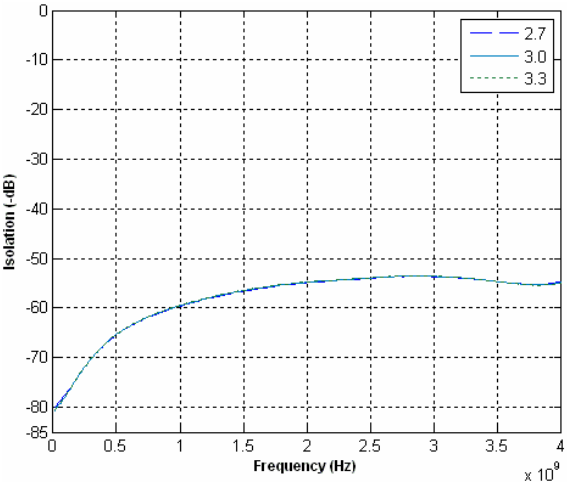
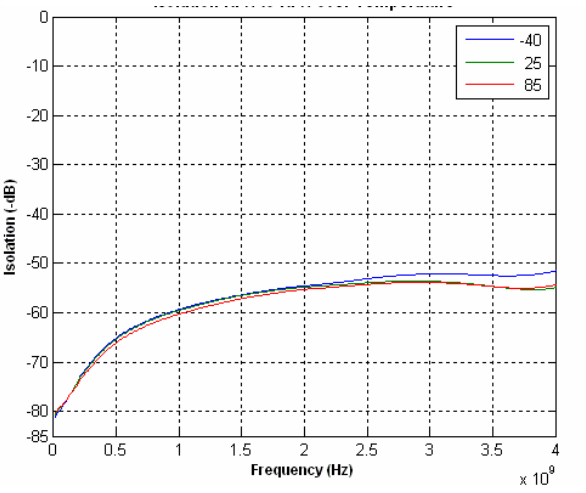


Figure 12. Isolation: RFX-RFX @ 3.0 V



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Performance Plots @ 25 °C and 3.0 V unless otherwise specified (Continued)

Figure 13. Return Loss at active port @ 25 °C

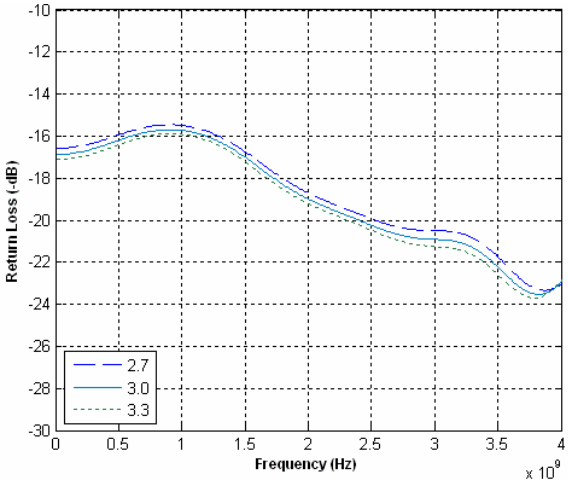


Figure 14. Return Loss at active port @ 3.0 V

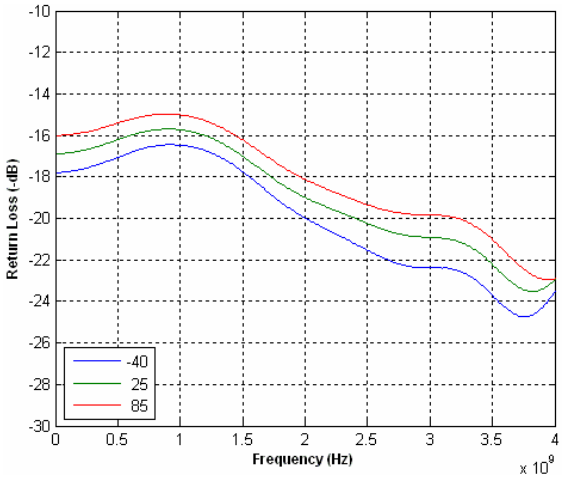


Figure 15. Return Loss: RFC @ 25 °C

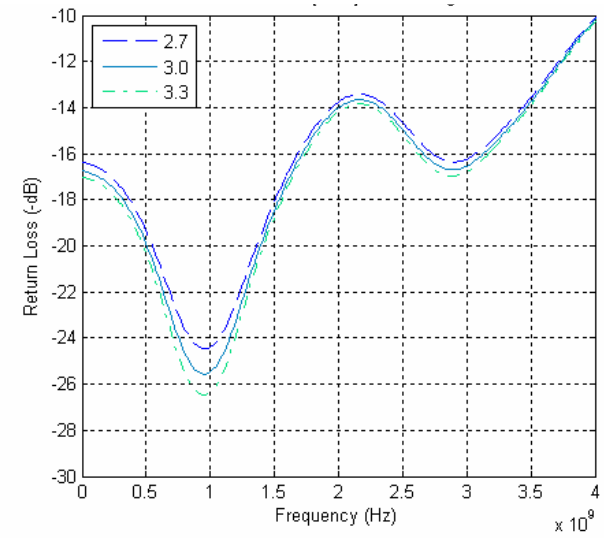


Figure 16. Return Loss: RFC @ 3.0 V

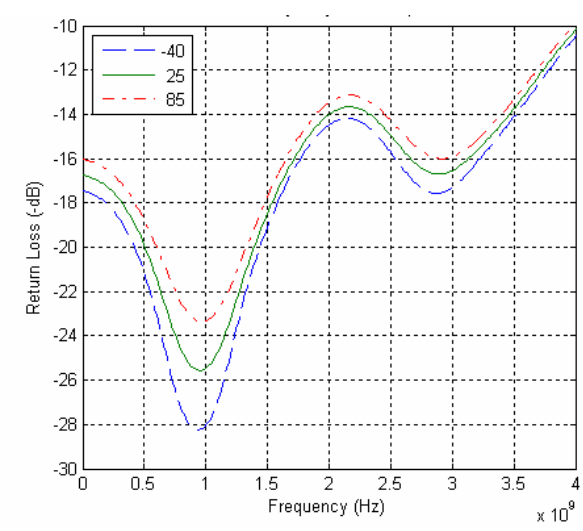
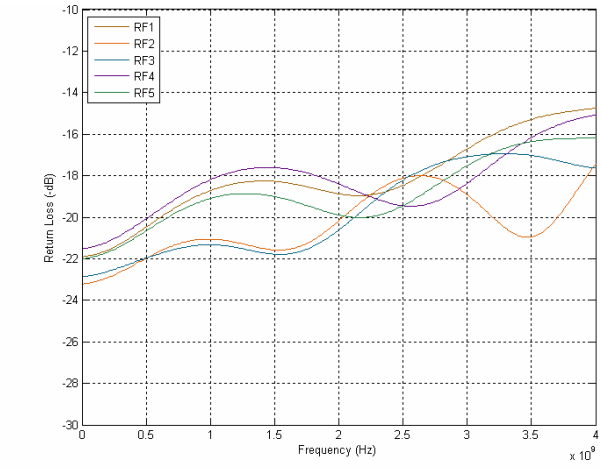


Figure 17. Return Loss: All Paths, Terminated



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Performance Plots @ 25 °C and 3.0 V unless otherwise specified (Continued)

Figure 18. Nominal Linearity Performance (IIP3)

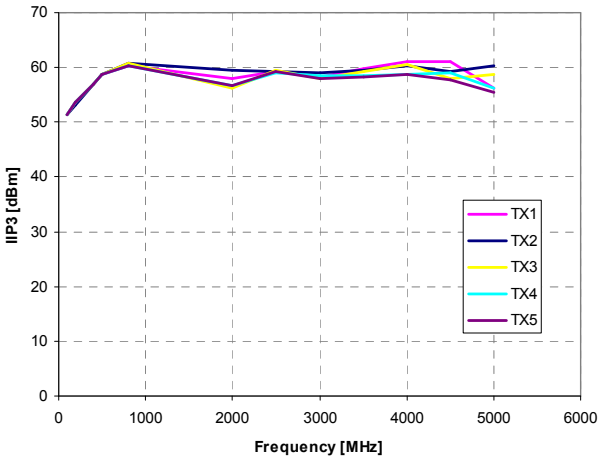
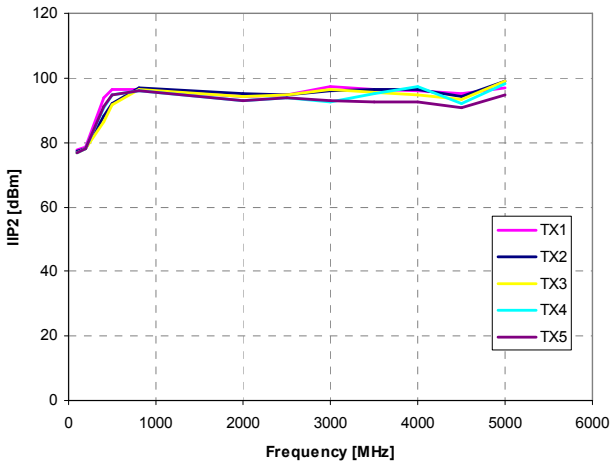


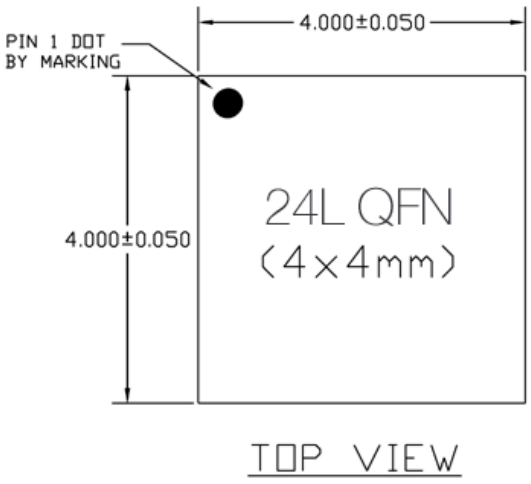
Figure 19. Nominal Linearity Performance (IIP2)

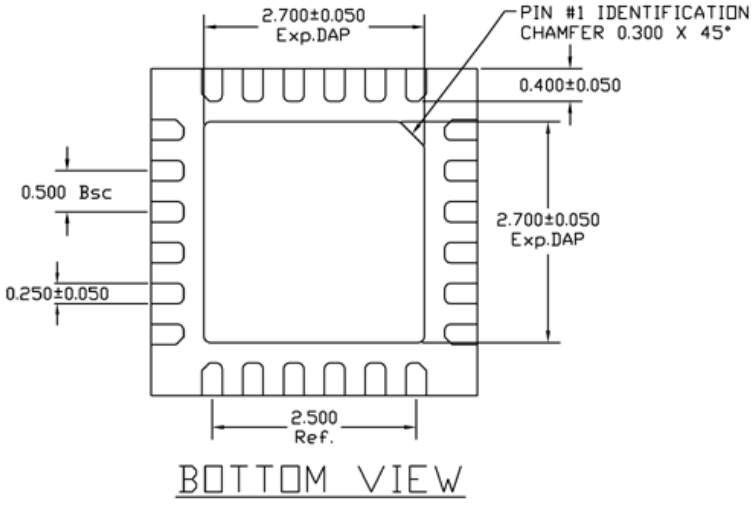


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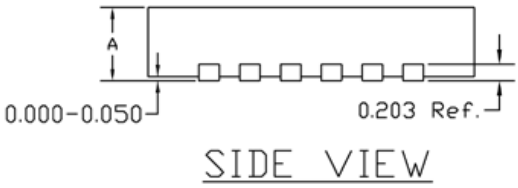
Figure 20. Package Drawing

Peregrine Specification 19/0130





A	Max.	0.900
	Nom.	0.850
	Min.	0.800



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Figure 21. Tape and Reel Drawing

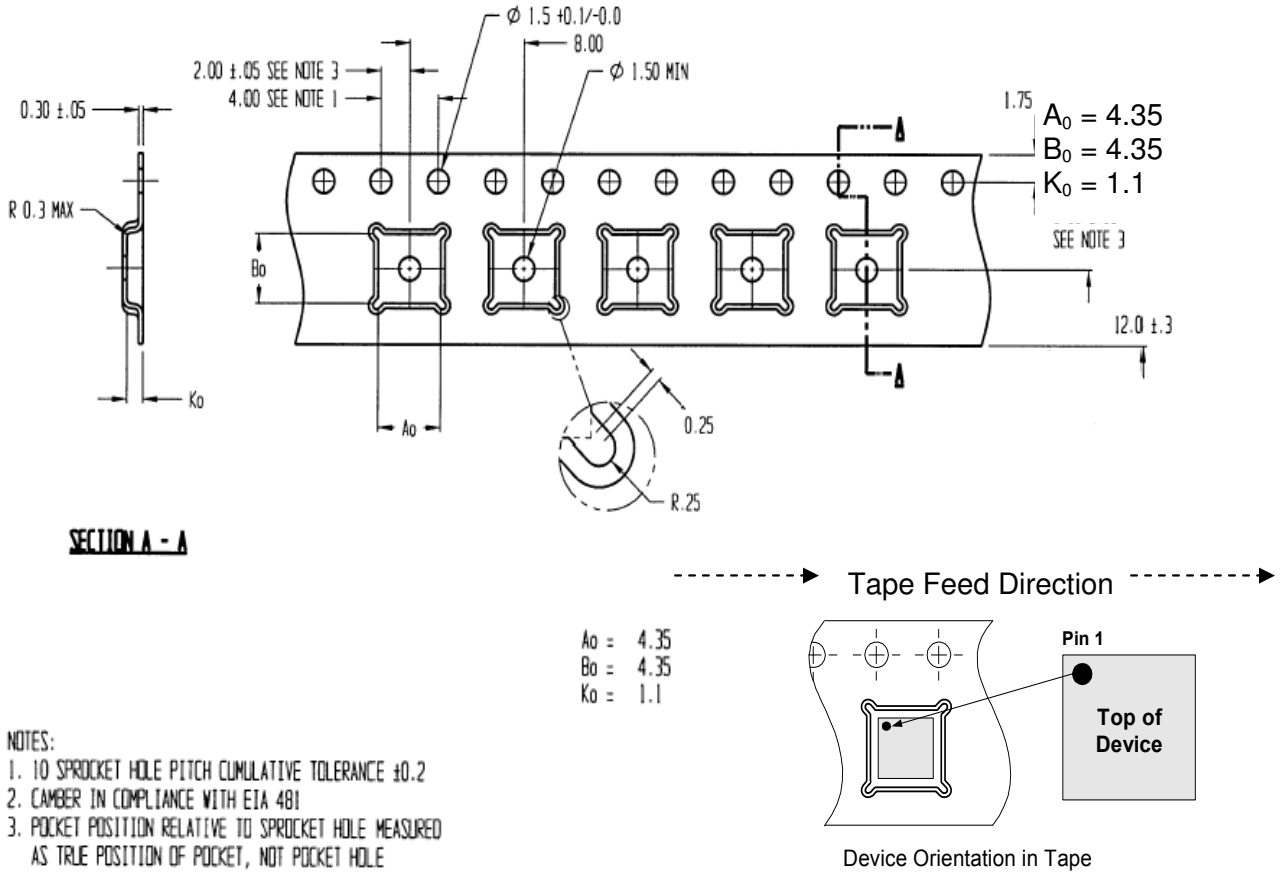
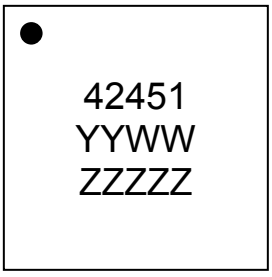


Figure 22. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
PE42451MLIAA	42451	PE42451G-24QFN 4x4mm-cut off tape and reel	Green 24-lead 4x4mm QFN	Bulk or tape cut from reel
PE42451MLIAA-Z	42451	PE42451G-24QFN 4x4mm-3000C	Green 24-lead 4x4mm QFN	3000 units / T&R
EK42451-01	PE42451 -EK	PE42451-24QFN 4x4mm-EK	Evaluation Kit	1 / Box

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Fax: +81-3-3502-5213

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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