To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

2002.04.18 Ver. 6.0

M5M5V416CWG -55HI, -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V416CWG is a family of low voltage 4-Mbit static RAMs organized as 262144-words by 16-bit, fabricated by Mitsubishi's high-performance 0.18µm CMOS technology.

The M5M5V416C is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

M5M5V416CWG is packaged in a CSP (chip scale package), with the outline of 7.0mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

FEATURES

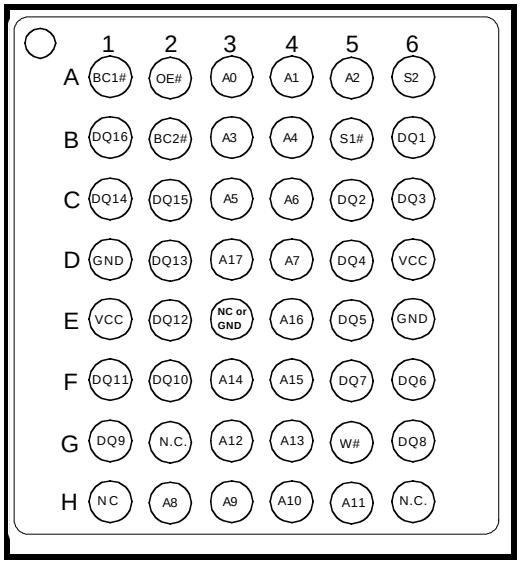
- Single 2.7~3.6V power supply
- Small stand-by current: 0.2µA (3.00V, typ.)
- No clocks, No refresh
- Data retention supply voltage =2.0V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S1#, S2, BC1# and BC2#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Process technology: 0.18µm CMOS
- Package: 48ball 7.0mm x 8.5mm CSP

Version, Operating temperature	Part name	Power Supply	Access time max.	Stand-by current (µA) * Typical(3.0V) 25°C	40°C	Ratings (max. @3.6V) Voltage	25°C	40°C	70°C	85°C	Active current Icc1 (3.0V, typ.)
I-version -40 ~ +85°C	M5M5V416CWG -55HI	2.7 ~ 3.6V	55ns	0.2	0.4	3.0V	1.0	2.0	10	20	30mA (10MHz) 5mA (1MHz)
						3.3V	1.5	2.5	10	20	
	M5M5V416CWG -70HI		70ns			3.6V	2.5	4.0	10	20	

* Typical parameter indicates the value for the center of distribution, and not 100% tested.

PIN CONFIGURATION

(TOP VIEW)



Pin	Function
A0 ~ A17	Address input
DQ1 ~ DQ16	Data input / output
S1#	Chip select input 1
S2	Chip select input 2
W#	Write control input
OE#	Output enable input
BC1#	Lower Byte (DQ1 ~ 8)
BC2#	Upper Byte (DQ9 ~ 16)
Vcc	Power supply
GND	Ground supply

Outline: 48FJA
NC: No Connection
*Don't connect E3 ball to voltage level more than 0V.

M5M5V416CWG -55HI, -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

FUNCTION

The M5M5V416CWG is organized as 262144-words by 16-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs BC1# , BC2# , S1#, S2 , W# and OE#. Each mode is summarized in the function table.

A write operation is executed whenever the low level W# overlaps with the low level BC1# and/or BC2# and the low level S1# and the high level S2. The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting W# at a high level and OE# at a low level while BC1# and/or BC2# and S1# and S2 are in an active state(S1#=L,S2=H).

When setting BC1# at the high level and other pins are in an active stage , upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting BC2# at a high level and other pins are in an active stage, lower-byte are in a selectable mode and upper-byte are in a non-selectable mode.

When setting BC1# and BC2# at a high level or S1# at a high level or S2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by BC1#, BC2# and S1#, S2.

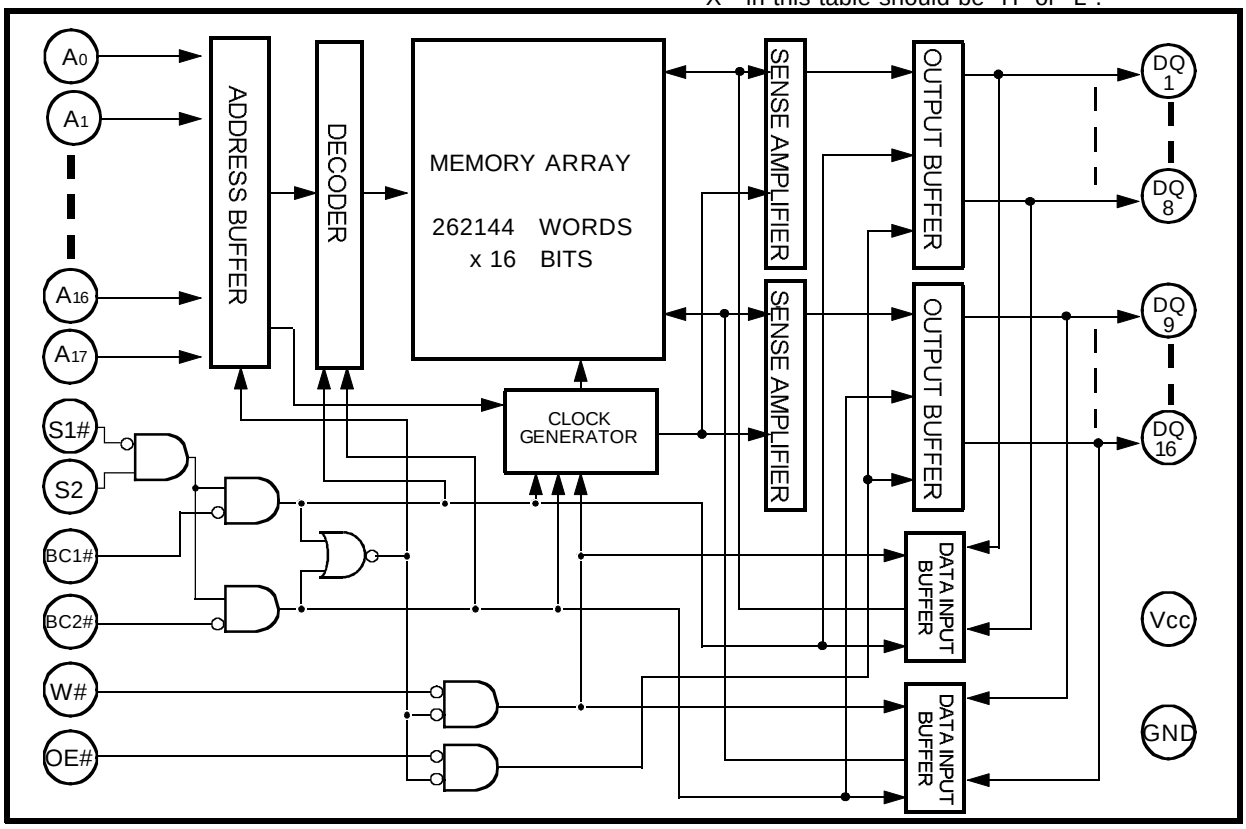
The power supply current is reduced as low as 0.2µA(25°C, typical), and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

S1#	S2	BC1#	BC2#	W#	OE#	Mode	DQ1~8	DQ9~16	Icc
X	L	X	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	X	X	X	X	Non selection	High-Z	High-Z	Standby
X	X	H	H	X	X	Non selection	High-Z	High-Z	Standby
L	H	L	H	L	X	Write	Din	High-Z	Active
L	H	L	H	H	L	Read	Dout	High-Z	Active
L	H	L	H	H	H	———	High-Z	High-Z	Active
L	H	H	L	L	X	Write	High-Z	Din	Active
L	H	H	L	H	L	Read	High-Z	Dout	Active
L	H	H	L	H	H	———	High-Z	High-Z	Active
L	H	L	L	L	X	Write	Din	Din	Active
L	H	L	L	H	L	Read	Dout	Dout	Active
L	H	L	L	H	H	———	High-Z	High-Z	Active

(note) "H" and "L" in this table mean V_{IH} and V_{IL}, respectively. "X" in this table should be "H" or "L".

BLOCK DIAGRAM



M5M5V416CWG -55HI, -70HI

4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V_I	Input voltage	With respect to GND	-0.3* ~ Vcc + 0.3	
V_O	Output voltage	With respect to GND	0 ~ Vcc	
P_d	Power dissipation	Ta=25°C	700	mW
T_a	Operating temperature	I-version	- 40 ~ +85	°C
T_{stg}	Storage temperature		- 65 ~ +150	°C

* -3.0V in case of AC (Pulse width ≦ 30ns)

DC ELECTRICAL CHARACTERISTICS

(Vcc=2.7 ~ 3.6V, unless noted.)

Symbol	Parameter	Conditions			Limits Min	Limits Typ	Limits Max	Units
V_{IH}	High-level input voltage				2.2		Vcc+0.2V	V
V_{IL}	Low-level input voltage				-0.2 *		0.4	
V_{OH}	High-level output voltage	I_{OH}= -0.5mA			2.4			
V_{OL}	Low-level output voltage	I_{OL}=2mA					0.4	
I_I	Input leakage current	V_I=0 ~ Vcc					±1	µA
I_O	Output leakage current	BC1# and BC2#=VIH or S1#=VIH or S2=VIL or OE#=VIH, VI/O=0 ~ Vcc					±1	
Icc1	Active supply current (AC,MOS level)	BC1# and BC2# ≦ 0.2V, S1# ≦ 0.2V, S2 ≧ Vcc-0.2V other inputs ≦ 0.2V or ≧ Vcc-0.2V Output - open (duty 100%)	f= 10MHz		-	30	50	mA
			f= 1MHz		-	5	10	
Icc2	Active supply current (AC,TTL level)	BC1# and BC2# =VIL , S1# =VIL ,S2=VIH other pins =VIH or VIL Output - open (duty 100%)	f= 10MHz		-	30	50	
			f= 1MHz		-	5	10	
Icc3	Stand by supply current (MOS level)	(1) S1# ≧ Vcc - 0.2V, S2 ≧ Vcc - 0.2V, other inputs = 0 ~ Vcc (2) S2 ≦ 0.2V, other inputs = 0 ~ Vcc (3) BC1# and BC2# ≧ Vcc - 0.2V, S1# ≦ 0.2V, S2 ≧ Vcc - 0.2V, other inputs = 0 ~ Vcc	~ +25°C	3.0V	-	0.2	1.0	µA
				3.3V			1.5	
				3.6V			2.5	
			~ +40°C	3.0V	-	0.4	2.0	
				3.3V			2.5	
				3.6V			4.0	
			~ +70°C	3.0V~3.6V	-	-	10	
			~ +85°C	3.0V~3.6V	-	-	20	
Icc4	Stand by supply current (TTL level)	BC1# and BC2# =VIH or S1# =VIH or S2=VIL Other inputs= 0 ~ Vcc			-	-	0.5	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

* -1.0V in case of AC (Pulse width ≦ 30ns)

Note 2: Typical parameter indicates the value for the center of distribution at 3.00V, and is not 100% tested.

CAPACITANCE

(Vcc=2.7 ~ 3.6V, unless noted.)

Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Units
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			10	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f=1MHz			10	

AC ELECTRICAL CHARACTERISTICS (Vcc=2.7 ~ 3.6V, unless noted.)

(1) TEST CONDITIONS

Supply voltage	2.7~3.6V
Input pulse	V_{IH}=2.4V, V_{IL}=0.2V
Input rise time and fall time	5ns
Reference level	V_{OH}=V_{OL}=1.50V Transition is measured ±200mV from steady state voltage.(for ten,tdis)
Output loads	Fig.1,CL=30pF CL=5pF (for ten,tdis)

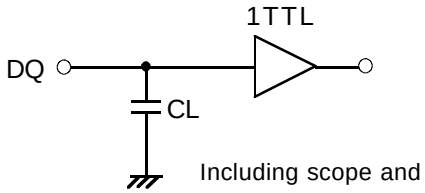


Fig.1 Output load

(2) READ CYCLE

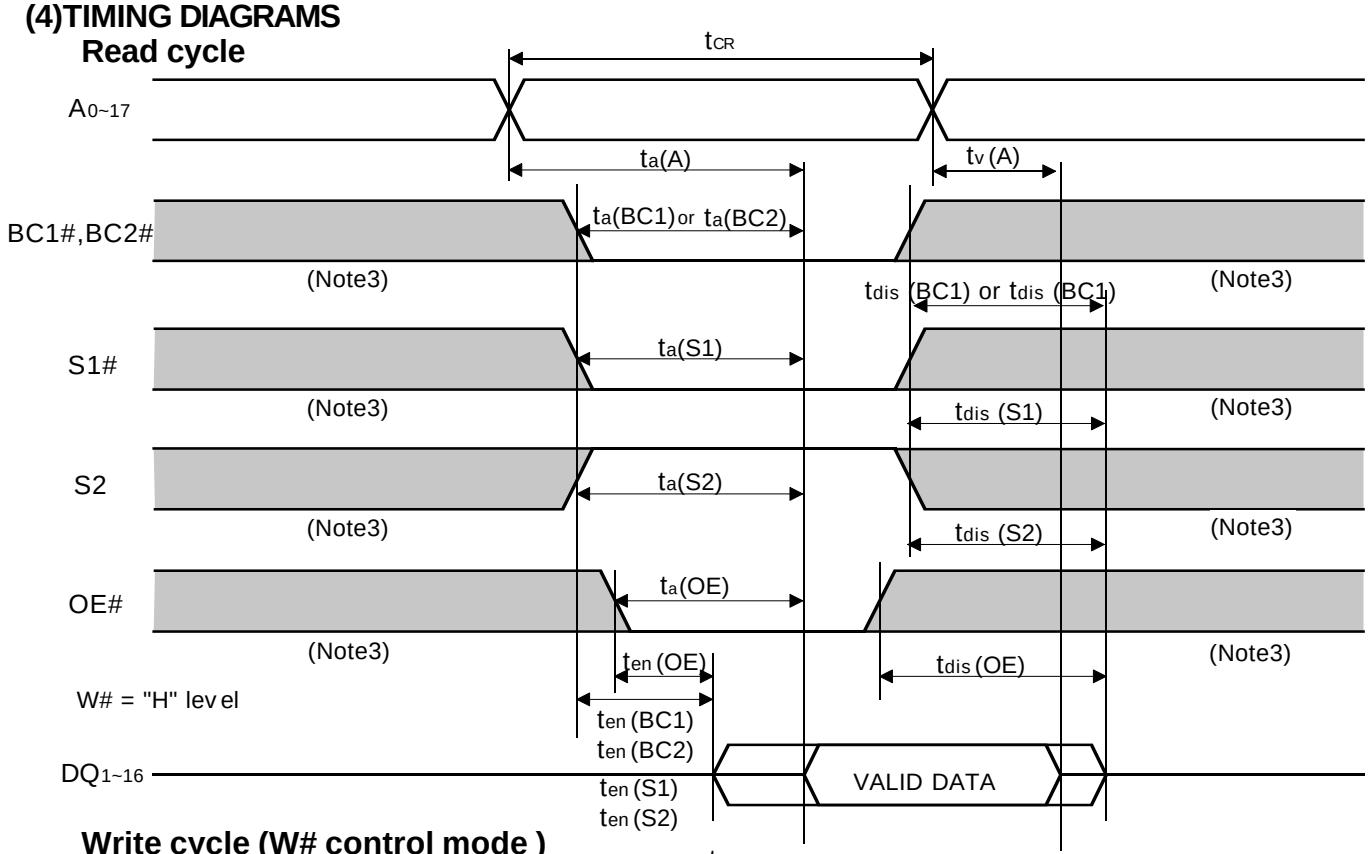
Symbol	Parameter	Limits 55HI		Limits 70HI		Units
		Min	Max	Min	Max	
t_{CR}	Read cycle time	55		70		ns
t_a(A)	Address access time		55		70	ns
t_a(S1)	Chip select 1 access time		55		70	ns
t_a(S2)	Chip select 2 access time		55		70	ns
t_a(BC1)	Byte control 1 access time		55		70	ns
t_a(BC2)	Byte control 2 access time		55		70	ns
t_a(OE)	Output enable access time		30		35	ns
t_{dis}(S1)	Output disable time after S1# high		20		25	ns
t_{dis}(S2)	Output disable time after S2 low		20		25	ns
t_{dis}(BC1)	Output disable time after BC1# high		20		25	ns
t_{dis}(BC2)	Output disable time after BC2# high		20		25	ns
t_{dis}(OE)	Output disable time after OE# high		20		25	ns
t_{en}(S1)	Output enable time after S1# low	10		10		ns
t_{en}(S2)	Output enable time after S2 high	10		10		ns
t_{en}(BC1)	Output enable time after BC1# low	5		5		ns
t_{en}(BC2)	Output enable time after BC2# low	5		5		ns
t_{en}(OE)	Output enable time after OE# low	5		5		ns
t_v(A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

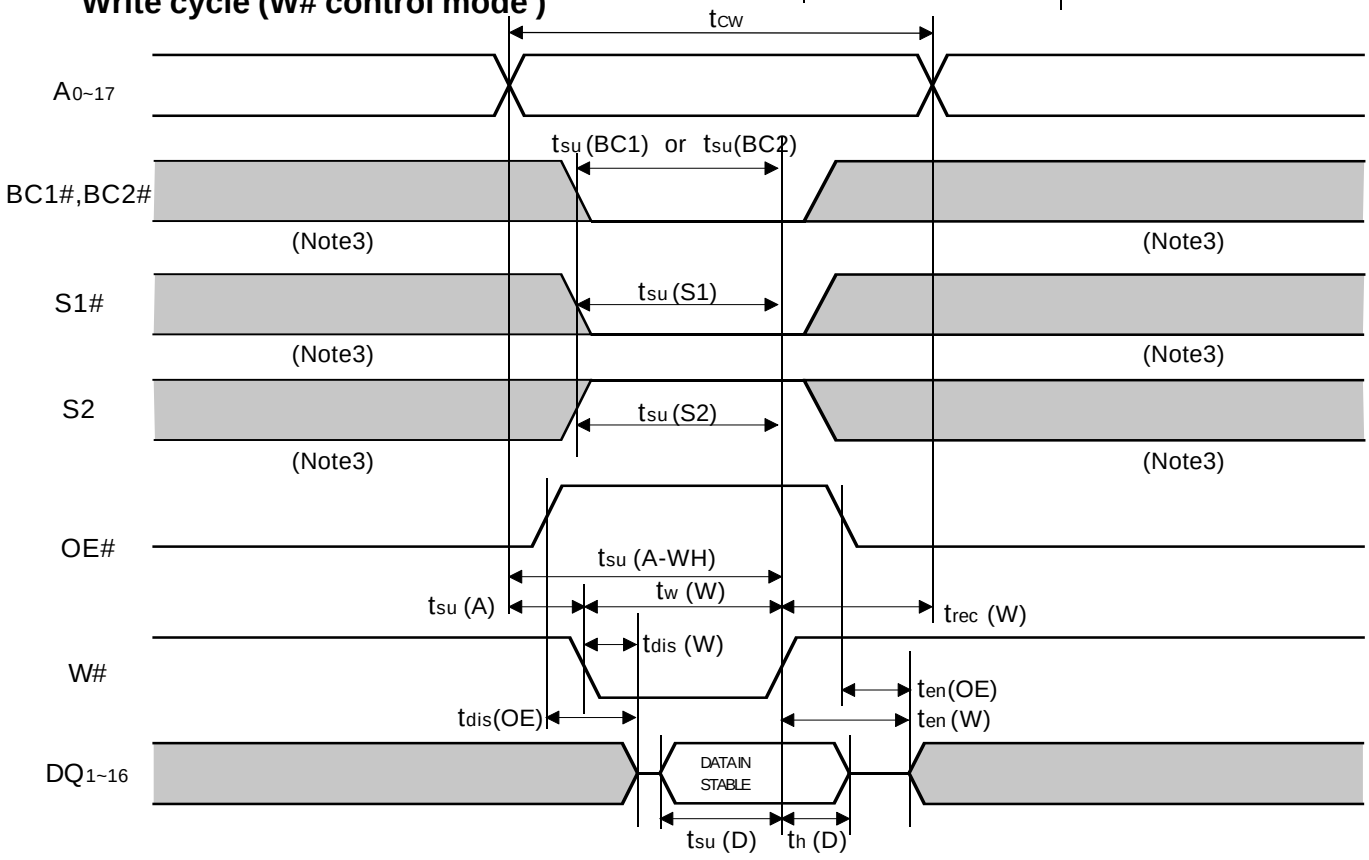
Symbol	Parameter	Limits 55HI		Limits 70HI		Units
		Min	Max	Min	Max	
t_{CW}	Write cycle time	55		70		ns
t_w(W)	Write pulse width	45		55		ns
t_{su}(A)	Address setup time	0		0		ns
t_{su}(A-WH)	Address setup time with respect to W#	50		60		ns
t_{su}(BC1)	Byte control 1 setup time	50		60		ns
t_{su}(BC2)	Byte control 2 setup time	50		60		ns
t_{su}(S1)	Chip select 1 setup time	50		60		ns
t_{su}(S2)	Chip select 2 setup time	50		60		ns
t_{su}(D)	Data setup time	30		35		ns
t_h(D)	Data hold time	0		0		ns
t_{rec}(W)	Write recovery time	0		0		ns
t_{dis}(W)	Output disable time from W# low		20		25	ns
t_{dis}(OE)	Output disable time from OE# high		20		25	ns
t_{en}(W)	Output enable time from W# high	5		5		ns
t_{en}(OE)	Output enable time from OE# low	5		5		ns

(4)TIMING DIAGRAMS

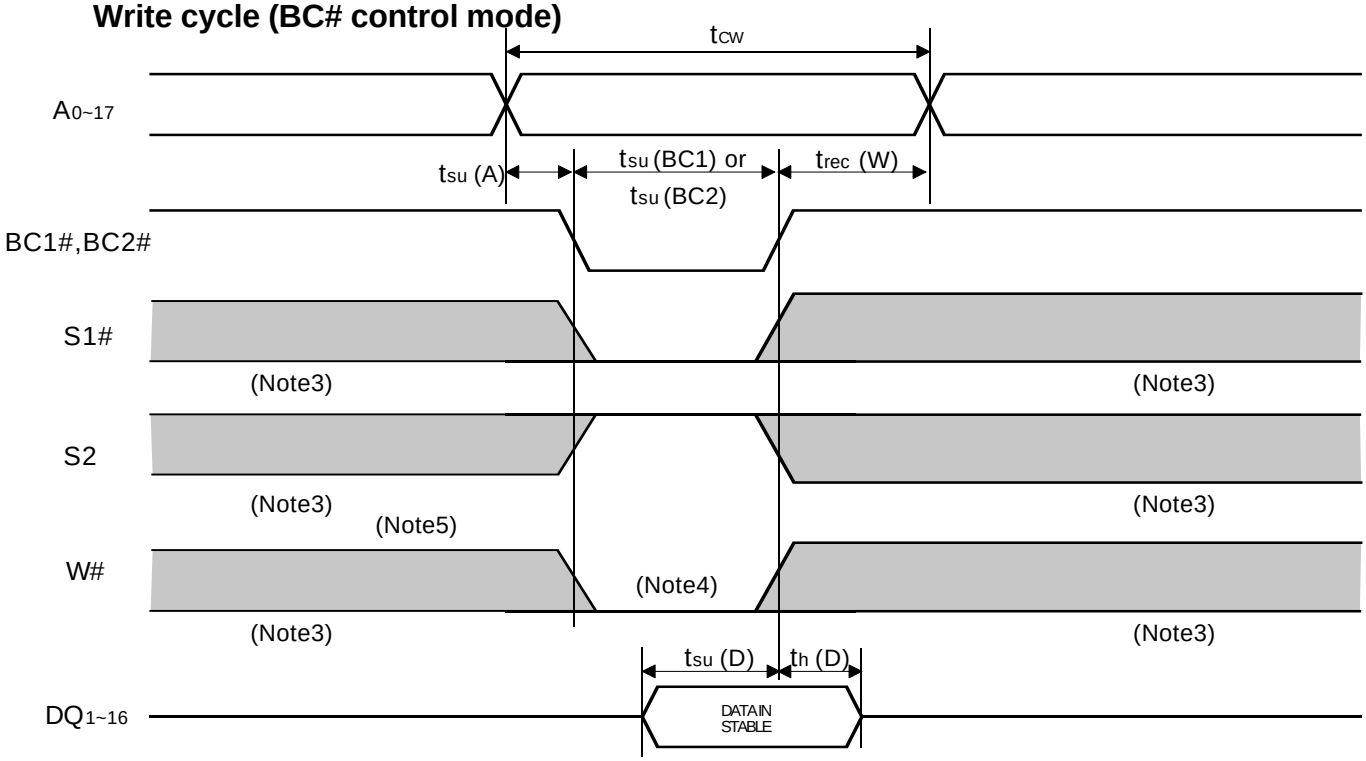
Read cycle



Write cycle (W# control mode)



Write cycle (BC# control mode)



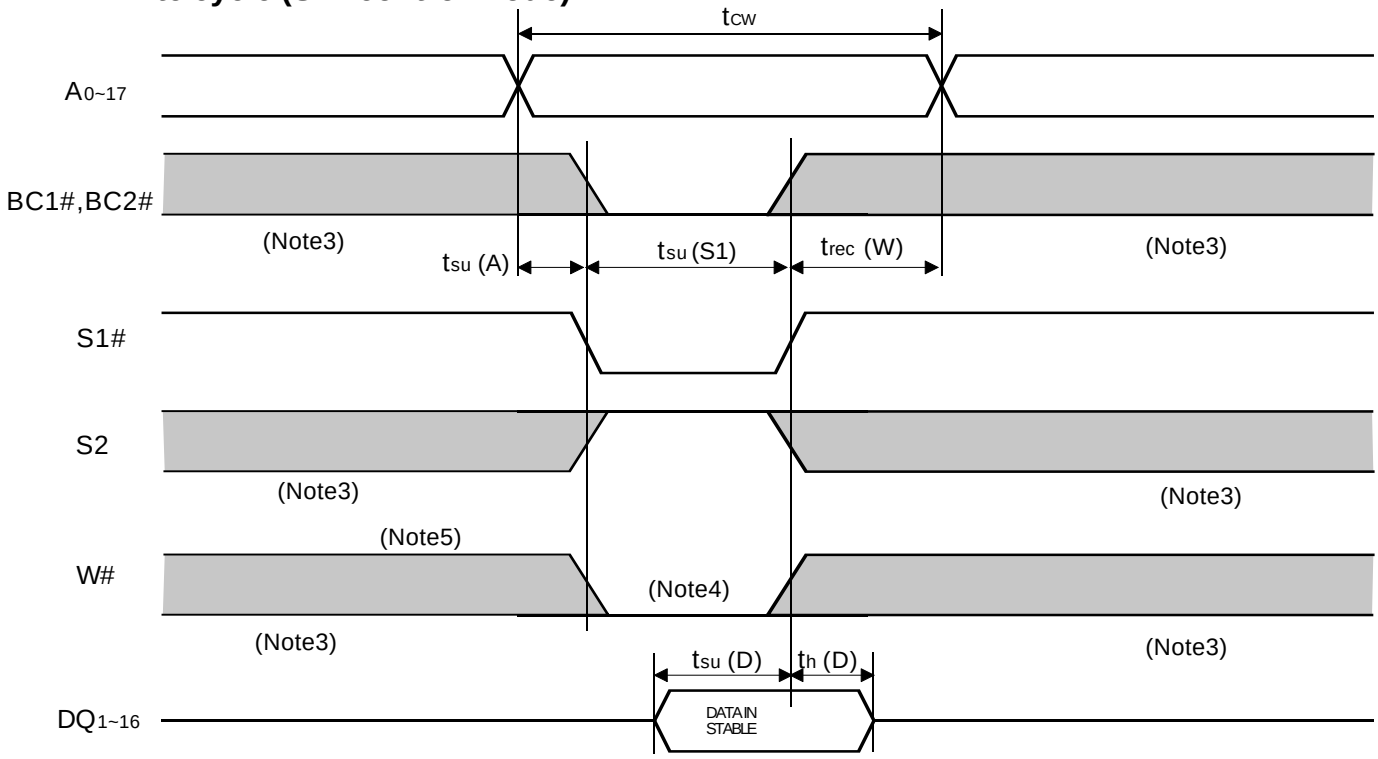
Note 3: Hatching indicates the state is "don't care".

Note 4: A Write occurs during S1# low, S2 high overlaps BC1# and/or BC2# low and W# low.

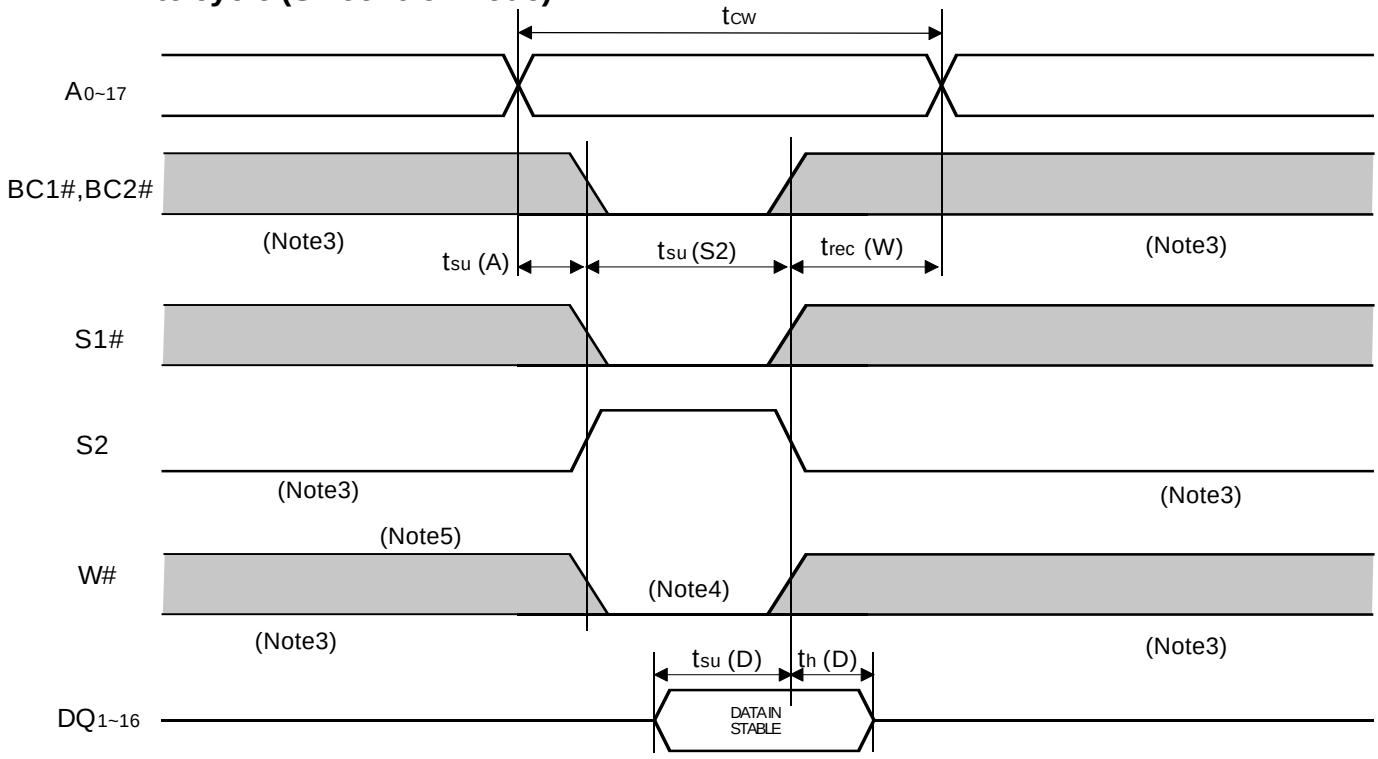
Note 5: When the falling edge of W# is simultaneously or prior to the falling edge of BC1# and/or BC2# or the falling edge of S1# or rising edge of S2, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.

Write cycle (S1# control mode)



Write cycle (S2 control mode)



POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Units
V_{CC} (PD)	Power down supply voltage			2.0			V
V_I (BC)	Byte control input BC1# & BC2#	2.2V ≤ Vcc(PD)		2.2			V
		2.0V ≤ Vcc(PD) ≤ 2.2V			Vcc(PD)		
V_I (S1)	Chip select input S1#	2.2V ≤ Vcc(PD)		2.2			V
		2.0V ≤ Vcc(PD) ≤ 2.2V			Vcc(PD)		
V_I (S2)	Chip select input S2					0.2	V
I_{CC} (PD)	Power down supply current	Vcc=2.0V (1) S1# ≥ Vcc-0.2V, other inputs = 0~Vcc (2) S2 ≤ 0.2V, other inputs = 0~Vcc (3) BC1# and BC2# ≥ Vcc-0.2V S1# ≤ 0.2V, S2 ≥ Vcc-0.2V other inputs = 0~Vcc	~ +25°C	-	0.05	0.8	µA
			~ +40°C	-	0.1	1.5	
			~ +70°C	-	-	7.5	
			~ +85°C	-	-	15	

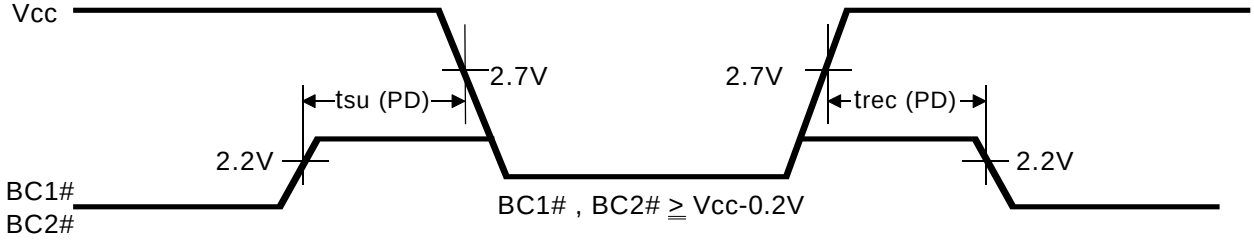
Note 7: Typical parameter of Icc(PD) indicates the value for the center of distribution at 2.0V, and not 100% tested.

(2) TIMING REQUIREMENTS

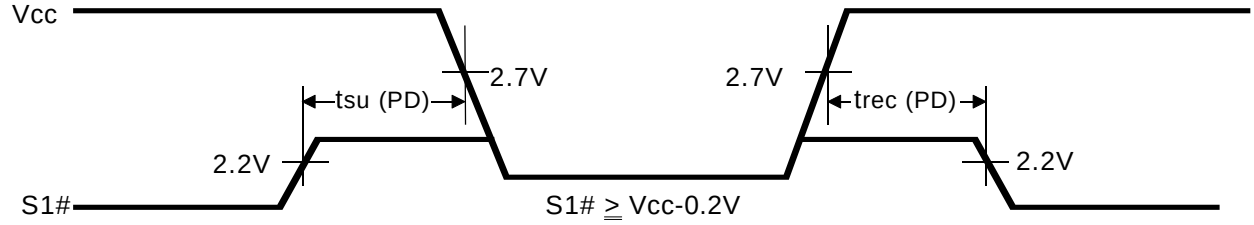
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Units
t_{su} (PD)	Power down set up time		0			ns
t_{rec} (PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

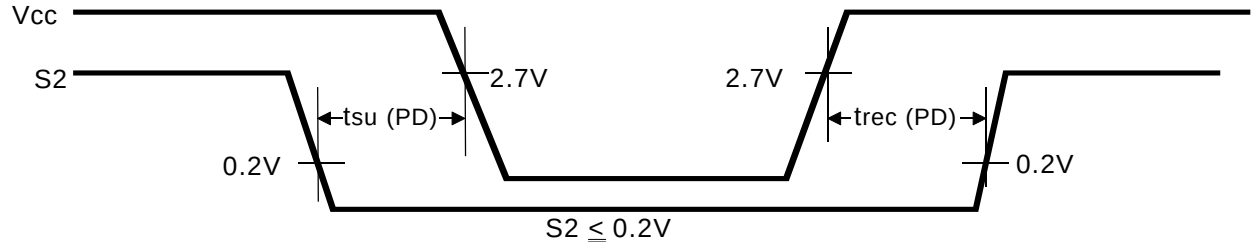
BC# control mode On the BC# control mode, the level of S1# and S2 must be fixed at S1# , S2 ≥ Vcc-0.2V or S2 ≤ 0.2V.



S1# control mode On the S1# mode, the level of S2 must be fixed at S2 ≥ Vcc-0.2V or S2 ≤ 0.2V.



S2 control mode



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