# LOW-VOLTAGE MOTOR DRIVER WITH SERIAL INTERFACE

**Check for Samples: DRV8830**

## FEATURES

- **H-Bridge Voltage-Controlled Motor Driver**
  - **Drives DC Motor, One Winding of a Stepper Motor, or Other Actuators/Loads**
  - **Efficient PWM Voltage Control for Constant Motor Speed With Varying Supply Voltages**
  - **Low MOSFET On-Resistance: HS + LS 450 mΩ**
- **1-A Maximum DC/RMS or Peak Drive Current**
- **2.75-V to 6.8-V Operating Supply Voltage Range**
- **300-nA (Typical) Sleep Mode Current**
- **Serial $I^2C$-Compatible Interface**
- **Multiple Address Selections Allow Up to 9 Devices on One $I^2C$ Bus**
- **Current Limit Circuit and Fault Output**
- **Thermally Enhanced Surface Mount Packages**

## APPLICATIONS

- **Battery-Powered:**
  - **Printers**
  - **Toys**
  - **Robotics**
  - **Cameras**
  - **Phones**
- **Small Actuators, Pumps, etc.**

## DESCRIPTION

The DRV8830 provides an integrated motor driver solution for battery-powered toys, printers, and other low-voltage or battery-powered motion control applications. The device has one H-bridge driver, and can drive one DC motor or one winding of a stepper motor, as well as other loads like solenoids. The output driver block consists of N-channel and P-channel power MOSFET's configured as an H-bridge to drive the motor winding.

Provided with sufficient PCB heatsinking, the DRV8830 can supply up to 1-A of DC/RMS or peak output current. It operates on power supply voltages from 2.75 V to 6.8 V.

To maintain constant motor speed over varying battery voltages while maintaining long battery life, a PWM voltage regulation method is provided. The output voltage is programmed via an $I^2C$-compatible interface, using an internal voltage reference and DAC.

Internal protection functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature protection.

The DRV8830 is available in tiny 3-mm x 3-mm 10-pin MSOP and WSON packages with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

**ORDERING INFORMATION(1)**

| PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| PowerPAD™ (MSOP) - DGQ | Reel of 2500 | DRV8830DGQR | 8830 |
| | Tube of 80 | DRV8830DGQ | 8830 |
| PowerPAD™ (WSON) - DRC | Reel of 3000 | DRV8830DRCR | 8830 |
| | Reel of 250 | DRV8830DRCT | 8830 |

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

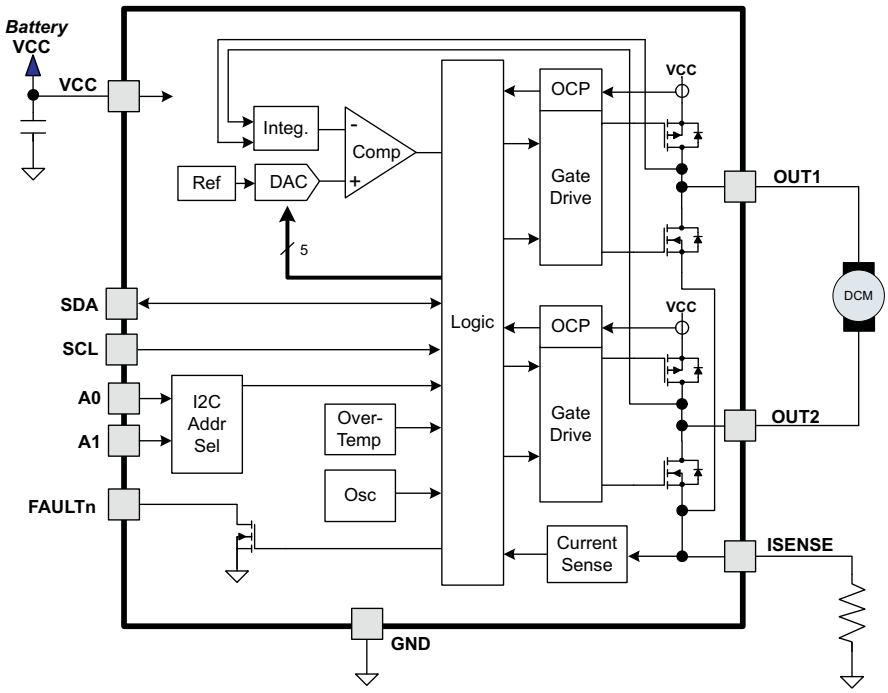
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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# DEVICE INFORMATION

## Functional Block Diagram





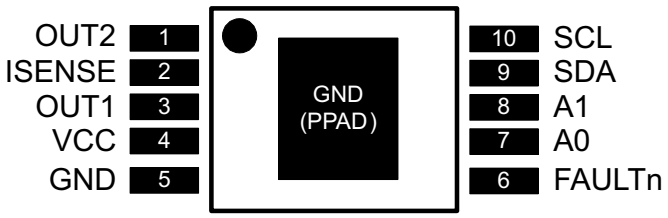
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**Table 1. TERMINAL FUNCTIONS**

| NAME | PIN | I/O(1) | DESCRIPTION | EXTERNAL COMPONENTS OR CONNECTIONS |
|---|---|---|---|---|
| GND | 5 | - | Device ground | |
| VCC | 4 | - | Device and motor supply | Bypass to GND with a 0.1-µF (minimum) ceramic capacitor. |
| SDA | 9 | IO | Serial data | Data line of $I^2C$ serial bus |
| SCL | 10 | I | Serial clock | Clock line of $I^2C$ serial bus |
| A0 | 7 | I | Address set 0 | Connect to GND, VCC, or open to set $I^2C$ base address. See serial interface description. |
| A1 | 8 | I | Address set 1 | |
| FAULTn | 6 | OD | Fault output | Open-drain output driven low if fault condition present |
| OUT1 | 3 | O | Bridge output 1 | Connect to motor winding |
| OUT2 | 1 | O | Bridge output 2 | |
| ISENSE | 2 | IO | Current sense resistor | Connect current sense resistor to GND. Resistor value sets current limit level. |

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

DGQ OR DRC PACKAGE
(TOP VIEW)




## ABSOLUTE MAXIMUM RATINGS(1)(2)

| | | VALUE | UNIT |
|---|---|---|---|
| VCC | Power supply voltage range | –0.3 to 7 | V |
| | Input pin voltage range | –0.5 to 7 | V |
| | Peak motor drive output current(3) | Internally limited | A |
| | Continuous motor drive output current(3) | 1 | A |
| | Continuous total power dissipation | See Dissipation Ratings table | |
| $T_J$ | Operating virtual junction temperature range | –40 to 150 | °C |
| $T_{stg}$ | Storage temperature range | –60 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

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## THERMAL INFORMATION

| THERMAL METRIC(1) | | DRV8830 DGQ 10 PINS | DRV8830 DRC 10 PINS | UNITS |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(2) | 69.3 | 50.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance(3) | 63.5 | 78.4 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance(4) | 51.6 | 18.8 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter(5) | 1.5 | 1.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(6) | 23.2 | 17.9 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance(7) | 9.5 | 5.1 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Motor power supply voltage range | 2.75 | | 6.8 | V |
| $I_{OUT}$ | Continuous or peak H-bridge output current(1) | 0 | | 1 | A |

(1) Power dissipation and thermal limits must be observed.


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## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 2.75 V to 6.8 V, $T_A$ = -40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $I_{VCC}$ | VCC operating supply current | $V_{CC}$ = 5 V | | 1.4 | 2 | mA |
| $I_{VCCQ}$ | VCC sleep mode supply current | $V_{CC}$ = 5 V, $T_A$ = 25°C | | 0.3 | 1 | µA |
| $V_{UVLO}$ | VCC undervoltage lockout voltage | $V_{CC}$ rising | | 2.575 | 2.75 | V |
| | | $V_{CC}$ falling | | 2.47 | | |
| **LOGIC-LEVEL INPUTS** | | | | | | |
| $V_{IL}$ | Input low voltage | | 0.25 x VCC | 0.38 x VCC | | V |
| $V_{IH}$ | Input high voltage | | | 0.46 x VCC | 0.5 x VCC | V |
| $V_{HYS}$ | Input hysteresis | | | 0.08 x VCC | | V |
| $I_{IL}$ | Input low current | $V_{IN}$ = 0 | -10 | | 10 | µA |
| $I_{IH}$ | Input high current | $V_{IN}$ = 3.3 V | | | 50 | µA |
| **LOGIC-LEVEL OUTPUTS (FAULTn)** | | | | | | |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 4 mA, $V_{CC}$ = 5 V | | 0.5 | | V |
| **H-BRIDGE FETS** | | | | | | |
| $R_{DS(ON)}$ | HS FET on resistance | $V_{CC}$ = 5 V, $I_O$ = 0.8 A, $T_J$ = 85°C | | 290 | 400 | mΩ |
| | | $V_{CC}$ = 5 V, $I_O$ = 0.8 A, $T_J$ = 25°C | | 250 | | |
| $R_{DS(ON)}$ | LS FET on resistance | $V_{CC}$ = 5 V, $I_O$ = 0.8 A, $T_J$ = 85°C | | 230 | 320 | mΩ |
| | | $V_{CC}$ = 5 V, $I_O$ = 0.8 A, $T_J$ = 25°C | | 200 | | |
| $I_{OFF}$ | Off-state leakage current | | –20 | | 20 | µA |
| **MOTOR DRIVER** | | | | | | |
| $t_R$ | Rise time | $V_{CC}$ = 3 V, load = 4 Ω | 50 | | 300 | ns |
| $t_F$ | Fall time | $V_{CC}$ = 3 V, load = 4 Ω | 50 | | 300 | ns |
| $f_{SW}$ | Internal PWM frequency | | | 44.5 | | kHz |
| **PROTECTION CIRCUITS** | | | | | | |
| $I_{OCP}$ | Overcurrent protection trip level | | 1.3 | | 3 | A |
| $t_{OCP}$ | OCP deglitch time | | | 2 | | µs |
| $T_{TSD}$ | Thermal shutdown temperature | Die temperature(1) | 150 | 160 | 180 | °C |
| **VOLTAGE CONTROL** | | | | | | |
| $V_{REF}$ | Reference output voltage | | 1.235 | 1.285 | 1.335 | V |
| $\Delta V_{LINE}$ | Line regulation | $V_{CC}$ = 3.3 V to 6 V, $V_{OUT}$ = 3 V,(1) $I_{OUT}$ = 500 mA | | ±1 | | % |
| $\Delta V_{LOAD}$ | Load regulation | $V_{CC}$ = 5 V, $V_{OUT}$ = 3 V, $I_{OUT}$ = 200 mA to 800 mA(1) | | ±1 | | % |
| **CURRENT LIMIT** | | | | | | |
| $V_{ILIM}$ | Current limit sense voltage | | 160 | 200 | 240 | mV |
| $t_{ILIM}$ | Current limit fault deglitch time | | | 275 | | ms |
| $R_{ISEN}$ | Current limit sense resistance (external resistor value) | | 0 | | 1 | Ω |

(1) Not production tested.

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## I²C TIMING REQUIREMENTS(1)

$V_{CC}$ = 2.75 V to 6.8 V, $T_A$ = -40°C to 85°C (unless otherwise noted)

| | | STANDARD MODE | | | FAST MODE | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{scl}$ | I²C clock frequency | 0 | | 100 | 0 | | 400 | kHz |
| $t_{sch}$ | I²C clock high time | 4 | | | 0.6 | | | µs |
| $t_{scl}$ | I²C clock low time | 4.7 | | | 1.3 | | | µs |
| $t_{sp}$ | I²C spike time | 0 | | 50 | 0 | | 50 | ns |
| $t_{sds}$ | I²C serial data setup time | 250 | | | 100 | | | ns |
| $t_{sdh}$ | I²C serial data hold time | 0 | | | 0 | | | ns |
| $t_{icr}$ | I²C input rise time | | | 1000 | 20+0.1Cb(2) | | 300 | ns |
| $t_{icf}$ | I²C input fall time | | | 300 | 20+0.1Cb(2) | | 300 | ns |
| $t_{ocf}$ | I²C output fall time | | | 300 | 20+0.1Cb(2) | | 300 | ns |
| $t_{buf}$ | I²C bus free time | 4.7 | | | 1.3 | | | µs |
| $t_{sts}$ | I²C Start setup time | 4.7 | | | 0.6 | | | µs |
| $t_{sth}$ | I²C Start hold time | 4 | | | 0.6 | | | µs |
| $t_{sps}$ | I²C Stop setup time | 4 | | | 0.6 | | | µs |
| $t_{vd}$ (data) | Valid data time (SCL low to SDA valid) | | | 1 | | | 1 | µs |
| $t_{vd}$ (ack) | Valid data time of ACK (ACK signal from SCL low to SDA low) | | | 1 | | | 1 | µs |

(1) Not production tested.
(2) $C_b$ = total capacitance of one bus line in pF

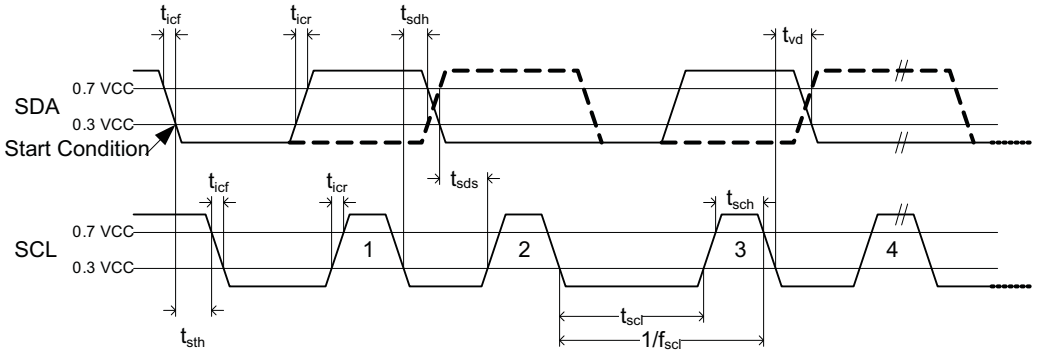



**Figure 1. I²C Timing Requirements**

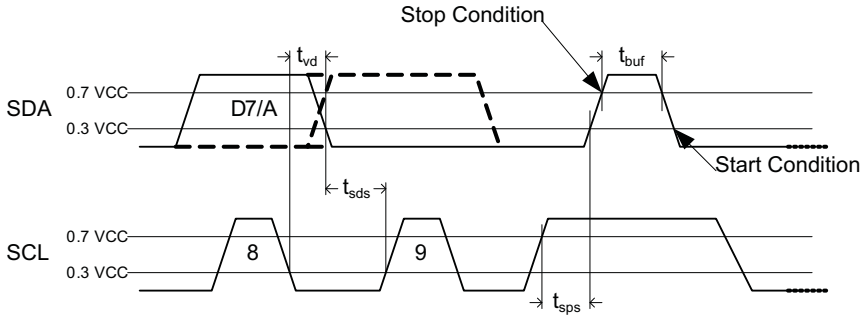



**Figure 2. I²C Timing Requirements**


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## TYPICAL PERFORMANCE GRAPHS

**EFFICIENCY**
**vs**
**LOAD CURRENT**
**($V_{IN}$ = 5 V, $V_{OUT}$ = 3 V)**

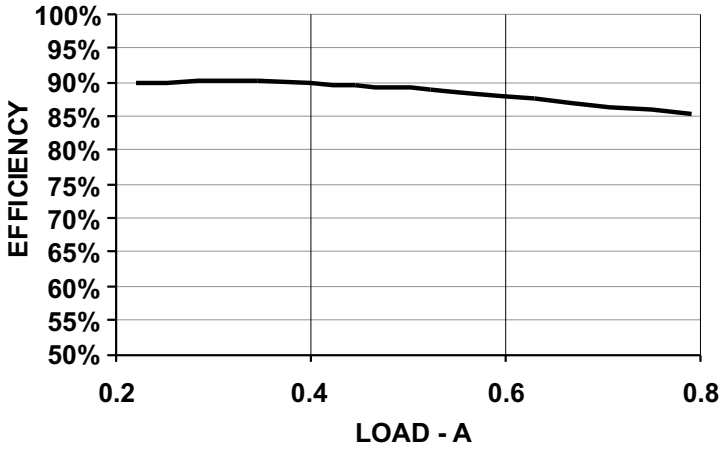



**Figure 3.**

**EFFICIENCY**
**vs**
**OUTPUT VOLTAGE**
**($V_{IN}$ = 5 V, $I_{OUT}$ = 500 mA)**

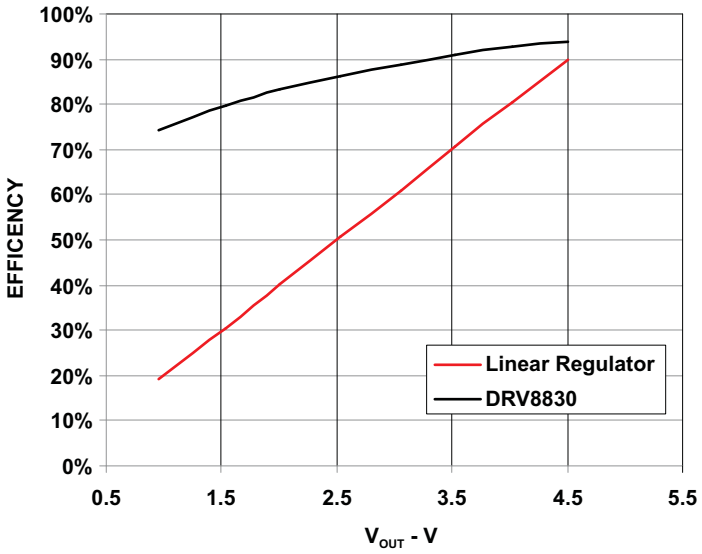



**Figure 4.**

# FUNCTIONAL DESCRIPTION

## PWM Motor Driver

The DRV8830 contains an H-bridge motor driver with PWM voltage-control circuitry with current limit circuitry. A block diagram of the motor control circuitry is shown below.

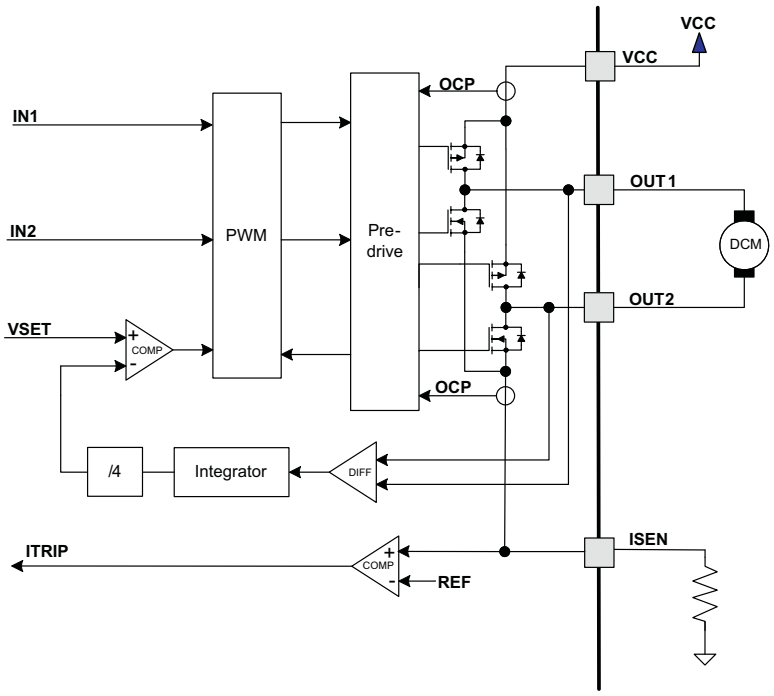



**Figure 5. Motor Control Circuitry**

## Bridge Control

The IN1 and IN2 control bits in the serial interface register enable the H-bridge outputs. The following table shows the logic:

**Table 2. H-Bridge Logic**

| IN1 | IN2 | OUT1 | OUT2 | Function |
|---|---|---|---|---|
| 0 | 0 | Z | Z | Standby/coast |
| 0 | 1 | L | H | Reverse |
| 1 | 0 | H | L | Forward |
| 1 | 1 | H | H | Brake |

When both bits are zero, the output drivers are disabled and the device is placed into a low-power shutdown state. The current limit fault condition (if present) is also cleared.

At initial power-up, the device will enter the low-power shutdown state. Note that when transitioning from either brake or standby mode to forward or reverse, the voltage control PWM starts at zero duty cycle. The duty cycle slowly ramps up to the commanded voltage. This can take up to 12 ms to go from standby to 100% duty cycle.


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## Voltage Regulation

The DRV8830 provides the ability to regulate the voltage applied to the motor winding. This feature allows constant motor speed to be maintained even when operating from a varying supply voltage such as a discharging battery.

The DRV8830 uses a pulse-width modulation (PWM) technique instead of a linear circuit to minimize current consumption and maximize battery life.

The circuit monitors the voltage difference between the output pins and integrates it, to get an average DC voltage value. This voltage is divided by 4 and compared to the output voltage of the VSET DAC, which is set through the serial interface. If the averaged output voltage (divided by 4) is lower than VSET, the duty cycle of the PWM output is increased; if the averaged output voltage (divided by 4) is higher than VSET, the duty cycle is decreased.

During PWM regulation, the H-bridge is enabled to drive current through the motor winding during the PWM on time. This is shown in the diagram below as case 1. The current flow direction shown indicates the state when IN1 is high and IN2 is low.

Note that if the programmed output voltage is greater than the supply voltage, the device will operate at 100% duty cycle and the voltage regulation feature will be disabled. In this mode the device behaves as a conventional H-bridge driver.

During the PWM off time, winding current is re-circulated by enabling both of the high-side FETs in the bridge. This is shown as case 2 below.

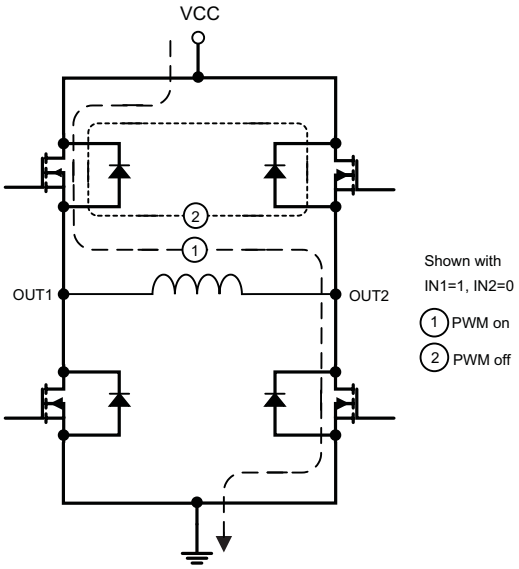



**Figure 6. Voltage Regulation**

## Voltage Setting (VSET DAC)

The DRV8830 includes an internal reference voltage that is connected to a DAC. This DAC generates a voltage which is used to set the PWM regulated output voltage as described above.

The DAC is controlled by the VSET bits from the serial interface. The commanded output voltage is as follows:

| VSET[5..0] | Output Voltage | | VSET[5..0] | Output Voltage |
|---|---|---|---|---|
| 0x00h | Reserved | | 0x20h | 2.57 |
| 0x01h | Reserved | | 0x21h | 2.65 |
| 0x02h | Reserved | | 0x22h | 2.73 |
| 0x03h | Reserved | | 0x23h | 2.81 |
| 0x04h | Reserved | | 0x24h | 2.89 |
| 0x05h | Reserved | | 0x25h | 2.97 |
| 0x06h | 0.48 | | 0x26h | 3.05 |
| 0x07h | 0.56 | | 0x27h | 3.13 |
| 0x08h | 0.64 | | 0x28h | 3.21 |
| 0x09h | 0.72 | | 0x29h | 3.29 |
| 0x0Ah | 0.80 | | 0x2Ah | 3.37 |
| 0x0Bh | 0.88 | | 0x2Bh | 3.45 |
| 0x0Ch | 0.96 | | 0x2Ch | 3.53 |
| 0x0Dh | 1.04 | | 0x2Dh | 3.61 |
| 0x0Eh | 1.12 | | 0x2Eh | 3.69 |
| 0x0Fh | 1.20 | | 0x2Fh | 3.77 |
| 0x10h | 1.29 | | 0x30h | 3.86 |
| 0x11h | 1.37 | | 0x31h | 3.94 |
| 0x12h | 1.45 | | 0x32h | 4.02 |
| 0x13h | 1.53 | | 0x33h | 4.10 |
| 0x14h | 1.61 | | 0x34h | 4.18 |
| 0x15h | 1.69 | | 0x35h | 4.26 |
| 0x16h | 1.77 | | 0x36h | 4.34 |
| 0x17h | 1.85 | | 0x37h | 4.42 |
| 0x18h | 1.93 | | 0x38h | 4.50 |
| 0x19h | 2.01 | | 0x39h | 4.58 |
| 0x1Ah | 2.09 | | 0x3Ah | 4.66 |
| 0x1Bh | 2.17 | | 0x3Bh | 4.74 |
| 0x1Ch | 2.25 | | 0x3Ch | 4.82 |
| 0x1Dh | 2.33 | | 0x3Dh | 4.90 |
| 0x1Eh | 2.41 | | 0x3Eh | 4.98 |
| 0x1Fh | 2.49 | | 0x3Fh | 5.06 |

The voltage can be calculated as 4 x VREF x (VSET +1) / 64, where VREF is the internal 1.285-V reference.


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## Current Limit

A current limit circuit is provided to protect the system in the event of an overcurrent condition, such as what would be encountered if driving a DC motor at start-up or with an abnormal mechanical load (stall condition).

The motor current is sensed by monitoring the voltage across an external sense resistor. When the voltage exceeds a reference voltage of 200 mV for more than approximately 3 µs, the PWM duty cycle is reduced to limit the current through the motor to this value. This current limit allows for starting the motor while controlling the current.

If the current limit condition persists for some time, it is likely that a fault condition has been encountered, such as the motor being run into a stop or a stalled condition. An overcurrent event must persist for approximately 275 ms before the fault is registered. After approximately 275 ms, a fault signaled to the host by driving the FAULTn signal low and setting the FAULT and ILIMIT bits in the serial interface register. Operation of the motor driver will continue.

The current limit fault condition is cleared by setting both IN1 and IN2 to zero to disable the motor current, by putting the device into the shutdown state (IN1 and IN2 both set to 1), by setting the CLEAR bit in the fault register, or by removing and re-applying power to the device.

The resistor used to set the current limit must be less than 1 Ω. Its value may be calculated as follows:

$$R_{ISENSE} = \frac{200\ mV}{I_{LIMIT}} \quad (1)$$

Where:

$R_{ISENSE}$ is the current sense resistor value.

$I_{LIMIT}$ is the desired current limit (in mA).

If the current limit feature is not needed, the ISENSE pin may be directly connected to ground.

## Protection Circuits

The DRV8830 is fully protected against undervoltage, overcurrent and overtemperature events. A FAULTn pin is available to signal a fault condition to the system, as well as a FAULT register in the serial interface that allows determination of the fault source.

### Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled, the FAULTn signal will be driven low, and the FAULT and OCP bits in the FAULT register will be set. The device will remain disabled until the CLEAR bit in the FAULT register is written to 1, or VCC is removed and re-applied.

Overcurrent conditions are sensed independently on both high and low side devices. A short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that OCP is independent of the current limit function, which is typically set to engage at a lower current level; the OCP function is intended to prevent damage to the device under abnormal (e.g., short-circuit) conditions.

### Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled, the FAULTn signal will be driven low, and the FAULT and OTS bits in the serial interface register will be set. Once the die temperature has fallen to a safe level operation will automatically resume.

### Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled, the FAULTn signal will be driven low, and the FAULT and UVLO bits in the FAULT register will be set. Operation will resume when VCC rises above the UVLO threshold.

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## I²C-Compatible Serial Interface

The I²C interface allows control and monitoring of the DRV8830 by a microcontroller. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C – Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with off-chip pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer.

A slave device receives and/or transmits data on the bus under control of the master device. This device operates only as a slave device.

I²C communication is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while SCL is held high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W). After receiving a valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse.

The lower three bits of the device address are input from pins A0 - A1, which can be tied to VCC (logic high), GND (logic low), or left open. These three address bits are latched into the device at power-up, so cannot be changed dynamically.

The upper address bits of the device address are fixed at 0xC0h, so the device address is as follows:

| A1 PIN | A0 PIN | A3..A0 BITS (as below) | ADDRESS (WRITE) | ADDRESS (READ) |
|---|---|---|---|---|
| 0 | 0 | 0000 | 0xC0h | 0xC1h |
| 0 | open | 0001 | 0xC2h | 0xC3h |
| 0 | 1 | 0010 | 0xC4h | 0xC5h |
| open | 0 | 0011 | 0xC6h | 0xC7h |
| open | open | 0100 | 0xC8h | 0xC9h |
| open | 1 | 0101 | 0xCAh | 0xCBh |
| 1 | 0 | 0110 | 0xCCh | 0xCDh |
| 1 | open | 0111 | 0xCEh | 0xCFh |
| 1 | 1 | 1000 | 0xD0h | 0xD1h |

The DRV8830 does not respond to the general call address.

A data byte follows the address acknowledge. If the R/W bit is low, the data is written from the master. If the R/W bit is high, the data from this device are the values read from the register previously selected by a write to the subaddress register. The data byte is followed by an acknowledge sent from this device. Data is output only if complete bytes are received and acknowledged. A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master to terminate the transfer.

A master bus device must wait at least 60 µs after power is applied to VCC to generate a START condition.

I²C transactions are shown in the timing diagrams below:

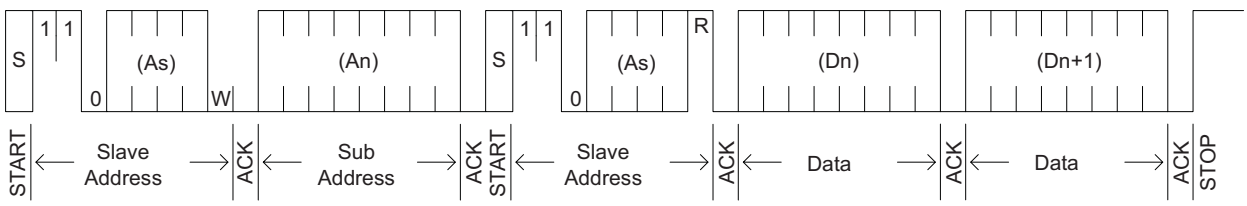



**Figure 7. I²C Read Mode**


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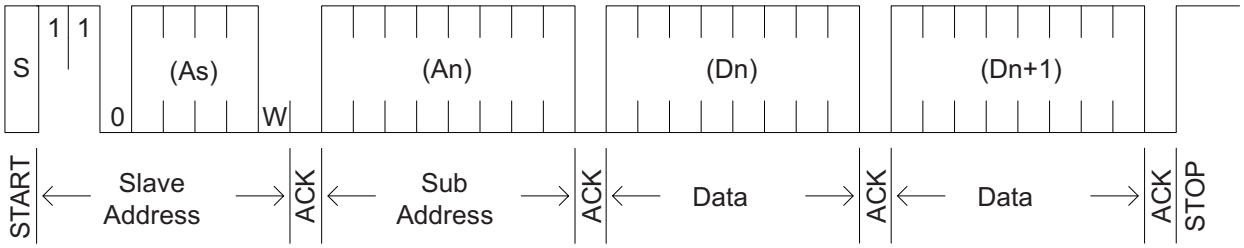



**Figure 8. I²C Write Mode**

## I²C Register Map

| REGISTER | SUB ADDRESS (HEX) | REGISTER NAME | DEFAULT VALUE | DESCRIPTION |
|---|---|---|---|---|
| 0 | 0x00 | CONTROL | 0x00h | Sets state of outputs and output voltage |
| 1 | 0x01 | FAULT | 0x00h | Allows reading and clearing of fault conditions |

### REGISTER 0 – CONTROL

The CONTROL register is used to set the state of the outputs as well as the DAC setting for the output voltage. The register is defined as follows:

| D7 - D2 | D1 | D0 |
|---|---|---|
| VSET[5..0] | IN2 | IN1 |

| | |
|---|---|
| VSET[5..0]: | Sets DAC output voltage. Refer to Voltage Setting above. |
| IN2: | Along with IN1, sets state of outputs. Refer to Bridge Control above. |
| IN1: | Along with IN2, sets state of outputs. Refer to Bridge Control above. |

### REGISTER 1 – FAULT

The FAULT register is used to read the source of a fault condition, and to clear the status bits that indicated the fault. The register is defined as follows:

| D7 | D6 - D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| CLEAR | Unused | ILIMIT | OTS | UVLO | OCP | FAULT |

| | |
|---|---|
| CLEAR: | When written to 1, clears the fault status bits |
| ILIMIT: | If set, indicates the fault was caused by an extended current limit event |
| OTS: | If set, indicates that the fault was caused by an overtemperature (OTS) condition |
| UVLO: | If set, indicates the fault was caused by an undervoltage lockout |
| OCP: | If set, indicates the fault was caused by an overcurrent (OCP) event |
| FAULT: | Set if any fault condition exists |

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## THERMAL INFORMATION

### Thermal Protection

The DRV8830 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 160°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

### Power Dissipation

Power dissipation in the DRV8830 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by Equation 2.

$$P_{TOT} = 2 \bullet R_{DS(ON)} \bullet (I_{OUT(RMS)})^2 \quad (2)$$

where $P_{TOT}$ is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.


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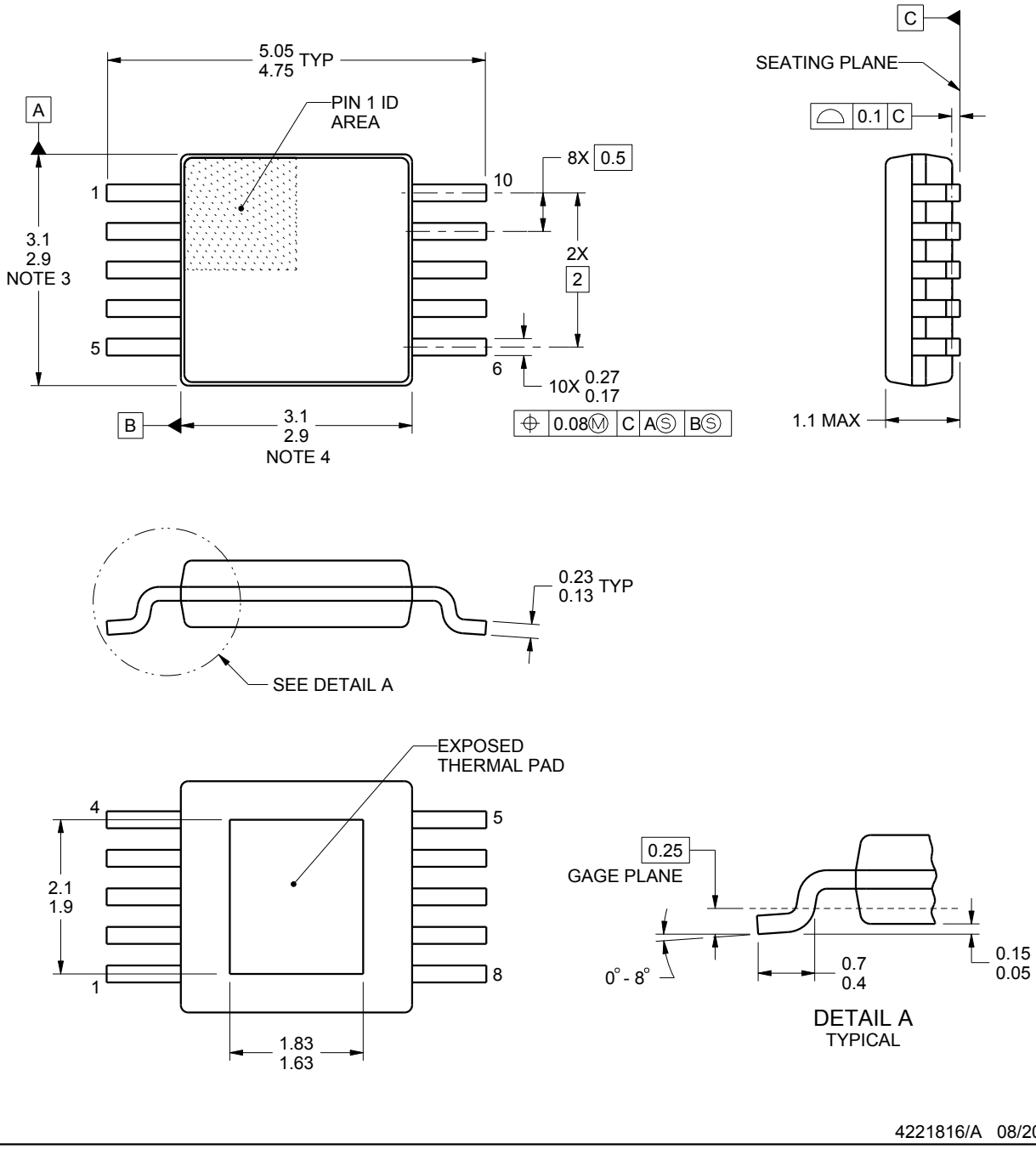


# PACKAGE OUTLINE

## DGQ0010E

## PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

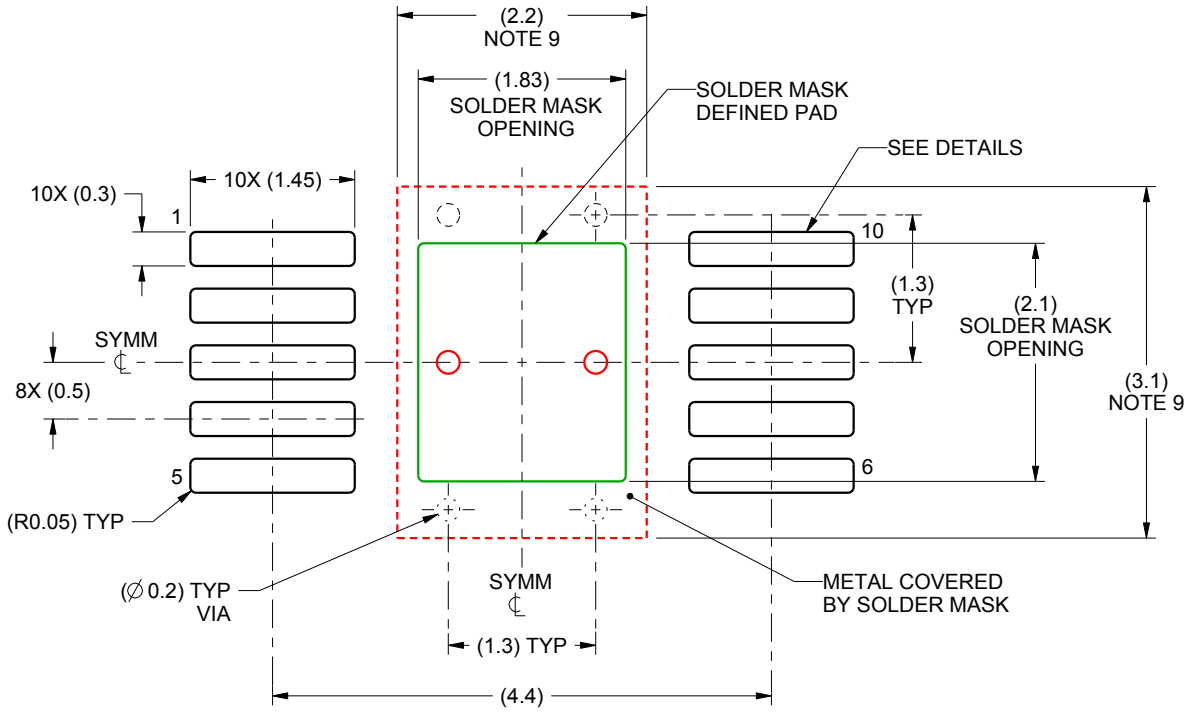



4221816/A 08/2015

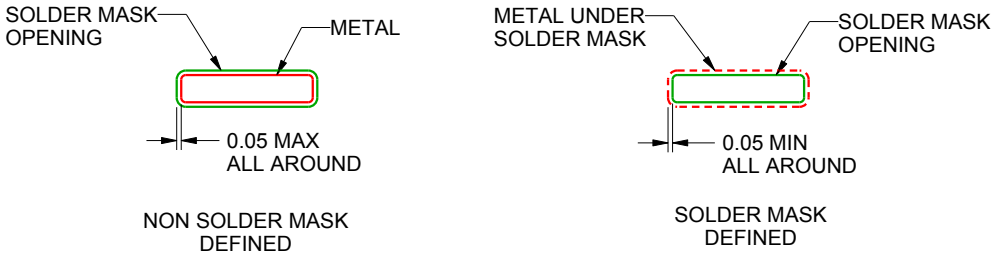
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.




LAND PATTERN EXAMPLE
SCALE:15X

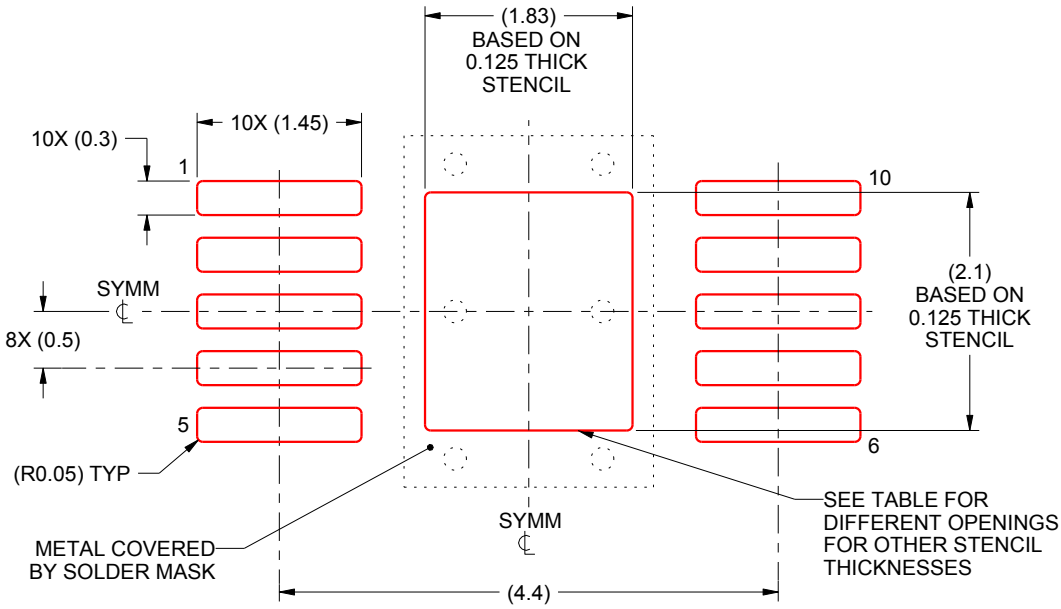



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.05 X 2.35 |
| 0.125 | 1.83 X 2.1 (SHOWN) |
| 0.150 | 1.67 X 1.92 |
| 0.175 | 1.55 X 1.77 |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8830DGQ | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | 8830 | Samples |
| DRV8830DGQR | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 85 | 8830 | Samples |
| DRV8830DRCR | ACTIVE | VSON | DRC | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 8830 | Samples |
| DRV8830DRCT | ACTIVE | VSON | DRC | 10 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 8830 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

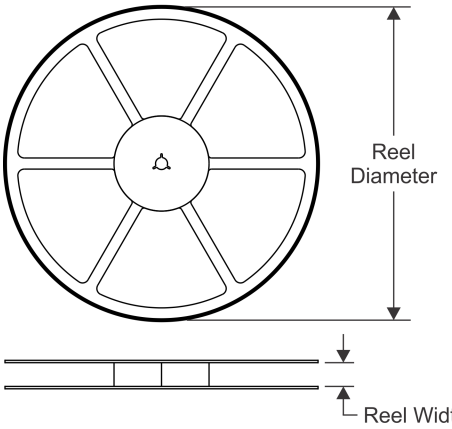
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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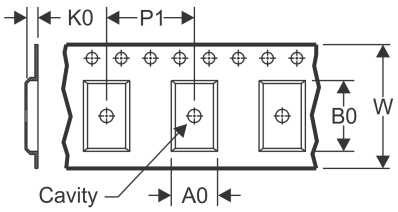
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

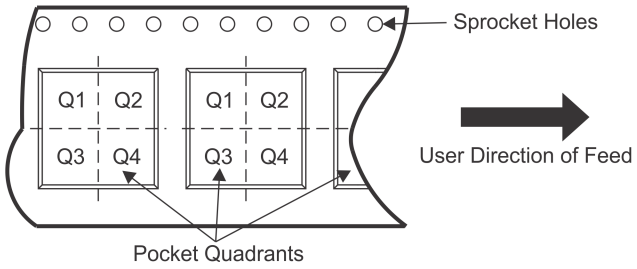



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

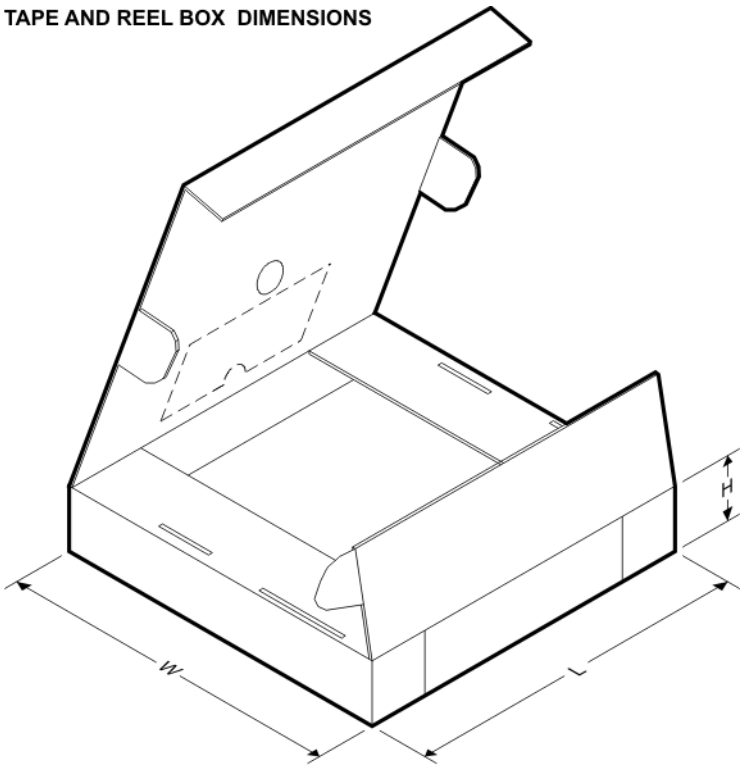
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DRV8830DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| DRV8830DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

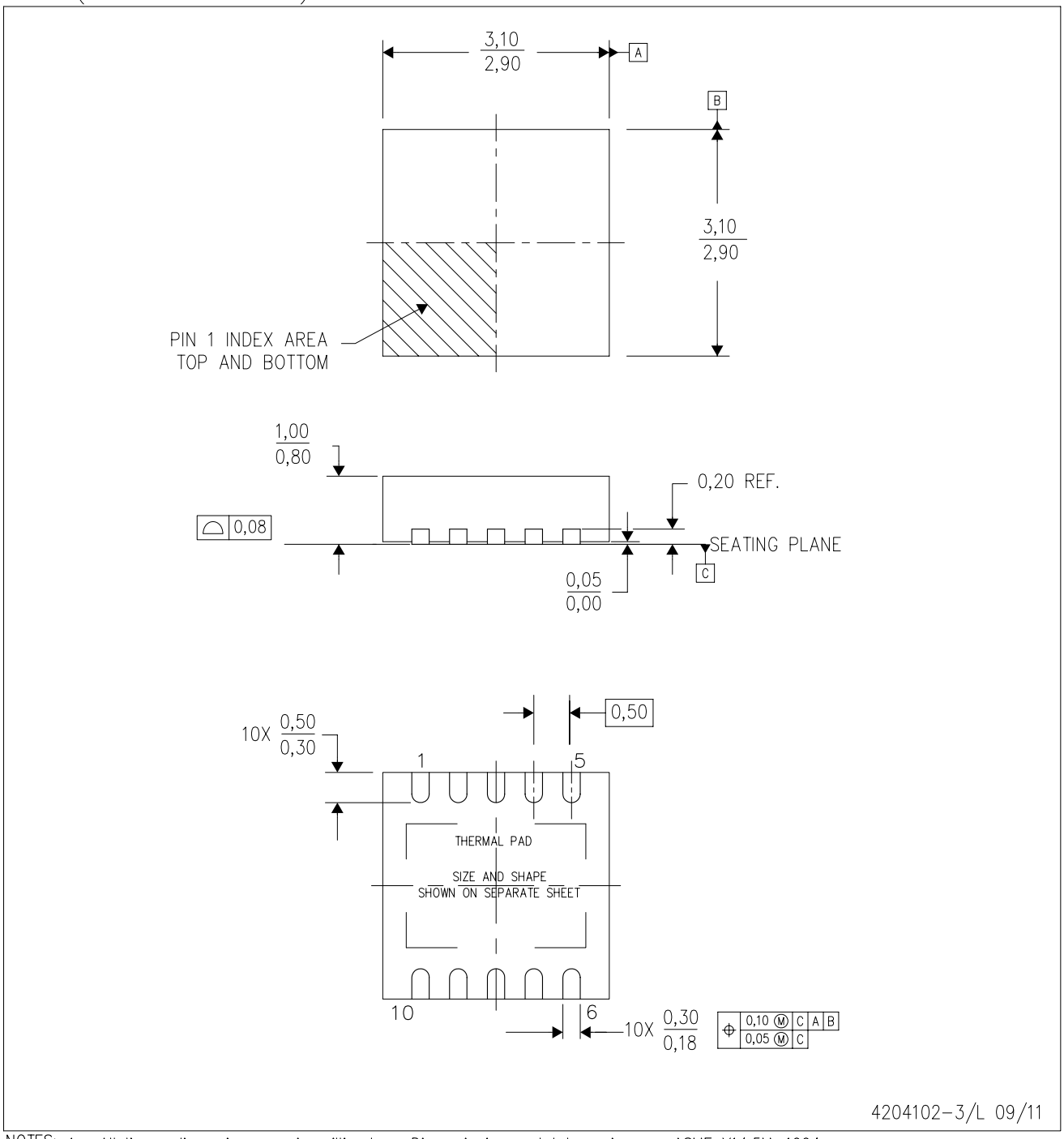
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DRV8830DRCR | VSON | DRC | 10 | 3000 | 367.0 | 367.0 | 35.0 |
| DRV8830DRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

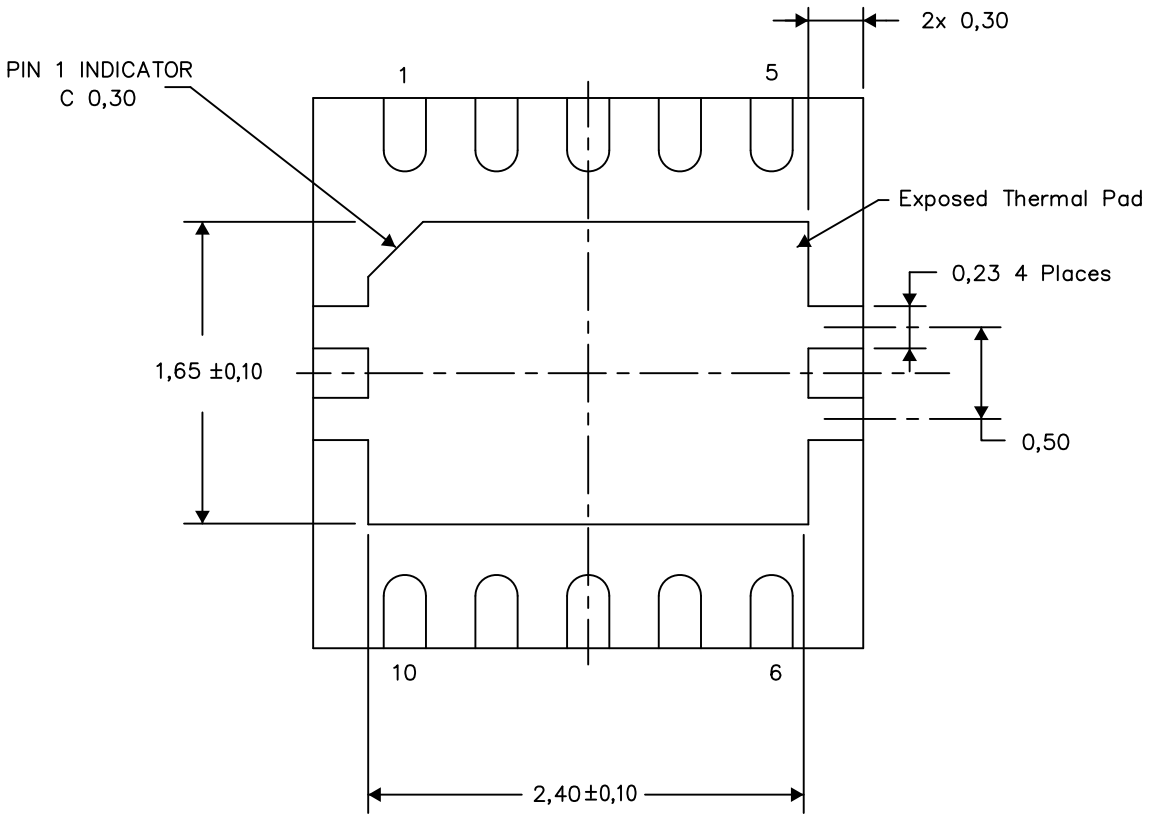
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



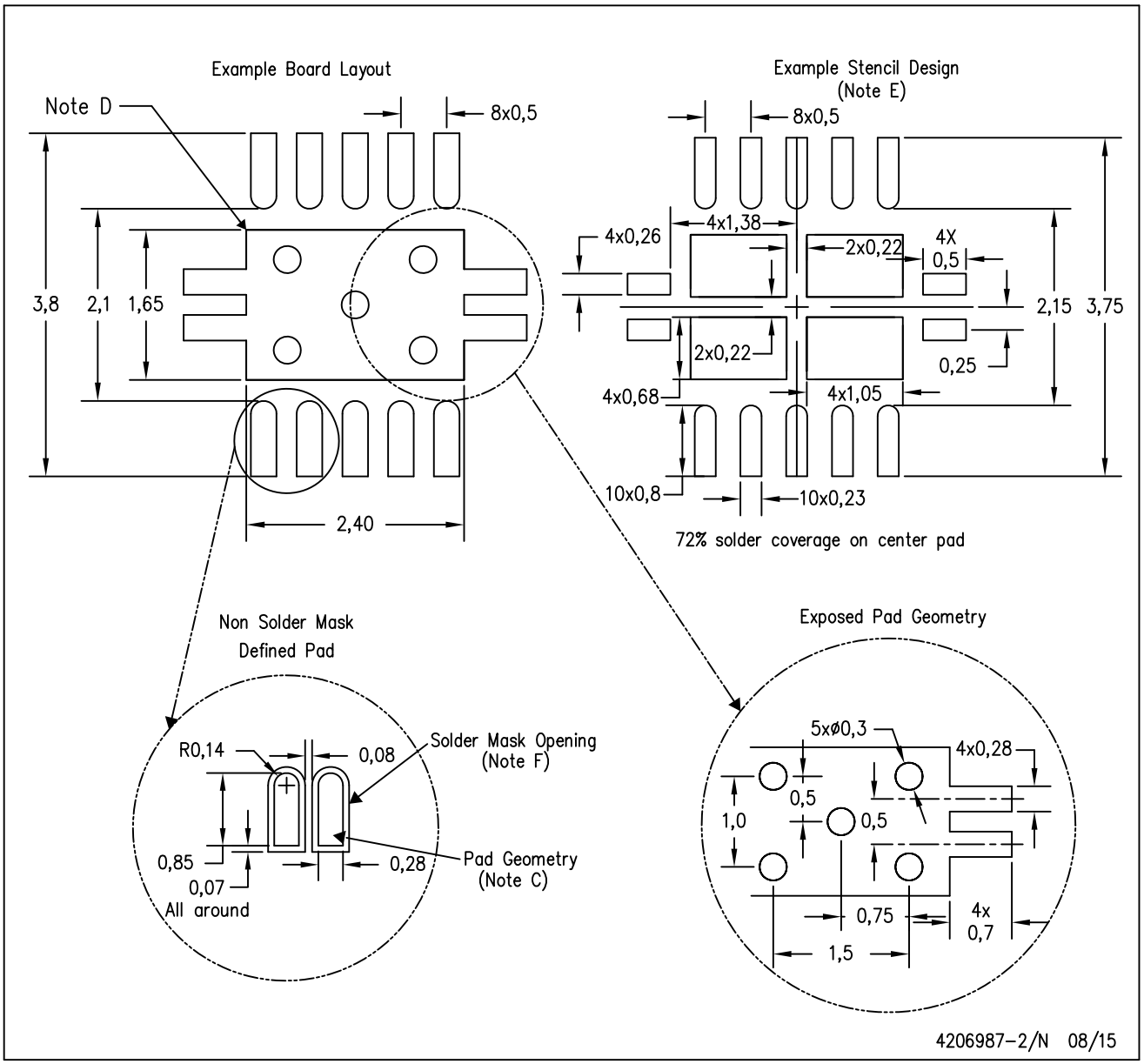

Bottom View

Exposed Thermal Pad Dimensions

4206565–3/X 07/15

NOTE: A. All linear dimensions are in millimeters

# DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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