AN4658
Application note

Migration of applications from STM32F429/439 lines to STM32F446 line

Introduction

For more and more applications using STM32 products, it is important to easily migrate a project to a different microcontroller in the same product family.

Migrating an application to a different microcontroller is needed, for instance, when product requirements grow, putting extra demands on memory size, or requiring an increase in the number of I/Os. On the other hand, cost reduction objectives may force to switch to cheaper components and towards shrinking the PCB area.

This application note is intended to help the user to analyze the steps needed to migrate from existing designs based on STM32F429xx and STM32F439xx products to STM32F446xx devices. It groups together all the most important information and lists the key items to address.

In this document the comparisons are carried out for “fully featured” microcontrollers of the STM32F429/439 and STM32F446 lines, user must consider that some products may have less features (depending on actual part number).

Migrating between two devices within the same family can require in some cases hardware and/or software changes: the required ones are described in this document.

To benefit fully from the information in this application note, the user should be familiar with the STM32 microcontroller family.

This application note has to be read in conjunction with STM32F429xx/STM32F439xx and STM32F446xx reference manuals (RM0090 and RM0390, respectively) and datasheets available at *www.st.com*.

Table 1. Applicable products

Product type	Product lines
Microcontrollers	STM32F429/439 STM32F446

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1 Hardware migration guide

Except for the LQFP100 and LQFP144 packages, the STM32F446xx devices are fully pin-to-pin compatible with the STM32F429xx/439xx devices, allowing the user to try different peripherals, and reaching higher performance (higher frequency) for a greater degree of freedom during the development cycle.

The transition from the STM32F429/439 lines to the STM32F446 line is simple since only a few pins are impacted, as summarized in *Table 2*.

Table 2. Pinout comparison (LQFP packages)

STM32F429xx/439xx			STM32F446xx		
QFP100	**QFP144**	**Pinout**	**QFP100**	**QFP144**	**Pinout**
48	-	PB11	48	-	VCAP1
49	-	VCAP1	49	-	VSS
-	70(1)	PB11 (OTG_HS_ULPI_D4)	-	70(1)	PB11
-	48(1)	PB2	-	48(1)	PB2 (OTG_HS_ULPI_D4)
-	95	VDD	-	95	VDDUSB

1. For the LQFP144 the PCB change is mandatory only when an external ULPI PHY is used in USB HS mode, otherwise no PCB update is needed.

1.1 Recommendations for board migration

For the LQFP100 package PB11 is not available anymore and it is replaced by VCAP1.

For the LQFP144 the PCB change is mandatory only when an external ULPI PHY is used in USB HS mode, otherwise no PCB update is needed.

A dedicated VDDUSB supply is used on STM32F446 and it is available only on LQFP144, UFBGA144 and WLCSP81 packages.

The pin PDR_ON used on STM32F429 to enable power supervisor is now managed in static way.

Figure 1 and *Figure 2* show two examples of board designs migrating from STM32F429 to STM32F446.

Figure 1. Compatible board design for LQFP100 package

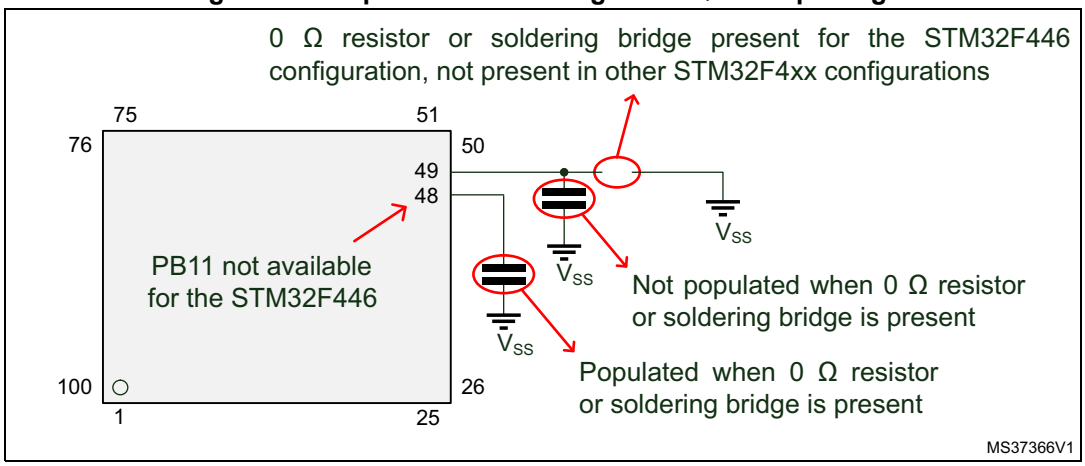
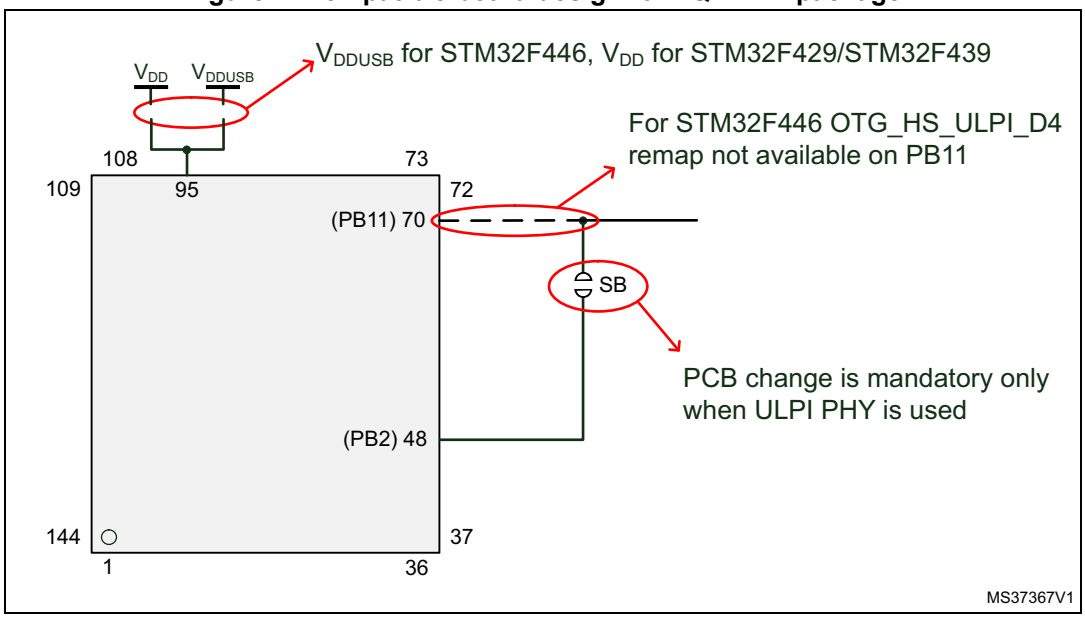


Figure 2. Compatible board design for LQFP144 package



2 Peripheral migration guide

2.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals that can be classed in three categories:

1. Peripherals which are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
2. Peripherals which are shared by all products but have only minor differences (in general to support new features), so migration from one product to another is very easy and does not need any significant new development effort.
3. Peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, migration will require new development at application level.

Table 3 summarizes the available peripherals and their compatibility between the STM32F429/439 and the STM32F446 lines.

Table 3. Peripheral compatibility analysis

Peripherals		STM32F429xx/439xx	STM32F446xx	Compatibility	
				SW	Comments
Flash memory (in Bytes)		2M	512K	-	-
SRAM (in KBytes)	System	256 (112+16+64+64)	128 (112+16)	-	-
	Backup	4	4	-	-
Timers	General Purpose	10	10	-	-
	Advanced control	2	2	-	-
	Basic	2	2	-	-

Table 3. Peripheral compatibility analysis (continued)

Peripherals		STM32F429xx/439xx	STM32F446xx	Compatibility	
				SW	Comments
Communication interfaces	SPI / I2S	6 / 2	4 / 3	API enhancement to handle new I2S clock sources	New clock source for I2S on APB2
	FMPI2C	No	1	-	New peripheral (new IOs to support FM+)
	USART / UART	4 / 4	4 /2	-	-
	USB OTG FS	Yes	Yes	-	Dedicated V_{DDUSB} More endpoints on STM32F446
	USB OTG HS				
	CAN	2	2	-	-
	SAI	1	2	API enhancement to handle new SAI clock sources	New clock source added
	SDIO/SDMMC	Yes	Yes	-	New clock source is SYSCLK
	SPDIF-RX	No	4 parallel inputs	-	New peripheral
RNG		Yes	No	-	-
QuadSPI		No	Yes	-	New peripheral
FMC (memory controller)		Yes	Yes	-	-
Ethernet		Yes	No	-	-
HDMI-CEC		No	Yes	-	-
DCMI		Yes	Yes	-	-
WWDG		Yes	Yes	-	-
IWDG		Yes	Yes	-	-
CRC		Yes	Yes	-	-
LCD-TFT		Yes	No	-	-
DMA		DMA1-DMA2 (8 streams each)		-	Enhanced dynamic power consumption
Chrom-Art-Accelerator™ DMA2D		Yes	No	-	-
Crypto		Yes	No	-	-
Hash		Yes	No	-	-
GPIOs		Up to 168	Up to 114	-	-

Table 3. Peripheral compatibility analysis (continued)

Peripherals		STM32F429xx/439xx	STM32F446xx	Compatibility	
				SW	Comments
ADC (12 bits)	Count	3	3	-	-
	Number of channels	16 / 24	16 / 24	-	-
DAC (12 bits)	Count	1	1	-	-
	Number of channels	2	2	-	-
RCC		Yes	Yes	-	More flexibility, with additional clock sources to AHB, USB and audio peripherals. Dedicated input clock divider input for PLL. New LSE mode.

The Cube Hardware Abstraction Layer (HAL) is compatible between the STM32F429/F439 and STM32F446 lines.

2.2 Memory mapping

Address mapping has been slightly changed in the STM32F446xx vs. STM32F429xx/439xx, the differences are shown in *Table 4*, where a gray cell indicates that the feature is not available (NA).

Table 4. Peripheral bus mapping comparison

Peripheral	Bus	STM32F429xx/439xx Base address	STM32F446xx Base address
QuadSPI Register	AHB3	NA	0xA000 1000
RNG	AHB2	0x5006 0800	NA
HASH		0x5006 0400	NA
CRYP		0x5006 0000	NA
DMA2D	AHB1	0x4002 B000	NA
ETHERNET MAC		0x40029000	NA
CPIOK		0x4002 2800	NA
GPIOJ		0x4002 2400	NA
GPIOI		0x4002 2000	NA

Table 4. Peripheral bus mapping comparison (continued)

Peripheral	Bus	STM32F429xx/439xx Base address	STM32F446xx Base address
LCD-TFT	APB2	0x4001 6800	NA
SPI6		0x4001 5400	NA
SPI5		0x4001 5000	NA
SAI2		NA	0x4001 5C00
UART8	APB1	0x4000 7C00	NA
UART7		0x4000 7800	NA
HDMI-CEC		NA	0x4000 6C00
I2S3ext		0x4000 4000	NA
SPDIFRX		NA	0x4000 4000
I2S2ext		0x4000 3400	NA

2.3 Flash memory

The differences between the Flash interface of STM32F446 products vs. those of the STM32F429/439 lines are indicated in *Table 5* (a gray cell indicates that the feature is not available).For more information on programming, erasing and protection of STM32F446xx, please refer to the RM0390 reference manual.

Table 5. Flash memory comparison

Flash	STM32F429xx/439xx	STM32F446xx
Main / Program memory	0x0800 0000 – (up to) 0x081F FFFF	0x0800 0000 - up to 0x0807 FFFF
	Up to 2 Mbytes (split in 2 banks) 4 sectors of 16 Kbytes 1 sector of 64 Kbytes 6 sectors of 128 Kbytes	Up to 512 Kbytes 4 sectors of 16 Kbytes 1 sector of 64 Kbytes 3 sectors of 128 Kbytes
Features	Read while Write (RWW) Dual Bank Boot	NA
Wait states	Up to 8 (depending on the supply voltage and frequency)	
One Time Programmable (OTP) memory	512 bytes	
Option bytes	0x1FFF C000 - 0x1FFF C00F 0x1FFE C000 - 0x1FFE C00F	0x1FFF C000 - 0x1FFF C00F
Interface	0x4002 3C00	

Table 5. Flash memory comparison (continued)

Flash	STM32F429xx/439xx	STM32F446xx
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	WDG_SW	IWDG_SW
	BOR_LEV[1:0]	BOR_LEV[2:0]
	BFB2	NA
	SPRMOD	SPRMOD
	DB1M	NA
	nWRP	nWRP

2.4 Flexible memory controller (FMC)

Table 6 presents the differences between the FMC features of STM32F429/439 and STM32F446 lines.

Table 6. FMC comparison

FMC		STM32F429xx/439xx	STM32F446xx
External memory interface		– SRAM – NOR/NAND memories – PSRAM (4 memory banks) – Two banks of NAND Flash memory with ECC hardware – 16-bit PC Card compatible devices	– SRAM – NOR/NAND memories – PSRAM (4 memory banks) – One bank of NAND Flash memory with ECC hardware
Data bus width		8, 16 or 32 bits	8 or 16 bits
FMC Bank memory mapping	Bank1 4x64MB	NOR/PSRAM/SRAM	NOR/PSRAM/SRAM
	Bank2 4x64MB	NAND Flash	Reserved
	Bank3 4x64MB	NAND Flash	NAND Flash
	Bank4 4x64MB	PC card	Reserved
	SDRAM Bank1 4x64MB	SDRAM	SDRAM
	SDRAM Bank2 4x64MB		

Table 6. FMC comparison (continued)

FMC		STM32F429xx/439xx	STM32F446xx
Memory mapping swap (SWP_FMC=01b)	0xD000 0000 to 0xDFFF FFFF	PC card 256 MB	Reserved
	0xC000 0000 to 0xCFFF FFFF	NAND Bank2 256 MB	NOR/RAM 256 MB
	0xA000 0000 to 0xAFFF FFFF	Registers	Registers
	0x9000 0000 to 0x9FFF FFFF	SDRAM Bank2 256 MB	QuadSPI 256 MB
	0x8000 0000 to 0x8FFF FFFF	SDRAM Bank1 256 MB	NAND Bank3 256 MB
	0x7000 0000 to 0x7FFF FFFF	NAND Bank1 256 MB	SDRAM Bank2 256 MB
	0x6000 0000 to 0x6FFF FFFF	NOR/RAM 256 MB	SDRAM Bank1 256 MB

2.5 Interrupts

Table 7 presents the interrupt vectors in the STM32F429/439 vs. the STM32F446 lines. Again, a gray cell indicates that the feature is not available.

Table 7. Interrupt vector comparison

Position	STM32F429xx/439xx	STM32F446xx
61	ETH	NA
62	ETH_WKUP	NA
79	CRYP	NA
80	HASH_RNG	NA
82	UART7	NA
83	UART8	NA
85	SPI5	NA
86	SPI6	NA
88	LCD-TFT	NA
89	LCD-TFT	NA
90	DMA2D	NA
91	NA	SAI2
92	NA	QUADSPI
93	NA	HDMI-CEC
94	NA	SPDIF-RX

Table 7. Interrupt vector comparison (continued)

Position	STM32F429xx/439xx	STM32F446xx
95	NA	FMP2C1
96	NA	FMPI2C1 error

2.6 RCC

The main differences related to Reset and Clock Controller in the STM32F446 line vs. the STM32F429/439 lines are presented in *Table 8*, where a gray cell indicates that the feature is not available.

Table 8. Reset and Clock Controller comparison

RCC	STM32F429xx/439xx	STM32F446xx
AHB	180 MHz	180 MHz
APB2	84 MHz	84 MHz
APB1	42 MHz	42 MHz
PLL	– One clock input divider for all PLLs (M factor)	– New dedicated clock input divider for each PLL – One input clock divider per PLL that needs to be configured before enabling the PLL
System clock (SYSCLK)	HSI/HSE	HSI/HSE
	PLL_P	PLL_P
		PLL_R
LSE modes	– One LSE mode is available: **low power**.	– New LSE modes are available in STM32446: **low power** and **high drive**. – User can select the LSE mode by configuring **RCC_BDCR[LSEMOD] bit**
Peripherals clock sources		
USB OTG FS / SDIO (PLL48CLK)	48 MHz from main PLL (PLLQ clock output)	48 MHz from main PLL (PLLQ clock output)
	-	48 MHz from PLLSAI (PLLSAIP clock output)
SDIO	PLL48CLK	PLL48CLK
		System clock (SYSCLK)
FMPI2C	NA	System clock (SYSCLK)
		HSI clock
		APB1 clock (PCLK1)

Table 8. Reset and Clock Controller comparison (continued)

RCC		STM32F429xx/439xx	STM32F446xx
I2S	Clock source for I2S on APB1	PLLI2SCLK	PLLI2SCLK
			I2S_CKIN
		I2S_CKIN	HSE/HSI
			Main PLL (PLLR output clock)
	Clock source for I2S on APB2	PLLI2SCLK	PLLI2SCLK
			I2S_CKIN
		NA	HSE/HSI
			Main PLL (PLLR output clock)
SAI1		PLLI2SQ(1)	PLLI2SQ(2)
		PLLSAIQ(1)	PLLSAIQ(2)
		I2S_CKIN(1)	I2S_CKIN(2)
		NA	Main PLL (PLLR output clock)(2)
SAI2		NA	PLLI2SQ(2)
			PLLSAIQ(2)
			I2S_CKIN(2)
			Main PLL (PLLR output clock)(2)
SPDIF-RX		NA	Main PLL (PLLR output clock)
HDMI-CEC		NA	LSE clock
			HSI clock divided by 488

1. Configurable clock per SAI sub-block.
2. Configurable clock per SAI block.

2.7 RTC

The STM32F446 and STM32F429/439 lines implement the same features on the RTC, as shown in *Table 9*.

Table 9. RTC comparison

RTC	STM32F429xx/439xx	STM32F446xx
Calendar in BCD	Yes	Yes
Calendar Sub seconds access	Yes	Yes
Calendar synchronization on the fly	Yes	Yes
Alarm on calendar	2 with subseconds	
Calendar Calibration	Calibration window: 8s / 16s / 32s Calibration step: 3.81ppm / 1.91ppm / 0.95 ppm Range [-480ppm +480ppm]	
Synchronization on mains	Yes	Yes

Table 9. RTC comparison

RTC	STM32F429xx/439xx	STM32F446xx
Periodic wakeup	Yes	Yes
Timestamp	Yes Sec, Min, Hour, Date, Sub-seconds	
RTC alternate functions pin	RTC_AF0 → PC13	
	RTC_AF1 → PI8	RTC_AF1 → PA0
RTC in Vbat	Yes	Yes

2.8 PWR

In STM32F446 lines the PWR controller presents some differences vs. STM32F429/439 lines, as highlighted in *Table 10*, where a gray cell indicates that the feature is not available.

Table 10. PWR comparison

PWR		STM32F429xx/439xx	STM32F446xx
Power supplies		NA	Independent USB transceivers supply (V_{DDUSB}). V_{DDUSB} supplies USB DP/DM pins. When internal USB PHY is used, V_{DDUSB} range is from 3.0 to 3.6 V, and is completely independent from V_{DD} or V_{DDA}. When internal USB PHY is not used V_{DDUSB} can be connected to V_{DD}.
Power control registers	PWR_CR(1)	NA	Added bits: – PWR_CR[FMSSR]: used to Stop the Flash Interface while System is in Run mode – PWR_CR[FMSSR]: used to force Flash into STOP or Deep Power Down mode while System is in Run mode
	PWR_CSR(2)	Only one wakeup pin available	Added / modified bits: – PWR_CSR [EWUP1] and PWR_CSR [EWUP2]: Wakeup Pin 1 and Wakeup Pin 2 Enable/Disable bits.

1. See *Table 11*
2. See *Table 12*

The added bits in PWR_CR and PWR_CSR registers are shown in *Table 11* and *Table 12*, respectively: the new features are highlighted in red, while blue indicates same feature with specification change or enhancement. Reserved bits are in light gray.

Table 11. PWR_CR register for STM32F446xx products

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	FISSR	FMSSR	UDEN[1:0]		ODSWEN	ODEN
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOS[1:0]		ADCDC1	Res.	MRUDS	LPUDS	FPDS	DBP	PLS[2:0]			PVDE	CSBF	CWUF	PDDS	LPDS

Table 12. PWR_CSR register for STM32F446xx products

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	UDRDY[1:0]		ODSWRDY	ODRDY
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	VOSRDY	Res.	Res.	Res.	Res.	BRE	EWUP1	EWUP2	Res.	Res.	Res.	BRR	PVDO	SBF	WUF

2.9 U(S)ART

The STM32F446 includes the Same USART interface used in the STM32F429/439, as indicated in *Table 13*.

Table 13. USART comparison

U(S)ART	STM32F429xx/439xx	STM32F446xx
UART/USART	4 / 4	4 / 2
Baudrate	up to 4x11.25 Mbit/s	
Clock	Single clock domain	
Data	Word length: programmable (8 or 9 bits)	
Interrupt	10 interrupt sources with flags	
Features	LIN mode SPI Master IrDA SIR ENDEC block Hardware flow control (CTS/RTS) Continuous communication using DMA Multiprocessor communication Single-wire half-duplex communication	

2.10 I2C

The STM32F446xx implements exactly the same features on the I2C interface (I2C1, I2C2 and I2C3) as the STM32F429xx/439xx.

2.11 Audio interfaces

The STM32F429/439 and STM32F446 lines implement the same features on the SPI, apart from I2S. This is clear from *Table 14*, where a gray cell indicates that the feature is not available. The added bit in SPI_I2SCFGR register is shown in *Table 15*, where the new feature is highlighted in red, and reserved bits are in light gray.

Table 14. Audio interfaces comparison

Audio interfaces	Description	STM32F429xx/439xx	STM32F446xx
SPI/I2S	Instances	x6 | x2 (SPI/I2S)	x4 | x3 (SPI/I2S)
	Features	– I²S Full duplex – SPI TI mode support – SPI Motorola support	– 3 I²S Half duplex – SPI TI mode support – SPI Motorola support – Enhanced clock source for I2S on APB1 and APB2
	Modifications	NA	Added bit SPI_I2SCFGR(1) [ASTREN]: allows to configure the I2S peripheral in asynchronous start mode.
SAIs	Instances	x1 (SAI)	x2 (SAI)
	Features	Clock source for each SAI sub-block to target independent audio frequency sampling	Internal synchronization between the two SAIs. Clock source for each SAI block to target independent audio frequency sampling.
SPDIFRx	Instances	NA	x1 (SPIDIFRx)

1. See *Table 15*

Table 15. SPI_I2SCFGR register for STM32F446xx products

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	ASTREN	I2SMOD	I2SE	I2SCFG		PCMSYNC	Res.	I2SSTD		CKPOL	DATLEN		CHLEN

2.12 CRC

The STM32F446xx implements CRC (Cyclic redundancy check) unit calculation similarly to STM32F429xx/439xx, the main features are listed in *Table 16*.

Table 16. CRC features for STM32F429xx/439xx and STM32F446xx

CRC	STM32F429xx/439xx and STM32F446xx
Features	Single input/output 32-bit data register CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size General-purpose 8-bit register (can be used for temporary storage) Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7 Handles 32-bit data size

2.13 USB OTG

The STM32F446xx and STM32F429xx/439xx implement similar USB peripherals, as shown in *Table 17*, where a gray cell indicates a not available feature.

Table 17. USB comparison

USB	STM32F429xx/439xx	STM32F446xx
Features	Universal Serial Bus Revision 2.0 Full support for the USB On-The-Go (USB OTG) USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	
	NA	Independent V_{DDUSB} power supply allowing lower V_{DD} (down to 1.8 V) while using USB
	FS mode	
	1 bidirectional control endpoint 3 IN endpoints (Bulk, Interrupt, Isochronous) 3 OUT endpoints (Bulk, Interrupt, Isochronous	1 bidirectional control endpoint 5 IN endpoints (Bulk, Interrupt, Isochronous) 5 OUT endpoints (Bulk, Interrupt, Isochronous)
	HS mode	
	6 bidirectional endpoints (including EP0) 12 Host mode channels	
Buffer memory	**FS mode**	
	Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO	Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO
	HS mode	
	4 KB total RAM	
Low-power modes	**FS mode**	
	USB suspend and resume	USB suspend and resume Link Power Management (LPM) support
	HS mode	
	LPM not supported	LPM supported

2.14 Digital camera interface (DCMI)

The STM32F429xx/439xx and STM32F446xx products have similar DCMI peripherals, as can be seen in *Table 18*, where a gray cell indicates that the feature is not available.

Table 18. DCMI comparison

DCMI	STM32F429xx/439xx	STM32F446xx
Parallel interface	8-, 10-, 12- and 14-bits	
Embedded synchronization	Yes	Yes
External line and frame synchronization	Yes	Yes
Crop feature	Yes	Yes
Supported data formats	8/10, 12, 14 bits progressive video (monochrome or raw bayer)	
	RGB565 progressive video	
	YCbCr4:2:2	
	8/10, 12, 14 bits progressive video (monochrome or raw bayer)	
	NA	YCbCr – Y only (Black and White)
	NA	Half resolution image extraction
	Compressed JPEG	
DCMI control register(1)	NA	Added bits: – DCMI_CR [BSM] and DCMI_CR [OEBS]: allows configuring the byte selection for capture – DCMI_CR [LSM] and DCMI_CR [OELS]: allows configuring the line selection for capture

1. See *Table 19*

The added bits in DCMI registers are shown in *Table 19*, the new features are highlighted in red, and reserved bits are in light gray.

Table 19. DCMI_CR register for STM32F446xx products

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	OELS	LSM	OEBS	BSM	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	ENABLE	Res.	Res.	EDM		FCRC		VSPOL	HSPOL	PCKPOL	ESS	JPEG	CROP	CM	CAPTURE

2.15 Secure digital input/output interface (SDIO)

The STM32F429xx and STM32F446xx products implement very similar SDIO module. The key differences are listed in *Table 20*, where a gray cell indicates that the feature is not available.

Table 20. SDIO comparison

SDIO	STM32F429xx/439xx	STM32F446xx
Features	Full compliance with MultiMediaCard System Specification Version 4.2 Full compliance with SD Memory Card Specifications Version 2.0 Full compliance with SD I/O Card Specification Version 2.0	
	Full support of the CE-ATA features	NA
SDMMC registers(1)	-	CE-ATA protocol related features removed from specification (updated SDIO_STA, SDIO_ICR and SDIO_CMD registers)

1. See *Table 21*, *Table 22* and *Table 23*.

The added bits in DCMI registers are shown in *Table 21*, *Table 22* and *Table 23*, where the changes are highlighted in red, and reserved bits are in light gray.

Table 21. SDIO_STA register for STM32F446xx products

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	SDIOIT	RXD AVL	TXD AVL	RX FIFOE	TX FIFOE	RX FIFOF	TX FIFOF
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX FIFO HF	TX FIFO HE	RXACT	TXACT	CMD ACT	DBCK END	Res.	DATA END	CMDS ENT	CMDR END	RX OVERR	TXUND ERR	DTIME OUT	CTIME OUT	DCRC FAIL	CCRC FAIL

Table 22. SDIO_ICR register for STM32F446xx products

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	SDIO ITC	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	DBCK ENDC	Res.	DATA ENDC	CMD SENTC	CMD RENDC	RX OVERRC	TX UNDERRC	DTIME OUTC	CTIME OUTC	DCRC FAILC	CCRC FAILC

Table 23. SDIO_CMD register for STM32F446xx products

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	SDIO Suspend	CPSM EN	WAIT PEND	WAIT INT	WAITRESP		CMDINDEX					

2.16 ADC/DAC

The STM32F446 and the STM32F429/439 lines implement the very same features on the ADC and DAC peripherals.

3 Conclusion

This application note is a useful complement to datasheets and reference manuals as it provides a simple guide to migrate from an existing design based on STM32F429xx/439xx devices to one using STM32F446xx products.

4 Revision history

Table 24. Document revision history

Date	Revision	Changes
18-Mar-2015	1	Initial release

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