CY28341-3

Universal Clock Chip for VIA™P4M/KT/KM400A DDR Systems

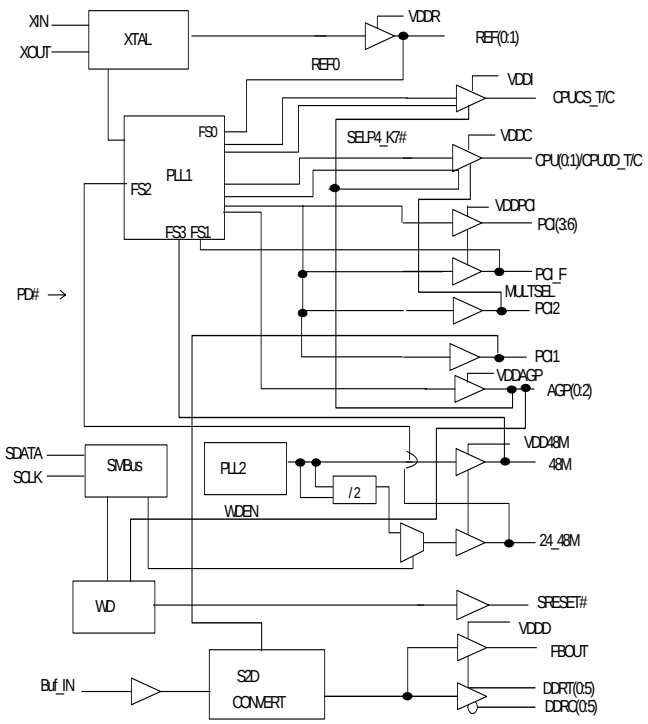
Features

- Supports VIA P4M/KM/KT/266/333/400A chipsets
- Supports Intel® Pentium® 4, Athlon™ processors
- Supports two DDR DIMMS
- Provides:
  - — Two different programmable CPU clock pairs
  - — Six differential DDR pairs
  - — Three low-skew/-jitter AGP clocks
  - — Seven low-skew/-jitter PCI clocks
  - — One 48M output for USB
  - — One programmable 24M or 48M for SIO
- Dial-A-Frequency® and Dial-A-dB™ features
- Spread Spectrum for best EMI reduction
- Watchdog feature for system recovery
- SMBus-compatible for programmability
- 56-pin SSOP and TSSOP packages

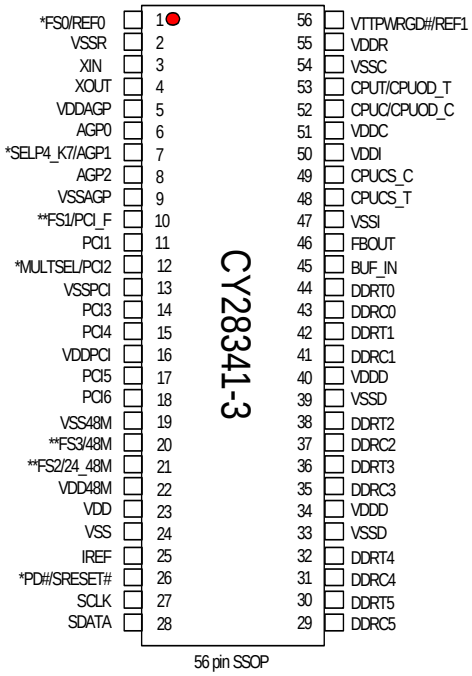
Table 1. Frequency Selection Table

FS(3:0)	CPU	AGP	PCI
0000	100.9	67.3	33.6
0001	100.0	66.7	33.3
0010	133.9	66.9	33.5
0011	133.3	66.7	33.3
0100	110.0	73.3	36.7
0101	145.2	72.6	36.3
0110	180.0	72.0	36.0
0111	198.4	71.7	35.8
1000	200.9	66.9	33.5
1001	200.0	66.7	33.3
1010	166.9	66.8	33.4
1011	166.6	66.6	33.3
1100	100.0	66.7	33.3
1101	133.3	66.7	33.3
1110	200.0	66.7	33.3
1111	166.6	66.6	33.3

Block Diagram



Pin Configuration[1]



Note:
1. Pins marked with [*] have internal 250 KΩ pull-up resistors. Pins marked with [**] have internal 250 KΩ pull-down resistors.

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Pin Description[2]

Pin Number	Pin Name	PWR	I/O	Pin Description
3	XIN		I	**Oscillator Buffer Input**. Connect to a crystal or to an external clock.
4	XOUT	VDD	O	**Oscillator Buffer Output**. Connect to a crystal. Do not connect when an external clock is applied at XIN.
1	FS0/REF0	VDDR	I/O PU	**Power-on Bidirectional Input/Output**. At power-up, FS0 is the input. When the power supply voltage crosses the input threshold voltage, FS0 state is latched and this pin becomes REF0, buffered copy of signal applied at XIN. (1-2 x strength, selectable by SMBus. Default value is 1 x strength.)
56	VTTPWRGD#	VDDR	I	**If SELP4_K7 = 1, with a P4 processor set up as CPUT/C**. At power-up, VTT_PWRGD# is an input. When this input transitions to a logic low, the FS (3:0) and MULTSEL are latched and all output clocks are enabled. After the first high to low transition on VTT_PWRGD#, this pin is ignored and will not effect the behavior of the device thereafter. When the VTT_PWRGD# feature is not used, please connect this signal to ground through a 10KΩ resistor.
	REF1	VDDR	O	**If SELP4_K7 = 0, with an Athlon (K7) processor as CPU_OD(T:C)**. VTT_PWRGD# function is disabled, and the feature is ignored. This pin becomes REF1 and is a buffered copy of the signal applied at XIN.
44,42,38, 36,32,30	DDRT (0:5)	VDDD	O	**DDR Clock Outputs**.
43,41,37 35,31,29	DDRC (0:5)	VDDD	O	**DDR Clock Outputs**.
7	SELP4_K7 / AGP1	VDDAGP	I/O PU	**Power-on Bidirectional Input/Output**. At power-up, SELP4_K7 is the input. When the power supply voltage crosses the input threshold voltage, SELP4_K7 state is latched and this pin becomes AGP1 clock output. SELP4_K7 = 1, P4 mode. SELP4_K7 = 0, K7 mode.
12	MULTSEL/PCI2	VDDPCI	I/O PU	**Power-on Bidirectional Input/Output**. At power-up, MULTSEL is the input. When the power supply voltage crosses the input threshold voltage, MULTSEL state is latched and this pin becomes PCI2 clock output. MULTSEL = 0, Ioh is 4 x IREFMULTSEL = 1, Ioh is 6 x IREF
53	CPUT/CPUOD_T	VDDC	O	**3.3V CPU Clock Outputs**. This pin is programmable through strapping pin7, SELP4_K7. If SELP4_K7 = 1, this pin is configured as the CPUT Clock Output. If SELP4_K7 = 0, this pin is configured as the CPUOD_T Open Drain Clock Output. See *Table 1*
52	CPUC/CPUOD_C	VDDC	O	**3.3V CPU Clock Outputs**. This pin is programmable through strapping pin7, SELP4_K7. If SELP4_K7 = 1, this pin is configured as the CPUC Clock Output. If SELP4_K7 = 0, this pin is configured as the CPUOD_C Open Drain Clock Output. See *Table 1*
48,49	CPUCS_T/C	VDDI	O	2.**5V CPU Clock Outputs for Chipset**. See *Table 1*.
14,15,17,18	PCI (3:6)	VDDPCI	O	**PCI Clock Outputs**. Are synchronous to CPU clocks. See *Table 1*
10	FS1/PCI_F	VDDPCI	I/O PD	**Power-on Bidirectional Input/Output**. At power-up, FS0 is the input. When the power supply voltage crosses the input threshold voltage, FS1 state is latched and this pin becomes PCI_F clock output.
20	FS3/48M	VDD48M	I/O PD	**Power-on Bidirectional Input/Output**. At power-up, FS3 is the input. When the power supply voltage crosses the input threshold voltage, FS3 state is latched and this pin becomes 48M, a USB clock output.
11	PCI1	VDDPCI	I/O PD	**PCI Clock Output**.
21	FS2/24_48M	VDD48M	I/O PD	**Power-on Bidirectional Input/Output**. At power-up, FS2 is the input. When the power supply voltage crosses the input threshold voltage, FS2 state is latched and this pin becomes 24_48M, a SIO programmable clock output.
6	AGP0	VDDAGP	O	**AGP Clock Output**. Is synchronous to CPU clocks. See *Table 1*.
8	AGP2	VDDAGP	O	**AGP Clock Output**. Is synchronous to CPU clocks. See *Table 1*.

Note:
2. PU = internal pull-up. PD = internal pull-down. Typically = 250 KΩ (range 200 KΩ to 500 KΩ).

Pin Description[2] (continued)

Pin Number	Pin Name	PWR	I/O	Pin Description
25	IREF		I	**Current reference programming input for CPU buffers**. A precise resistor is attached to this pin, which is connected to the internal current reference.
28	SDATA		I/O	**Serial Data Input**. Conforms to the Phillips I2C specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
27	SCLK		I	**Serial Clock Input**. Conforms to the Philips I2C specification.
26	PD#/SRESET#		I/O PU	**Power-down Input/System Reset Control Output**. If Byte6 Bit7 = 0(default), this pin becomes a SRESET# open drain output. See system reset description. If Byte6Bit7 = 1, this pin becomes PD# input with an internal pull-up. When PD# is asserted low, the device enters power down mode. See power management function.
45	BUF_IN			**Input to DDR Differential Buffers**.
46	FBOUT			**2.5V single-ended SDRAM buffered output of the signal applied at BUF_IN**.
5	VDDAGP			**3.3V power supply for AGP clocks**.
51	VDDC			**3.3V power supply for CPUT/C clocks**.
16	VDDPCI			**3.3V power supply for PCI clocks**.
55	VDDR			**3.3V power supply for REF clock**.
50	VDDI			**2.5V power supply for CPUCS_T/C clocks**.
22	VDD_48M			**3.3V power supply for 48M**.
23	VDD			**3.3V Common power supply**.
34,40	VDDD			**2.5V power supply for DDR clocks**.
9	VSSAGP			**Ground for AGP clocks**.
13	VSSPCI			**Ground for PCI clocks**.
54	VSSC			**Ground for CPUT/C clocks**.
33,39	VSSD			**Ground for DDR clocks**.
19	VSS_48M			**Ground for 48M clock**.
47	VSSI			**Ground for CPUCS_T/C clocks**.
2	VSSR			**Ground for REF**.
24	VSS			**Common Ground**.

Power Management Functions

All clocks can be individually enabled or stopped via the two-wire control interface. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stop and on transitions from stopped to running when the chip was not powered down. On power up, the VCOs will stabilize to the correct pulse widths within about 0.5 mS.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '00000000' stands for block operation	11:18	Command Code – 8 bits '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge from master
....	.....	39:46	Data byte from slave – 8 bits
....	Data Byte (N–1) –8 bits	47	Acknowledge from master
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Data Byte N –8 bits	56	Acknowledge from master
....	Acknowledge from slave	....	Data byte N from slave – 8 bits
....	Stop	....	Acknowledge from master
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '100xxxxx' stands for byte operation, bits[4:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '100xxxxx' stands for byte operation, bits[4:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits

Table 4. Byte Read and Byte Write Protocol (continued)

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Acknowledge from master
		39	Stop

Serial Control Registers

Byte 0: Frequency Select Register

Bit	@Pup	Pin#	Name	Description
7	0		Reserved	Reserved
6	H/W Setting	21	FS2	For Selecting Frequencies in *Frequency Selection Table on page 1*
5	H/W Setting	10	FS1	For Selecting Frequencies in *Frequency Selection Table on page 1*
4	H/W Setting	1	FS0	For Selecting Frequencies in *Frequency Selection Table on page 1*
3	0		FS_Override	If this bit is programmed to “1”, it enables WRITE to bits (6:4,1) for selecting the frequency via software (SMBus) If this bit is programmed to a “0” it enable only READ of bits (6:4,1), which reflect the hardware setting of FS(0:3).
2	0	11	Reserved	Reserved, set = 0
1	H/W Setting	20	FS3	For Selecting frequencies in *Frequency Selection Table on page 1*
0	H/W Setting	7	SELP4_K7	Only for reading the hardware setting of the CPU interface mode, status of SELP4_K7# strapping.

Byte 1: CPU Clocks Register

Bit	@Pup	Pin#	Name	Description
7	0		MODE	0 = Down Spread. 1 = Center Spread. *See Table 9* on page 8
6	1		SSCG	1 = Enable (default). 0 = Disable
5	1		SST1	Select spread bandwidth. *See Table 9* on page 8
4	1		SST0	Select spread bandwidth. *See Table 9* on page 8
3	1	48,49	CPUCS_T, CPUCS_C	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
2	1	53,52	CPUT/CPUOD_T CPUC/CPUOD_C	1 = output enabled (running). 0 = output disable.
1	0	53,52	CPUT/C	In K7 mode, this bit is ignored.In P4 mode, 0 = when PD# asserted LOW, CPUT stops in a high state, CPUC stops in a low state. In P4 mode, 1 = when PD# asserted LOW, CPUT and CPUC stop in High-Z.
0	1	11	MULT0	Only for reading the hardware setting of the Pin11 MULT0 value.

Byte 2: PCI Clock Register

Bit	@Pup	Pin#	Name	Description
7	0		PCI_DRV	PCI clock output drive strength 0 = Low strength, 1 = High strength
6	1	10	PCI_F	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
5	1	18	PCI6	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
4	1	17	PCI5	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
3	1	15	PCI4	1 = output enabled (running). 0 = output disabled asynchronously in a low state.

Byte 2: PCI Clock Register (continued)

2	1	14	PCI3	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
1	1	12	PCI2	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
0	1	11	PCI1	1 = output enabled (running). 0 = output disabled asynchronously in a low state.

Byte 3: AGP/Peripheral Clocks Register

Bit	@Pup	Pin#	Name	Description
7	0	21	24_48M	0 = pin21 output is 24MHz. Writing a '1' into this register asynchronously changes the frequency at pin21 to 48 MHz.
6	1	20	48MHz	1 = output enabled (running). 0 = output disabled asynchronously in a low
5	1	21	24_48M	1 = output enabled (running). 0 = output disabled asynchronously in a low
4	0	6,7,8	DASAG1	Programming these bits allow shifting skew of the AGP(0:2) signals relative to their default value. See *Table 5*.
3	0	6,7,8	DASAG0	
2	1	8	AGP2	1 = output enabled (running). 0 = output disabled asynchronously in a low
1	1	7	AGP1	1 = output enabled (running). 0 = output disabled asynchronously in a low
0	1	6	AGP0	1 = output enabled (running). 0 = output disabled asynchronously in a low

Table 5. Dial-a-Skew™ AGP(0:2)

DASAG (1:0)	AGP(0:2) Skew Shift
00	Default
01	–280 ps
10	+280 ps
11	+480 ps

Byte 4: Peripheral Clocks Register

Bit	@Pup	Pin#	Name	Description
7	1	20	48M	1 = Low strength, 0 = High strength
6	1	21	24_48M	1 = Low strength, 0 = High strength
5	0	6,7,8	DARAG1	Programming these bits allow modifying the frequency ratio of the AGP(2:0), PCI(6:1, F) clocks relative to the CPU clocks. See *Table 6*.
4	0	6,7,8	DARAG0	
3	1	1	REF0	1 = output enabled (running). 0 = output disabled asynchronously in a low
2	1	56	REF1	1 = output enabled (running). 0 = output disabled asynchronously in a low
1	1	1	REF0	1 = Low strength, 0 = High strength
0	1	56	REF1	1 = Low strength, 0 = High strength (K7 Mode only)

Table 6. Dial-A-Ratio™ AGP(0:2)

DARAG (1:0)	CU/AGP Ratio
00	Frequency Selection Default
01	2/1
10	2.5/1
11	3/1

Byte 5: SDR/DDR Clock Register

Bit	@Pup	Pin#	Name	Description
7	0	45	BUF_IN threshold voltage	DDR Mode, BUF_IN threshold setting. 0 = 1.15V, 1 = 1.05V
6	1	46	FBOUT	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
5	1	29,30	DDRT/C5	1 = output enabled (running). 0 = output disabled asynchronously in a low state.

Byte 5: SDR/DDR Clock Register (continued)

Bit	@Pup	Pin#	Name	Description
4	1	31,32	DDRT/C4	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
3	1	35,36	DDRT/C3	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
2	1	37,38	DDRT/C2	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
1	1	41,42	DDRT/C1	1 = output enabled (running). 0 = output disabled asynchronously in a low state.
0	1	43,44	DDRT/C0	1 = output enabled (running). 0 = output disabled asynchronously in a low state.

Byte 6: Watchdog Register

Bit	@Pup	Pin#	Name	Description
7	0	26	SRESET#	1 = Pin 26 is the input pin as PD# signal. 0 = Pin 26 is the output pin as SRESET# signal.
6	0		Frequency Revert	This bit allows setting the Revert Frequency once the system is rebooted due to Watchdog time out only. 0 = select frequency of existing H/W setting, 1 = select frequency of the second to last S/W table setting. (the software setting prior to the one that caused a system reboot).
5	0		WDTEST	For IMI Test - WD-Test, ALWAYS program to '0'
4	0		WD Alarm	This bit is set to “1” when the Watchdog times out. It is reset to “0” when the system clears the WD time stamps (WD3:0).
3	0		WD3	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 7*
2	0		WD2	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 7*
1	0		WD1	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 7*
0	0		WD0	This bit allows the selection of the time stamp for the Watchdog timer. See *Table 7*

Table 7. Watchdog Time Stamp

WD3	WD2	WD1	WD0	FUNCTION
0	0	0	0	Off
0	0	0	1	1 second
0	0	1	0	2 seconds
0	0	1	1	3 seconds
0	1	0	0	4 seconds
0	1	0	1	5 seconds
0	1	1	0	6 seconds
0	1	1	1	7 seconds
1	0	0	0	8 seconds
1	0	0	1	9 seconds
1	0	1	0	10 seconds
1	0	1	1	11 seconds
1	1	0	0	12 seconds
1	1	0	1	13 seconds
1	1	1	0	14 seconds
1	1	1	1	15 seconds

Byte 7: Dial-a-Frequency Control Register N

Bit	@Pup	Pin#	Name	Description
7	0		Reserved	Reserved for device function test.
6	0		N6, MSB	These bits are for programming the PLL's internal N register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0		N5	
4	0		N4	
3	0		N3	
2	0		N2	
1	0		N3	
0	0		N0, LSB	

Byte 8: Silicon Signature Register (all bits are read-only)

Bit	@Pup	Pin#	Name	Description
7	0		Revision_ID3	Revision ID bit [3]
6	0		Revision_ID2	Revision ID bit [2]
5	0		Revision_ID1	Revision ID bit [1]
4	0		Revision_ID0	Revision ID bit [0]
3	1		Vendor_ID3	Cypress's Vendor ID bit [3].
2	0		Vendor_ID2	Cypress's Vendor ID bit [2].
1	0		Vendor_ID1	Cypress's Vendor ID bit [1].
0	0		Vendor_ID0	Cypress's Vendor ID bit [0].

Byte9: Dial-A-Frequency Control Register R

Bit	@Pup	Pin#	Name	Description
7	0		Reserved	Reserved
6	0		R5, MSB	These bits are for programming the PLL's internal R register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0		R4	
4	0		R3	
3	0		R2	
2	0		R1	
1	0		R0	
0	0		DAF_ENB	R and N register mux selection. 0 = R and N values come from the ROM. 1 = data is load from DAF (SMBus) registers.

Dial-A-Frequency Feature

SMBus Dial-a-Frequency feature is available in this device via Byte7 and Byte9.

P is a PLL constant that depends on the frequency selection prior to accessing the Dial-a-Frequency feature.

Table 8.

FS(4:0)	P
XXXXX	96016000

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is enabled/disabled via SMBus register Byte 1, Bit 7.

Table 9. Spread Spectrum Table

Mode	SST1	SST0	% Spread
0	0	0	–1.5%
0	0	1	–1.0%
0	1	0	–0.7%
0	1	1	–0.5%
1	0	0	±0.75%
1	0	1	±0.5%
1	1	0	±0.35%
1	1	1	±0.25%

Swing Select Functions Through Hardware

MULTSEL	Board Target Trace/Term Z	Reference R, IREF = VDD/(3*Rr)	Output Current	VOH@Z
1	50 Ohm	Rr = 475 1%, IREF = 2.32mA	IOH = 6* Iref	0.7V@50

Watchdog Self-Recovery Sequence

This feature is designed to allow the system designer to change frequency while the system is running and reboot the operation of the system in case of a hang-up due to the frequency change.

When the system sends an SMBus command requesting a frequency change through the Dial-a-Frequency Control Registers, it must have previously sent a command to the Watchdog timer to select which time-out stamp the Watchdog must perform, otherwise the System Self-Recovery feature will not be applicable. Consequently, this device will change frequency and then the Watchdog timer starts timing. Meanwhile, the system BIOS is running its operation with the new frequency. If this device receives a new SMBus command to clear the bits originally programmed in the Watchdog timer bits (reprogram to 0000) before the Watchdog times out, then this device will keep operating in its normal condition with the new selected frequency.

The Watchdog timer will also be triggered if you program the software frequency select bits (FSEL) to a new frequency selection. If the Watchdog times out before the new SMBus reprograms the Watchdog timer bits to (0000), then this device send a low system reset pulse, on SRESET# and changes Watchdog time-out bit to “1”.

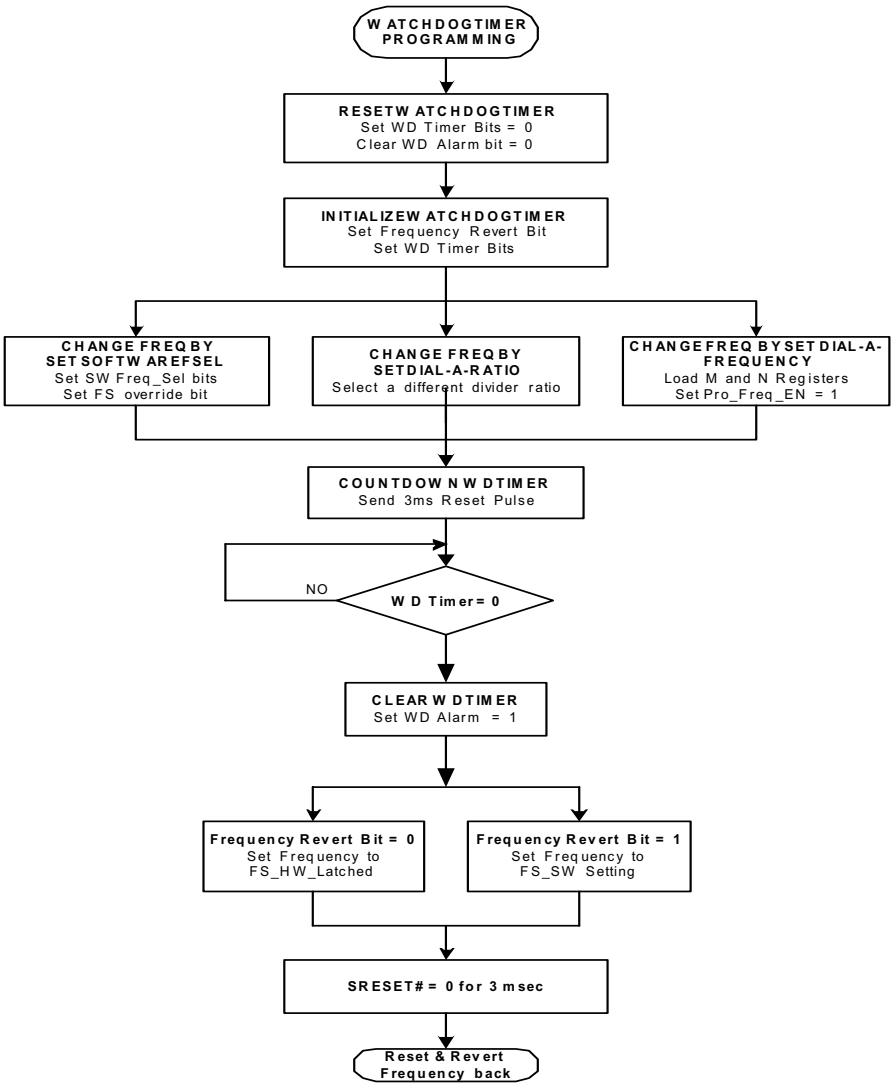


Figure 1. Watchdog Self Recovery Sequence Flowchart

P4 Processor SELP4_K7# = 1

Power-down Assertion (P4 Mode)

When PD# is sampled low by two consecutive rising edges of CPU# clock then all clock outputs except CPU clocks must be held low on their next high to low transition. CPU clocks must be held with the CPU clock pin driven high with a value of 2 x Iref, and CPU# undriven. Note that *Figure 1* shows CPU = 133 MHz. This diagram and description are applicable for all valid CPU frequencies 66, 100, 133, 200 MHz. Due to the state of internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.

Power-down Deassertion (P4 Mode)

The power-up latency needs to be less than 3 mS.

AMD K7 processor SELP4_K7# = 0

Power-down Assertion (K7 Mode)

When the PD# signal is asserted low, all clocks are disabled to a low level in an orderly fashion prior to removing power from the part. When PD# is asserted (forced) low, the device transitions to a shutdown (power down) mode and all power supplies may then be removed. When PD# is sampled low by two consecutive rising edges of CPU clock, then all affected clocks are stopped in a low state as soon as possible. When in power down (and before power is removed), all outputs are synchronously stopped in a low state (see *Figure 3* below), all PLL's are shut off, and the crystal oscillator is disabled. When the device is shutdown, the I2C function is also disabled.

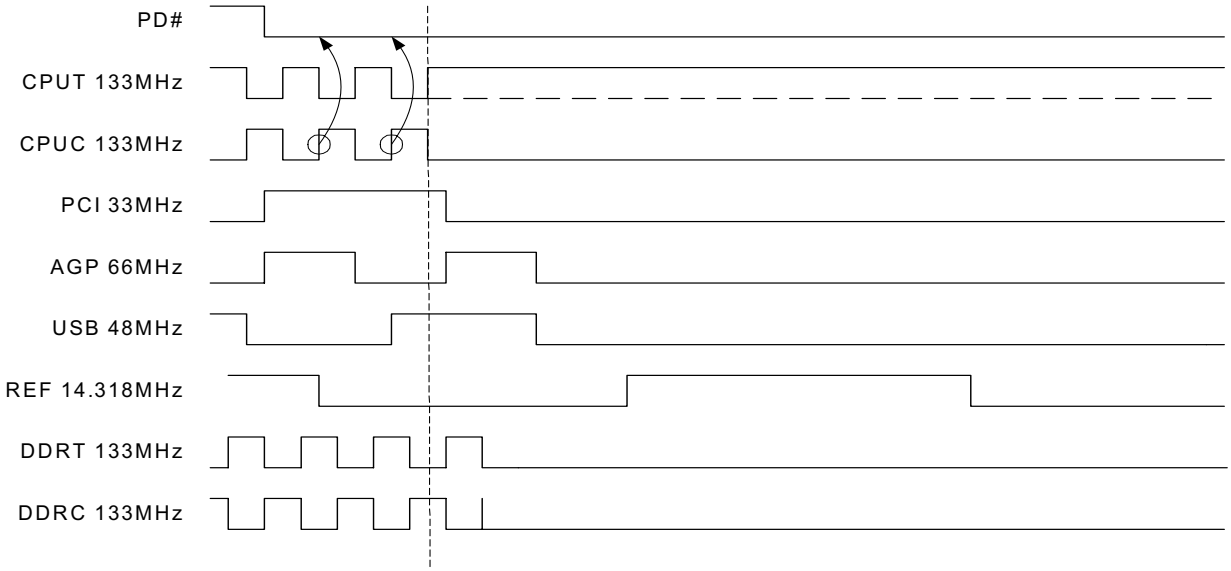


Figure 2. Power-down Assertion Timing Waveform (in P4 Mode)

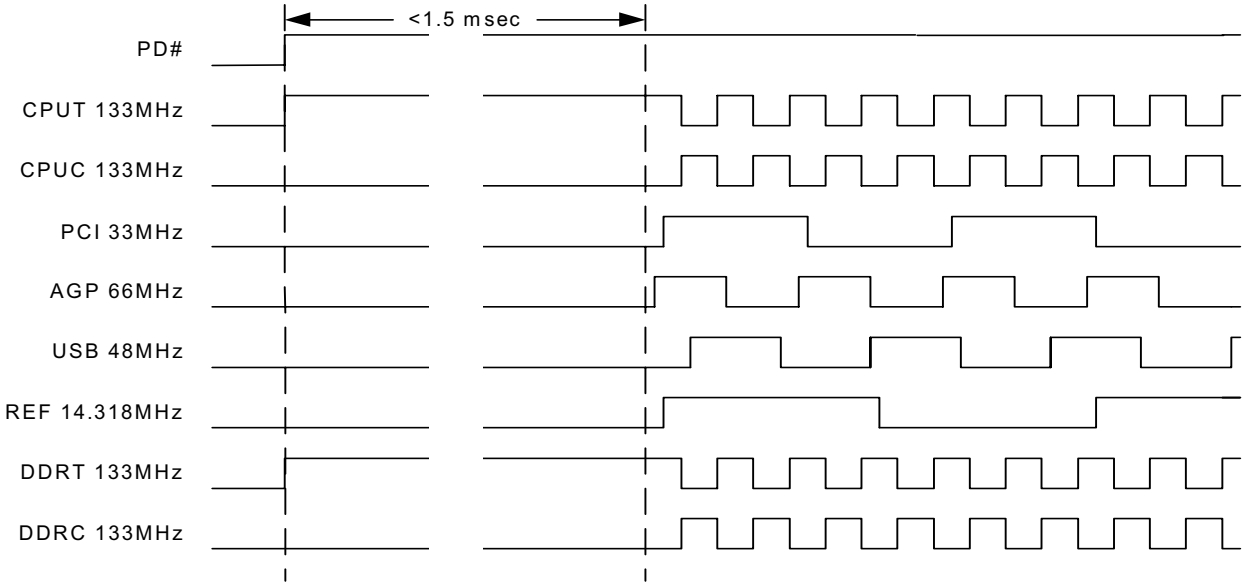


Figure 3. Power-down Deassertion Timing Waveform (in P4 mode)

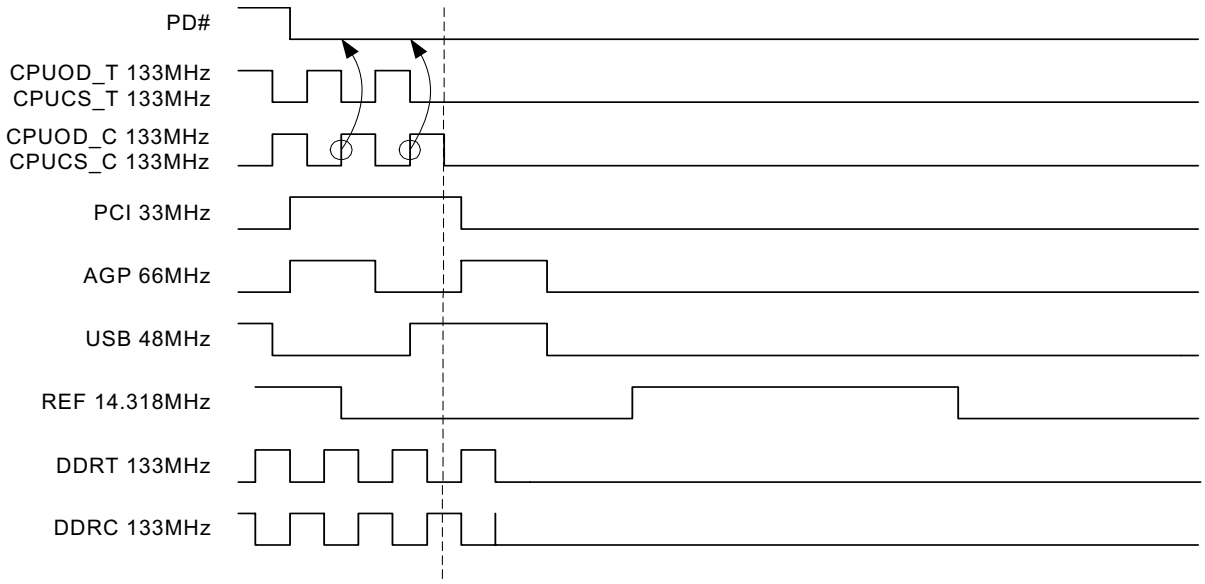


Figure 4. Power-down Assertion Timing Waveform (In K7 Mode)

Power-down Deassertion (K7 Mode)

When deasserted PD# to high level, all clocks are enabled and start running on the rising edge of the next full period in order to guarantee a glitch free operation, no partial clock pulses.

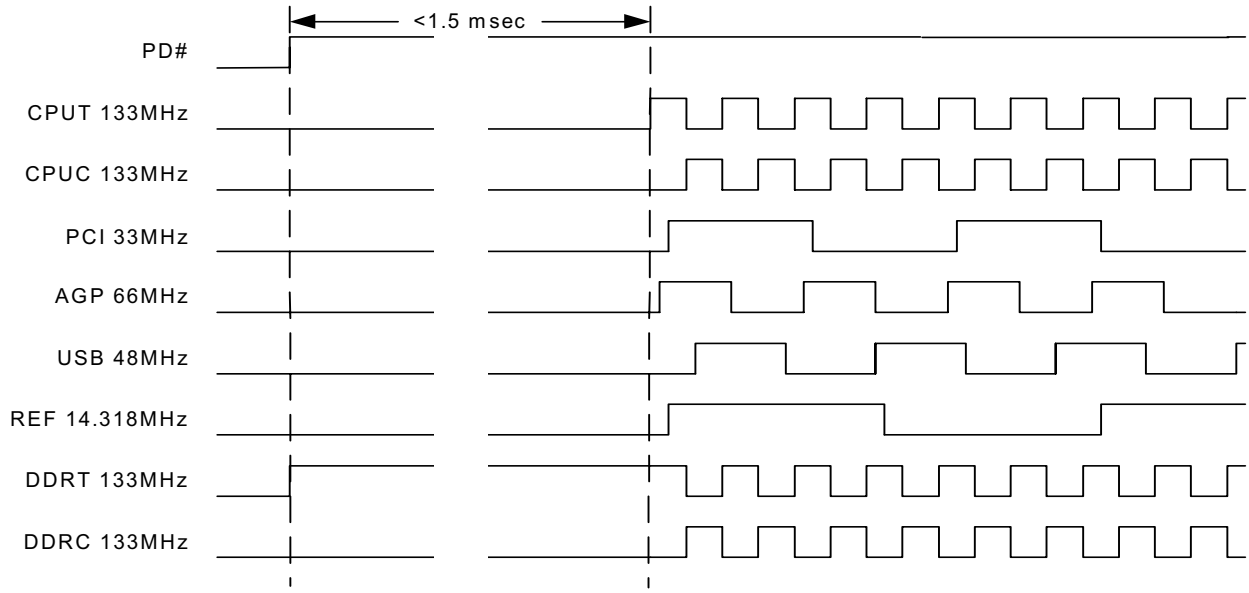


Figure 5. Power-down Deassertion Timing Waveform (in K7 Mode)

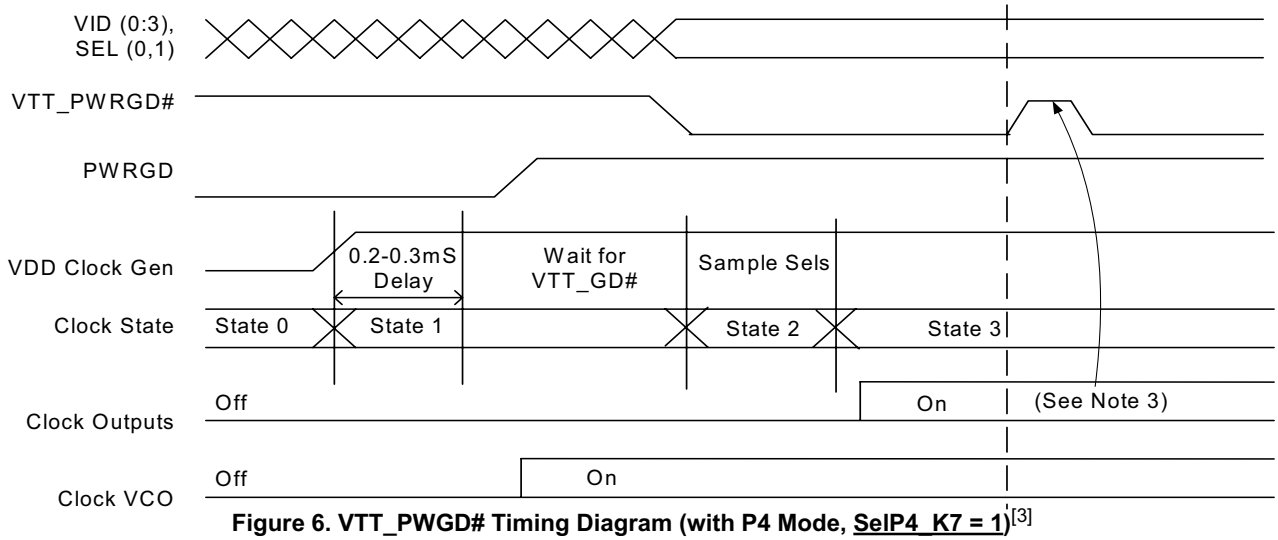


Figure 6. VTT_PWGD# Timing Diagram (with P4 Mode, SelP4_K7 = 1)[3]

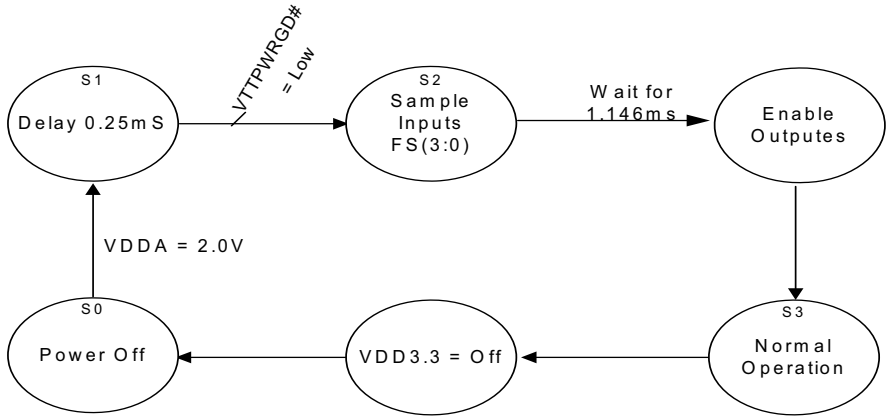


Figure 7. Clock Generator Power-up/Run State Diagram (with P4 Processor SELP4_K7#=1)

Connection Circuit DDRT/C Signals

For open-drain CPU output signals (with K7 processor SELP4_K7#=0)

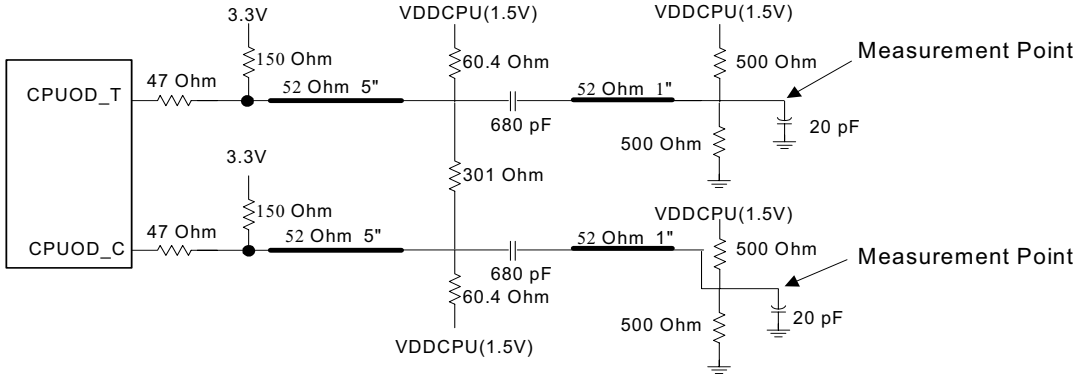


Figure 8. K7 Load Termination

Note:
3. This time diagram shows that VTT_PWRGD# transits to a logic low in the first time at power-up. After the first high-to-low transition of VTT_PWRGD#, device is not affected, VTT_PWRGD# is ignored.

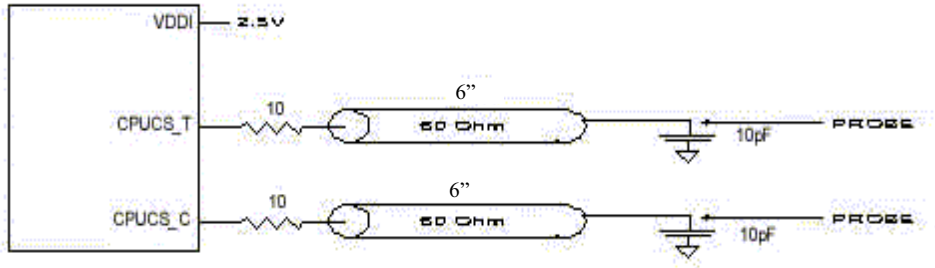


Figure 9. CS Load Termination

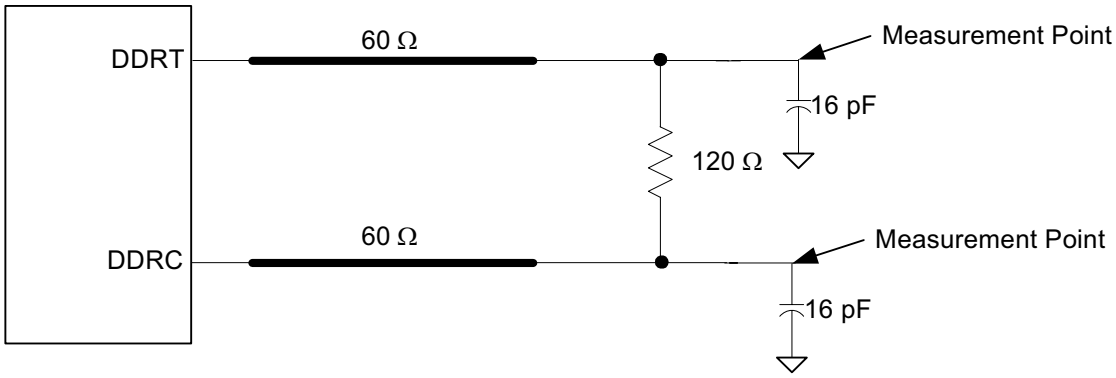


Figure 10. DDR Termination

Table 10.Signal Loading Table

Clock Name	Max Load (pF)
REF, 48MHz (USB), 24_48MHz	20
AGP	30
PCI_F	30
DDRT/C, FBOUT	16
CPUT/C	*See Figure 11*
CPUOD_T/C	*See Figure 8*
CPUCS_T/C	*See Figure 9*

For Differential CPU Output Signals (with P4 Processor SELP4_K7= 1)

The following diagram shows lumped test load configurations for the differential Host Clock outputs.

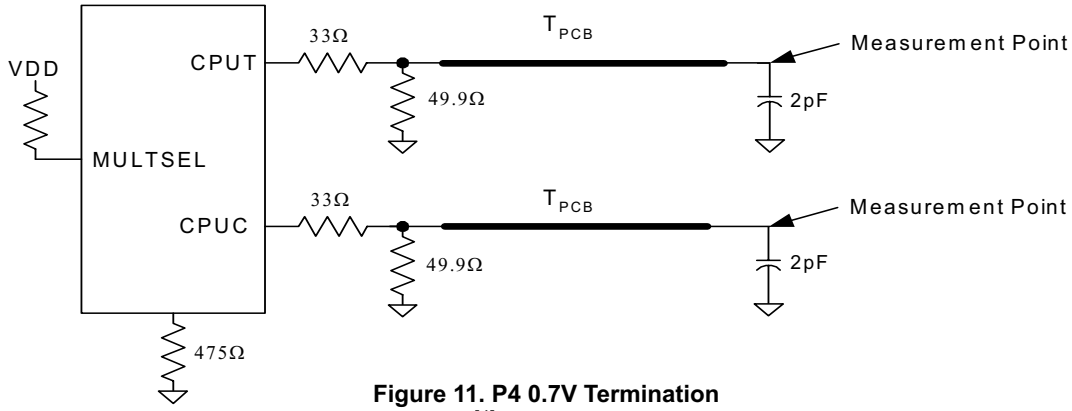


Figure 11. P4 0.7V Termination

Table 11.Group Timing Relationships and Tolerances[4]

		Offset (ps)	Tolerance (ps)	Conditions
t_{CSAGP}	CPUCS to AGP	750	500	CPUCS Leads
t_{AP}	AGP to PCI	1,250	500	AGP Leads

Note:

4. Ideally the probes should be placed on the pins. If there is a transmission line between the test point and the pin for one signal of the pair (e.g., CPU), the same length of transmission line should be added to the other signal of the pair (e.g., AGP).

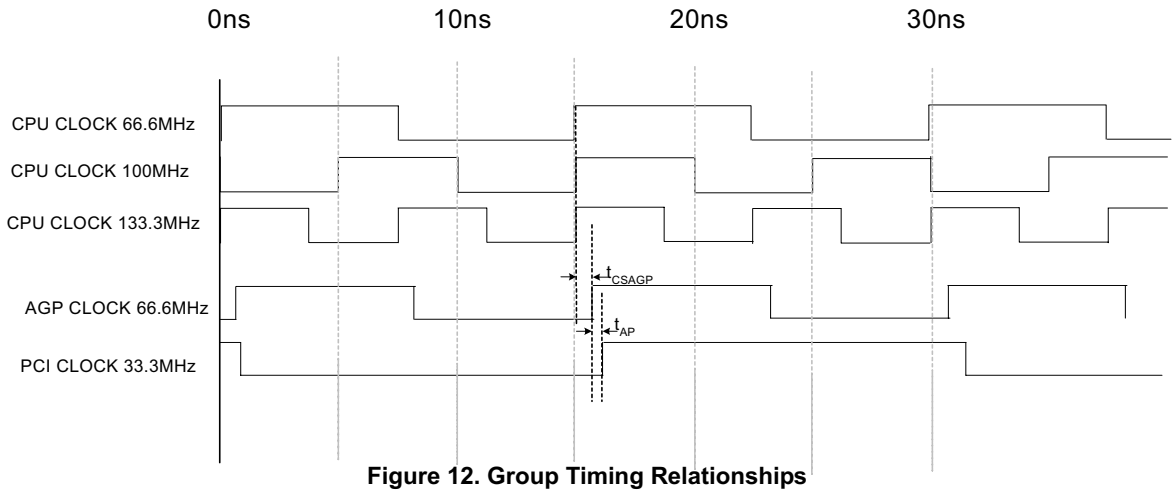


Figure 12. Group Timing Relationships

Absolute Maximum Conditions

Parameter	Description	Condition		Min.	Max.	Unit
V_{DD}	Core Supply Voltage			–0.5	4.6	V
V_{DDA}	Analog Supply Voltage			–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}		–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional		–65	+150	°C
T_A	Temperature, Operating Ambient	Functional		0	70	°C
T_J	Temperature, Junction	Functional		–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015		2000	–	V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-STD 883E, Method 1012.1	TSSOP	20.92		°C/W
			SSOP	38.62		
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	TSSOP	75.18		
			SSOP	69.97		
UL–94	Flammability Rating	At 1/8 in.		V–0		
MSL	Moisture Sensitivity Level			1		

Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power-supply sequencing is NOT required.

DC Electrical Specifications (V_{DD}=V_{DDPCI}=V_{DDAGP}=V_{DDR}=V_{DD48M}=V_{DDC}= 3.3v±5%, V_{DDI} = V_{DD}=2.5±5%, T_A=0°C TO +70°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL1}	Input Low Voltage	Applicable to PD#, F S(0:4)	–	–	0.8	Vdc
V_{IH1}	Input High Voltage		2.0	–	–	Vdc
V_{IL2}	Input Low Voltage	Applicable to SDATA and SCLK	–	–	1.0	Vdc
V_{IH2}	Input High Voltage		2.2	–	–	Vdc
V_{OL}	Output Low Voltage for SRESET#	I_{OL}	0.4	–	–	V
L_{OL}	Pull-down current for SRESET#	V_{OL} = 0.4V	24	35	–	mA
I_{OZ}	Three-state leakage Current		–	–	10	µA
Idd3.3V	Dynamic Supply Current	CPU frequency set at 133.3 MHz, *Note 5*	–	150	190	mA
Idd2.5V	Dynamic Supply Current	CPU frequency set at 133.3 MHz, *Note 5*	–	175	195	mA
I_{PD}	Power Down Supply current	PD# = 0	–	95	600	µA
I_{PUP}	Internal Pull-up Device Current	Input @ V_{SS}	–	–	–25	µA
I_{PDWN}	Internal Pull-down Device Current	Input @ V_{DD}	–	–	10	µA
C_{IN}	Input pin capacitance		–	–	5	pF
C_{OUT}	Output pin capacitance		–	–	6	pF
L_{PIN}	Pin Inductance		–	–	7	pF
C_{XTAL}	Crystal pin capacitance	Measured from the Xin or Xout to V_{SS}	27	36	45	pF

AC Parameters

Parameter	Description	100 MHz		133MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max	Min.	Max.		
XTAL									
T_{DC}	Xin Duty Cycle	45	55	45	55	45	55	%	6,17
T_{PERIOD}	Xin Period	69.841	71.0	69.84	71.0	69.84	71.0	ns	6,17
V_{HIGH}	Xin High Voltage	.7V_{DD}	V_{DD}	.7V_{DD}	V_{DD}	.7V_{DD}	V_{DD}	V	15
V_{LOW}	Xin Low Voltage	0	.3V_{DD}	0	.3V_{DD}	0	.3V_{DD}	V	15
T_R/T_F	Xin Rise and Fall Times	–	10.0	–	10	–	10	ns	16
T_{CCJ}	Xin Cycle to Cycle Jitter	–	500	–	500	–	500	ps	7,14
Txs	Crystal Start-up Time		30		30		30	ms	13,15

AC Parameters (continued)

Parameter	Description	100 MHz		133MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max	Min.	Max.		
P4 Mode CPU at 0.7V									
T_{DC}	CPUT/C Duty Cycle	45	55	45	55	45	55	%	6,7,9,20,23
T_{PERIOD}	CPUT/C Period	9.997	10.003	7.4978	7.5023	4.9985	5.0015	ns	6,7,9,20,23
T_R/T_F	CPUT/C Rise and Fall Times	175	1300	175	1300	175	1300	ps	22
	Rise/Fall Matching	–	20%	–	20%	–	20%		22,25
$\Delta T_R/T_F$	Rise/Fall Time Variation	–	125	–	125	–	125	ps	7,22,23
T_{SKEW}	CPUCS_T/C to CPUT/C Clock Skew	–	100	–	100	–	100	ps	7,10,20,23
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	–	250	–	250	–	250	ps	7,10,20,23
V_{CROSS}	Crossing Point Voltage at 0.7V Swing	250	550	250	550	250	550	mV	23
K7 Mode									
T_{DC}	CPUOD_T/C Duty Cycle	45	55	45	55	45	55	%	7,9
T_{PERIOD}	CPUOD_T/C Period	9.997	10.003	7.4978	7.5023	4.9985	5.0015	ns	7,9
T_{LOW}	CPUOD_T/C Low Time	2.8	–	1.67	–	2.8	–	ns	7,9
T_F	CPUOD_T/C Fall Time	0.4	1.6	0.4	1.6	0.4	1.6	ns	7,8
T_{SKEW}	CPUCS_T/C to CPUODT/C Clock Skew	–	100	–	100	–	100	0	7,10,20
T_{CCJ}	CPUOD_T/C Cycle-to-Cycle Jitter	–	150	–	150	–	150	ps	7,9
V_{DIFF}	Differential Voltage AC	.4	Vp+.6V	.4	Vp+.6V	.4	Vp+.6V	V	19
V_{CROSS}	Differential Crossover Voltage	$0.5*V_{DDC}-0.1$	$0.5*V_{DDC}+0.1$	$0.5*V_{DDC}-0.1$	$0.5*V_{DDC}+0.1$	$0.5*V_{DDC}-0.1$	$0.5*V_{DDC}+0.1$	mV	18
CHIPSET CLOCK									
T_{DC}	CPUCS_T/C Duty Cycle	40	60	40	60	40	60	%	6,7,9
T_{PERIOD}	CPUCS_T/C Period	9.997	10.003	7.4978	7.5023	4.9985	5.0015	ns	6,7,9
T_R / T_F	CPUCS_T/C Rise and Fall Times	0.4	1.6	0.4	1.6	0.4	1.6	ns	6,7,8
V_{DIFF}	Differential Voltage AC	.4	Vp+.6V	.4	Vp+.6V	.4	Vp+.6V	V	21
V_{CROSS}	Differential Crossover Voltage	$0.5*V_{DDI}-0.8$	$0.5*V_{DDI}+0.8$	$0.5*V_{DDI}-0.8$	$0.5*V_{DDI}+0.8$	$0.5*V_{DDI}-0.8$	$0.5*V_{DDI}+0.8$	V	20
AGP									
T_{DC}	AGP Duty Cycle	45	55	45	55	45	55	%	6,7,9
T_{PERIOD}	AGP Period	15	15.3	15	15.3	15	15.3	ns	6,7,9
T_{HIGH}	AGP High Time	4.95	–	4.95	–	4.95	–	ns	7,11
T_{LOW}	AGP Low Time	4.55	–	4.55	–	4.55	–	ns	7,12
T_R / T_F	AGP Rise and Fall Times	0.5	2.0	0.5	2.0	0.5	2.0	ns	7,8
T_{SKEW}	Any AGP to Any AGP Clock Skew	–	250	–	250	–	250	ps	7,10
T_{CCJ}	AGP Cycle-to-Cycle Jitter	–	500	–	500	–	500	ps	7,9,10
PCI									
T_{DC}	PCI_F Duty Cycle	45	55	45	55	45	55	%	6,7,9
T_{PERIOD}	PCI_F Period	30.0	–	30.0	–	30.0	–	ns	6,7,9
T_{HIGH}	PCI_F High Time	12.0	–	12.0	–	12.0	–	ns	7,11
T_{LOW}	PCI_F Low Time	12.0	–	12.0	–	12.0	–	ns	7,12
T_R / T_F	PCI_F Rise and Fall Times	0.5	2.0	0.5	2.0	0.5	2.0	ns	7,27
T_{SKEW}	Any PCI to Any PCI Clock Skew	–	500	–	500	–	500	ps	7,10
T_{CCJ}	PCI_F Cycle-to-Cycle Jitter	–	500	–	500	–	500	ps	7,9,10
48 MHz									
T_{DC}	48-MHz Duty Cycle	45	55	45	55	45	55	%	6,7,9
T_{PERIOD}	48-MHz Period	20.8299	20.8333	20.8299	20.8333	20.8299	20.8333	ns	6,7,9
T_R / T_F	48-MHz Rise and Fall Times	1.0	2.0	1.0	2.0	1.0	2.0	ns	7,8
T_{CCJ}	48-MHz Cycle-to-Cycle Jitter	–	350	–	350	–	350	ps	7,9,10

AC Parameters (continued)

Parameter	Description	100 MHz		133MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max	Min.	Max.		
24 MHz									
T_{DC}	24-MHz Duty Cycle	45	55	45	55	45	55	%	6,7,9
T_{PERIOD}	24-MHz Period	41.660	41.667	41.660	41.667	41.660	41.667	ns	6,7,9
T_R / T_F	24-MHz Rise and Fall Times	1.0	4.0	1.0	4.0	1.0	4.0	ns	7,8
T_{CCJ}	24-MHz Cycle-to-Cycle Jitter	–	500	–	500	–	500	ps	7,9,10
REF									
T_{DC}	REF Duty Cycle	45	55	45	55	45	55	%	6,7,9
T_{PERIOD}	REF Period	69.8413	71.0	69.8413	71.0	69.8413	71.0	ns	6,7,9
T_R / T_F	REF Rise and Fall Times	1.0	4.0	1.0	4.0	1.0	4.0	ns	7,8
T_{CCJ}	REF Cycle-to-Cycle Jitter	–	1000	–	1000	–	1000	ps	7,9,10
DDR									
V_X	Crossing Point Voltage of DDRT/C	$0.5*V_{DDD}$–0.2	$0.5*V_{DDD}$+0.2	$0.5*V_{DDD}$–0.2	$0.5*V_{DDD}$+0.2	$0.5*V_{DDD}$–0.2	$0.5*V_{DDD}$+0.2	V	18
V_D	Differential Voltage Swing	0.7	V_{DDD} + 0.6	0.7	V_{DDD} + 0.6	0.7	V_{DDD} + 0.6	V	19
T_{DC}	DDRT/C(0:5) Duty Cycle	45	55	45	55	45	55	%	20
T_{PERIOD}	DDRT/C(0:5) Period	9.997	10.003	7.4978	7.5023	4.9985	5.0015	ns	20
T_R/T_F	DDRT/C(0:5) Rise/Fall Slew Rate	1	3	1	3	1	3	V/ns	8
T_{SKEW}	DDRT/C to any DDRT/C Clock Skew	–	100	–	100	–	100	ps	7,10,20
T_{CCJ}	DDRT/C(0:5) Cycle-to-Cycle Jitter	–	±150	–	±150	–	±150	ps	7,10,20
T_{HPJ}	DDRT/C(0:5) Half-period Jitter	–	±100	–	±100	–	±100	ps	7,10,20
T_{DELAY}	BUF_IN to Any DDRT/C Delay	1	4	1	4	1	4	ns	7,9
T_{SKEW}	FBOUT to Any DDRT/C Skew	–	100	–	100	–	100	ps	7,9
T_{STABLE}	All-Clock Stabilization from Power-up	–	3	–	3	–	3	ms	13

Notes:

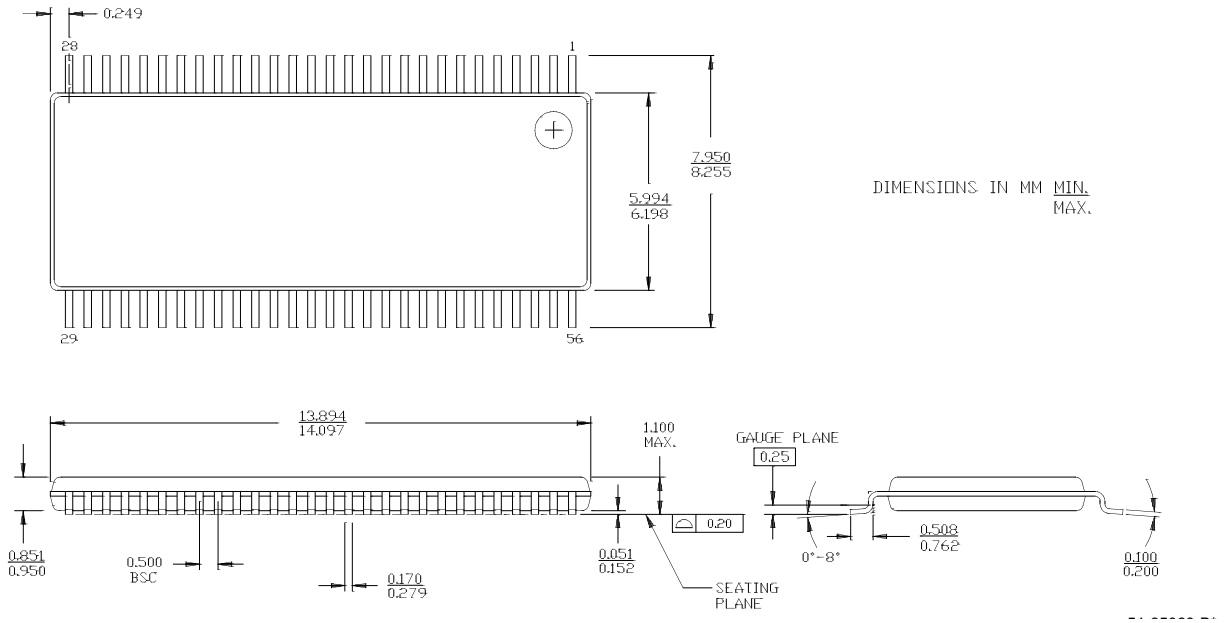
5. All outputs loaded as per maximum capacitive load table.
6. This parameter is measured as an average over a 1-us duration, with a crystal center frequency of 14.31818 MHz.
7. All outputs loaded as per loading specified in *Table 11*.
8. Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V signals and between 20% and 80% for differential signals.
9. Probes are placed on the pins, and measurements are acquired at 1.5V for 3.3V signals and at 1.25V for 2.5V and 50% point for differential signals.
10. This measurement is applicable with Spread ON or spread OFF.
11. Probes are placed on the pins, and measurements are acquired at 2.4V for 3.3V signals and at 2.0V for 2.5V signals).
12. Probes are placed on the pins, and measurements are acquired at 0.4V.
13. The time specified is measured from when all VDDs reach their respective supply rail (3.3V and 2.5V) till the frequency output is stable and operating within the specifications.
14. When Xin is driven from and external clock source (3.3V parameters apply).
15. When crystal meets minimum 40-ohm device series resistance specification.
16. Measured between $0.2V_{DD}$ and $0.7V_{DD}$.
17. This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
18. The typical value of VX is expected to be $0.5*V_{DDD}$ (or $0.5*V_{DDC}$ for CPUCS signals) and will track the variations in the DC level of the same.
19. VD is the magnitude of the difference between the measured voltage level on a DDRT (and CPUCS_T) clock and the measured voltage level on its complementary DDRC (and CPUCS_C) one.
20. Measured at VX, or where subtraction of CLK-CLK# crosses 0V.
21. Measured at VX between the rising edge and the following falling edge of the signal.
22. Measured from Vol = 0.175V to Voh = 0.525V.
23. See *Figure 11* for 0.7V loading specification.
24. Measurement taken from differential waveform, from –0.35V to +0.35V.
25. Measurements taken from common mode waveforms, measure rise/fall time from 0.41V to 0.86V. Rise/fall time matching is defined as “the instantaneous difference between maximum clk rise (fall) and minimum clk# fall (rise) time, or minimum clk rise (fall) and maximum clk# fall (rise) time”. This parameter is designed for waveform symmetry.
26. Measured in absolute voltage, i.e., single-ended measurement.
27. Probes are placed on the pins, and measurements are acquired between 0.8V and 2.0V signals and between 20% and 80% for differential signals.

Ordering Information

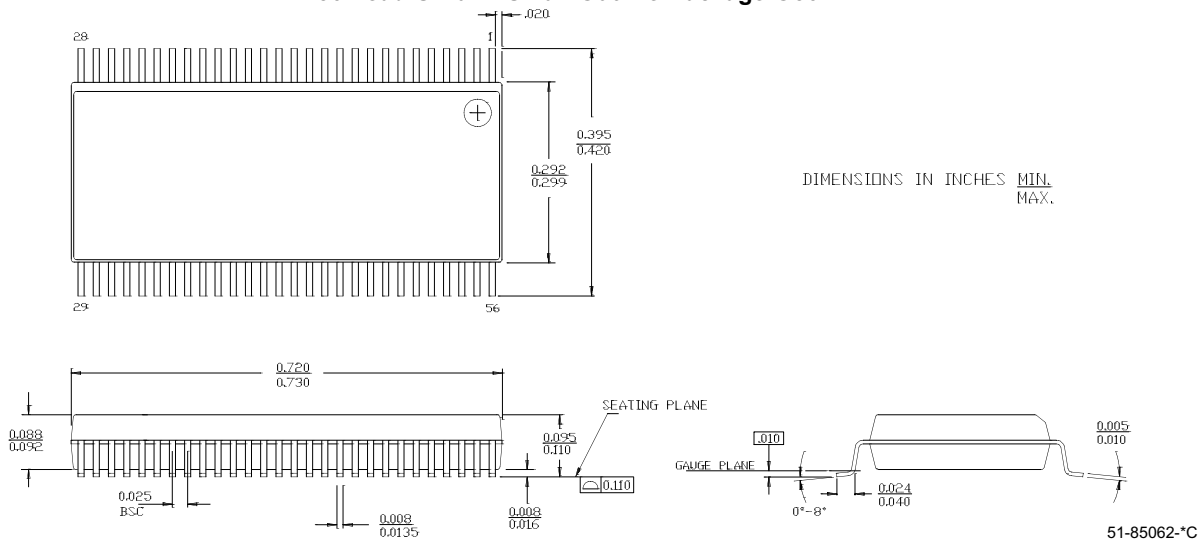
Part Number	Package Type	Product Flow
CY28341OC–3	56-pin Shrunk Small Outline package (SSOP)	Commercial, 0° to 70°C
CY28341OC–3T	56-pin Shrunk Small Outline package (SSOP)–Tape and Reel	Commercial, 0° to 70°C
CY28341ZC–3	56-pin Thin Shrunk Small Outline package(TSSOP)	Commercial, 0° to 70°C
CY28341ZC–3T	56-pin Thin Shrunk Small Outline package(TSSOP)–Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

56-pin Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



56-Lead Shrunk Small Outline Package O56



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