2.5-W Stereo Audio Power Amplifier with Advanced DC Volume Control

DESCRIPTOIN

The EUA6021A is a stereo audio power amplifier that drives 2.5 W/channel of continuous RMS power into a 4-Ω load. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control.

The 20-pin DIP package allows for the use of a heatsink which provides higher output power.

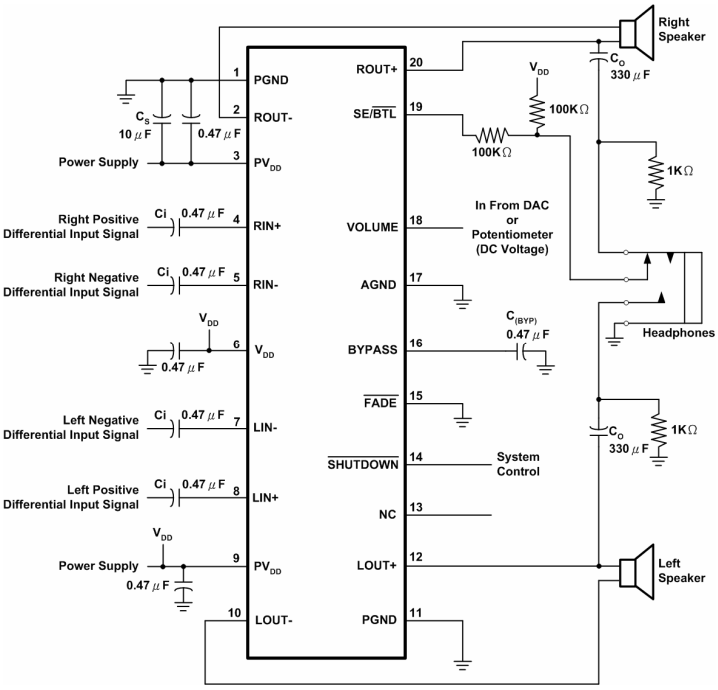
To ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

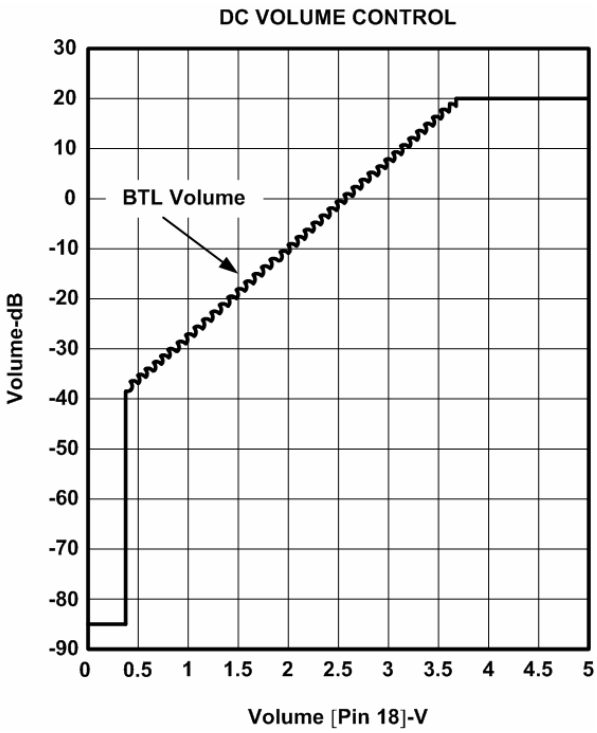
FEATURES

- 2.5 W into 4-Ω Speakers With External Heatsink
- DC Volume Control with 2-dB
  Step from -40dB to 20dB
  -Fade Mode
  - -85-dB Mute Mode
- Differential Inputs
- 1 μ A Shutdown Current (Typical)
- Headphone Mode
- RoHS Compliant and 100% Lead (Pb)-Free

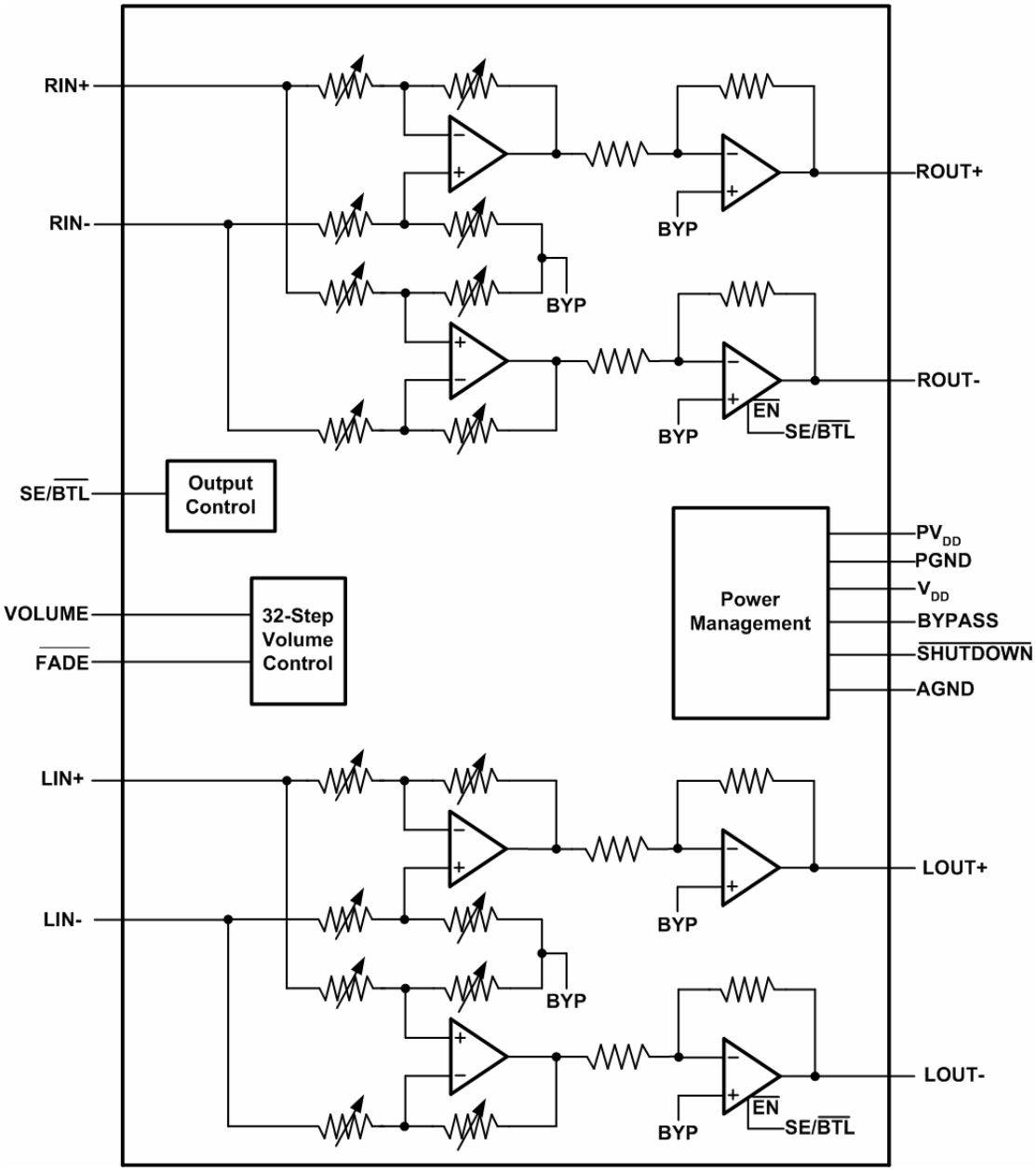
APPLICATIONS

- LCD Monitors





Block Diagram



Typical Application Circuit

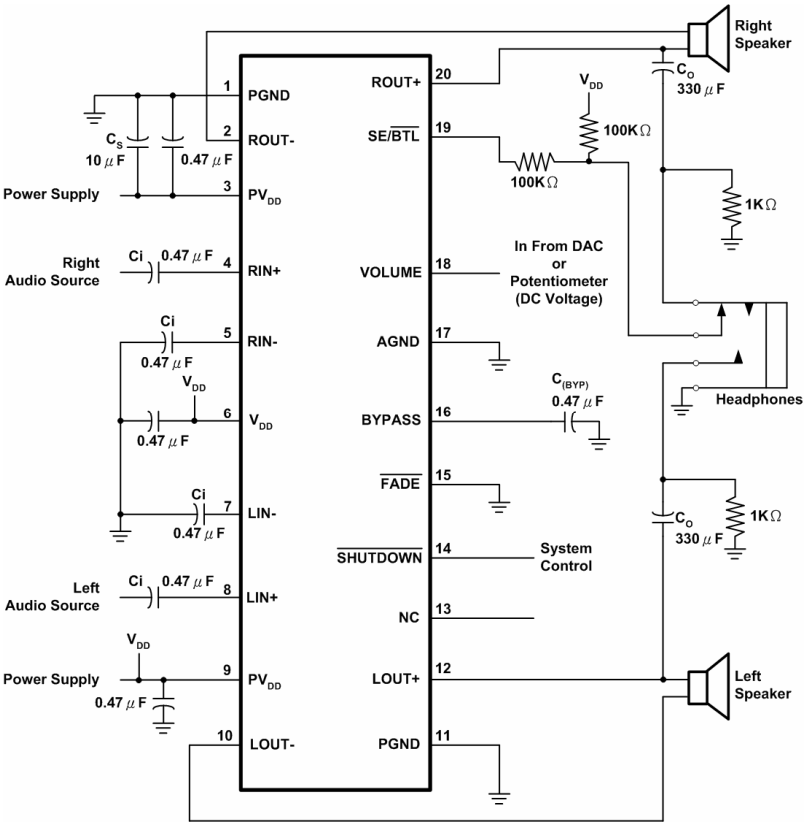


Figure 1. Application circuit using single-ended inputs and input MUX

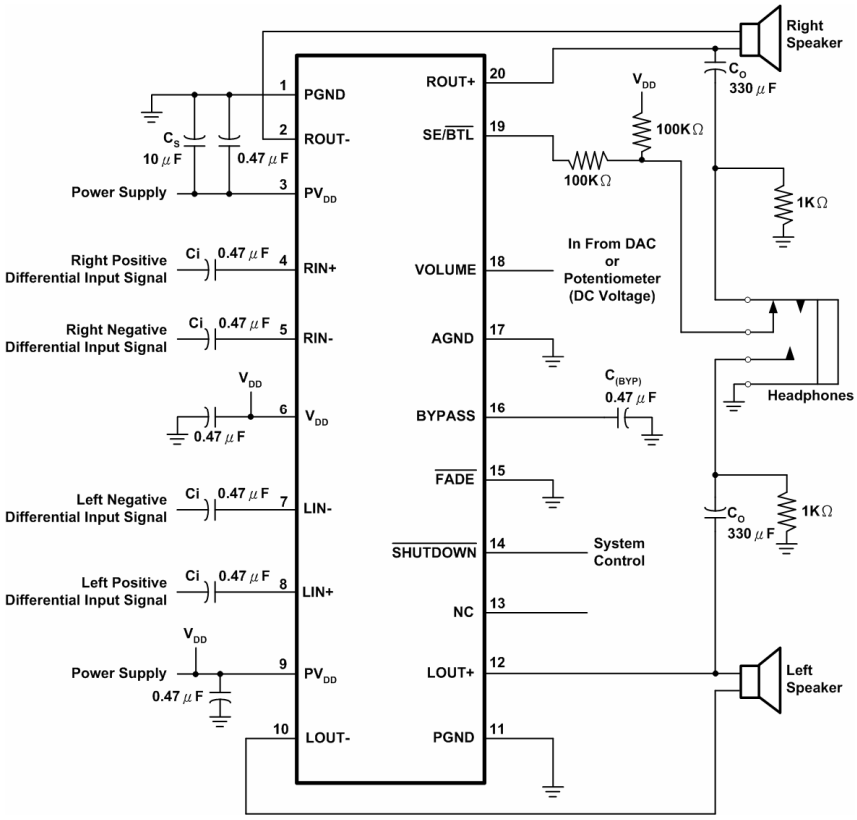
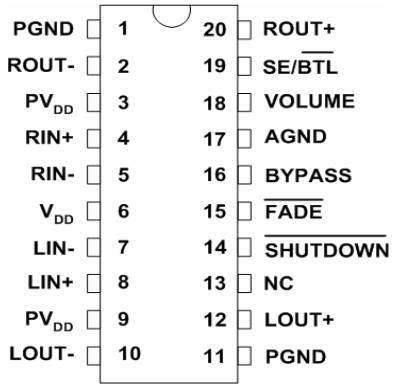


Figure 2. Application circuit using differential inputs

Pin Configurations

Package	Pin Configurations(Top View)
DIP-20	

Pin Description

PIN	PIN	I/O	DESCRIPTION
BYPASS	16	I	Tap to voltage divider for internal midsupply bias generator used for analog reference
$\overline{\text{FADE}}$	15	I	Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic high is placed on this terminal.
AGND	17	-	Analog power supply ground
LIN-	7	I	Left channel negative input for fully differential input.
LIN+	8	I	Left channel positive input for fully differential input.
LOUT-	10	O	Left channel negative audio output.
LOUT+	12	O	Left channel positive audio output.
NC	13	-	No connection
PGND	1,11	-	Power ground
PV_{DD}	3,9	-	Supply voltage terminal for power stage
RIN-	5	I	Right channel negative input for fully differential input.
RIN+	4	I	Right channel positive input for fully differential input.
ROUT-	2	O	Right channel negative audio output
ROUT+	20	O	Right channel positive audio output
SE/$\overline{\text{BTL}}$	19	I	Output control. When this terminal is high, SE outputs are selected. When this terminal is low, BTL outputs are selected.
$\overline{\text{SHUTDOWN}}$	14	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal
V_{DD}	6	-	Supply voltage terminal
VOLUME	18	I	Terminal for dc volume control. DC voltage range is 0 to V_{DD}.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUA6021AIIT1	DIP-20	xxxxx A6021AA	-40 °C to 85°C

EUA6021A □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
T: Tube

Operating temperature range
I: Industry Standard

Package Type
I: DIP

Absolute Maximum Ratings

- Supply voltage, V_{DD} ---------- 6V
- Input voltage, V_I ---------- –0.3 V to V_{DD} +0.3 V
- Continuous total power dissipation ---------- internally limited
- Operating free-air temperature range, T_A ---------- –40°C to 85° C
- Operating junction temperature range, T_J ---------- –40°C to 150°C
- Storage temperature range, T_{stg} ---------- –65°C to 150°C
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Thermal Resistance

  θ_{JA} (DIP) ---------- 87.9°C/W

Recommended Operating Conditions

		Min	Max	Unit
Supply voltage, V_{DD}		4	5.5	V
High-level input voltage, V_{IH}	$SE/\overline{BTL}$, $\overline{FADE}$	$V_{DD} \times 0.8$		V
	$\overline{SHUTDOWN}$	2		
Low-level input voltage, V_{IL}	$SE/\overline{BTL}$, $\overline{FADE}$		$V_{DD} \times 0.6$	V
	$\overline{SHUTDOWN}$		0.8	
Operating free-air temperature, T_A		-40	85	°C

Electrical Characteristics at Specified Free-air Temperature, VDD = PVDD=5.5V, T_A = 25°C

Symbol	Parameter	Conditions	EUA6021A			Unit
			Min.	Typ.	Max.	
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	$V_{DD=}$ 5.5V,Gain=0 dB, $SE/\overline{BTL}$ =0V			30	mV
		$V_{DD=}$ 5.5V,Gain=20 dB, $SE/\overline{BTL}$ =0V			50	mV
PSRR	Power supply rejection ratio	V_{DD}= $PV_{DD=}$ 4 V to 5.5 V	-42	-70		dB
$\lvert I_{IH} \rvert$	High-level input current ($SE/\overline{BTL}$, $\overline{SHUTDOWN}$, $\overline{FADE}$, VOLUME,)	V_{DD}= $PV_{DD=}$5.5V, V_I= V_{DD} =PV_{DD}			1	µA
$\lvert I_{IL} \rvert$	Low-level input current	V_{DD}= $PV_{DD=}$5.5V, V_I= 0V			1	µA
I_{DD}	Supply current, no load	V_{DD}= $PV_{DD=}$5.5V, , $SE/\overline{BTL}$ =0V, $\overline{SHUTDOWN}$ =2V	6	7.5	9	mA
		V_{DD}= $PV_{DD=}$5.5V, , $SE/\overline{BTL}$ =5.5V $\overline{SHUTDOWN}$ =2V	3	5	6	
I_{DD}	Supply current, max power into a 3-Ω load	V_{DD}= $PV_{DD=}$5.5V, , $SE/\overline{BTL}$ =0V, $\overline{SHUTDOWN}$ =2V,R_L=3Ω, Po=2 W, stereo		1.5		A_{RMS}
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ =0V		1	20	µA

Operating Characteristics, VDD =PVDD= 5V, T_A = 25°C, R_L = 4Ω, Gain =6 dB

Symbol	Parameter	Conditions		EUA6021A			Unit
				Min.	Typ.	Max.	
P_O	Output power	THD=1%, f=1kHz			1.85		W
		THD=10%, f=1kHz,V_{DD}=5V			2.5		
THD+N	Total harmonic distortion plus noise	P_O=1W, R_L=8Ω,f=1 kHz			<0.4%		
V_{OH}	High-level output voltage	R_L =8Ω,Measured between output and V_{DD}				700	mV
V_{OL}	Low-level output voltage	R_L =8Ω,Measured between output and GND				400	mV
$V_{(Bypass)}$	Bypass voltage (Nominally V_{DD}/2)	Measured at pin 17,No load, V_{DD}=5.5V		2.65	2.75	2.85	V
B_{OM}	Maximum output power bandwidth	THD=5%			＞20		kHz
	Supply ripple rejection ratio	f =1kHz,Gain=0 dB $C_{(BYP)}$=0.47μF	BTL mode		-63		dB
			SE mode		-57		dB
	Noise output voltage	f=20 Hz to 20 kHz, Gain=0 dB, $C_{(BYP)}$=0.47μF,	BTL mode		36		μV_{RMS}
Z_I	Input impedance (see Figure 25)	VOLUME=5 V			14		kΩ

Typical Operating Characteristics

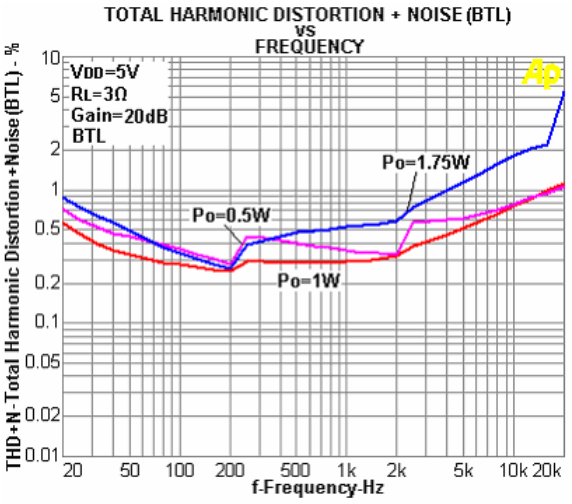


Figure 3

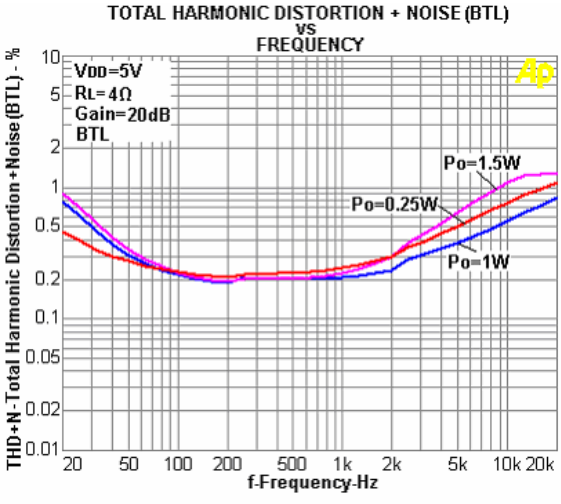


Figure 4

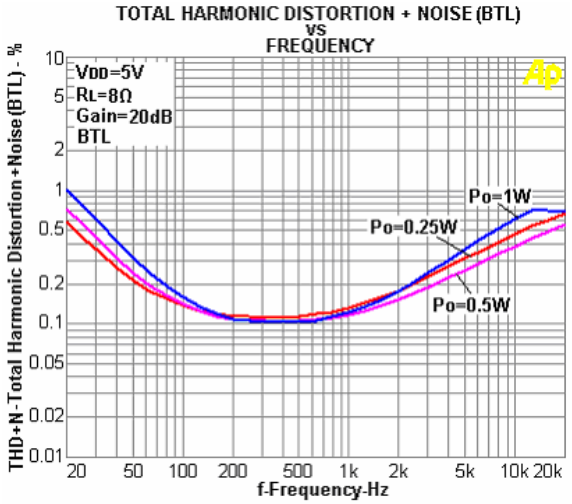


Figure 5

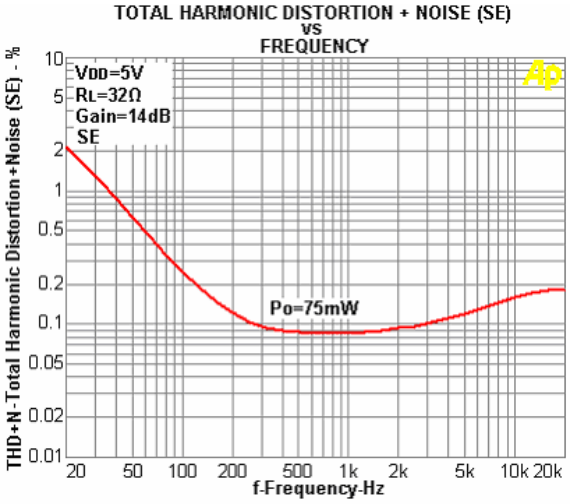


Figure 6

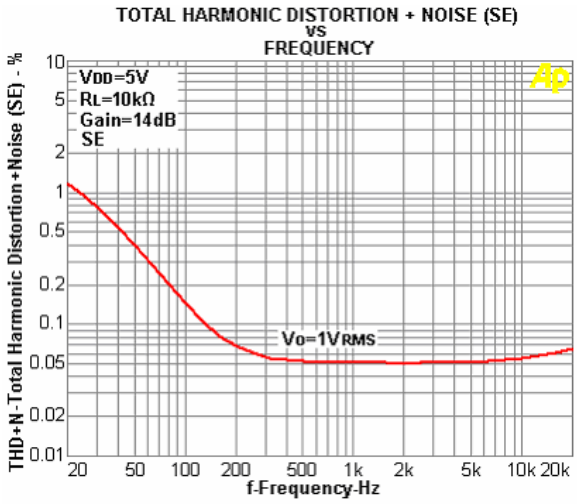


Figure 7

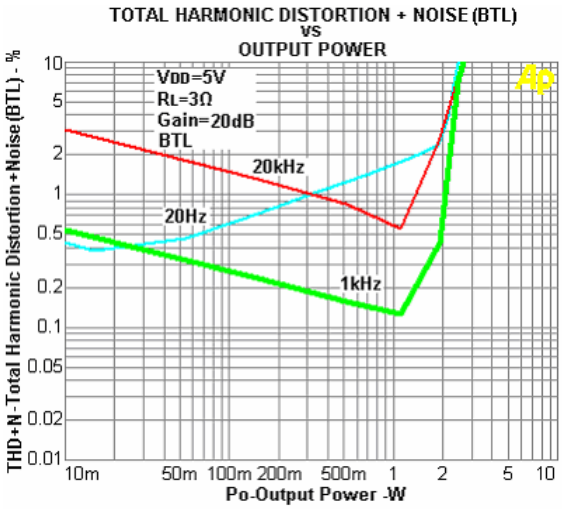


Figure 8

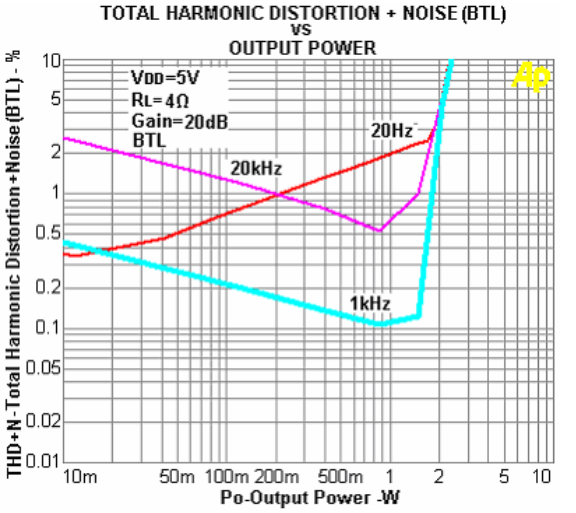


Figure 9

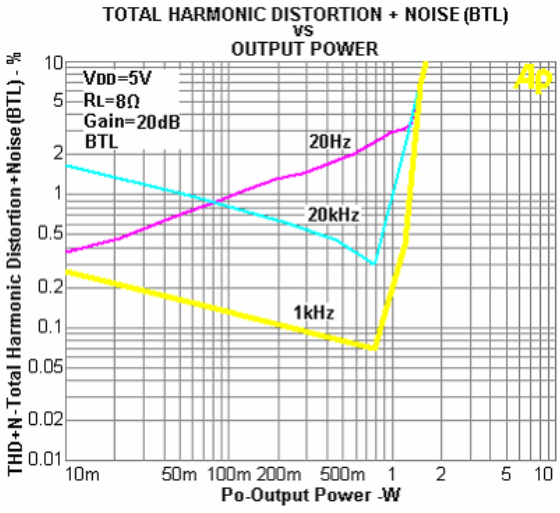


Figure 10

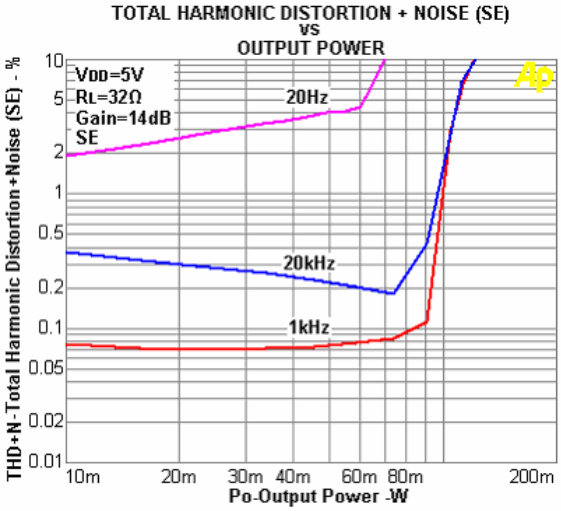


Figure 11

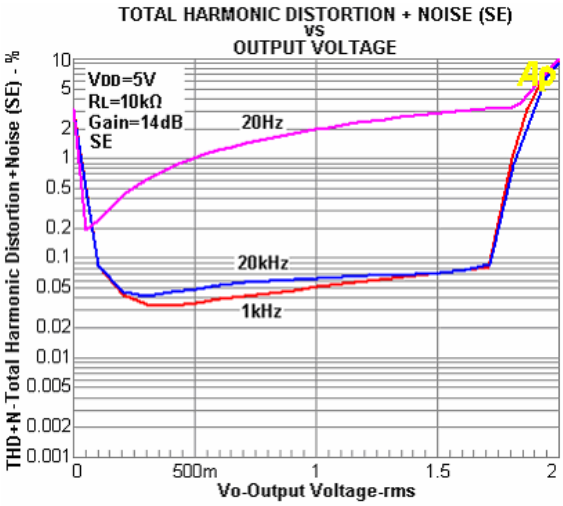


Figure 12

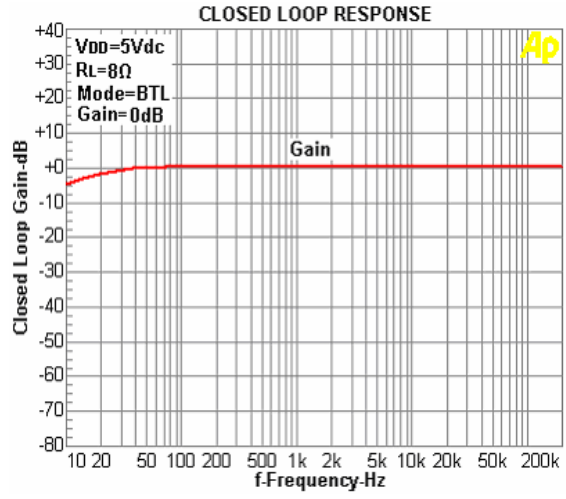


Figure 13

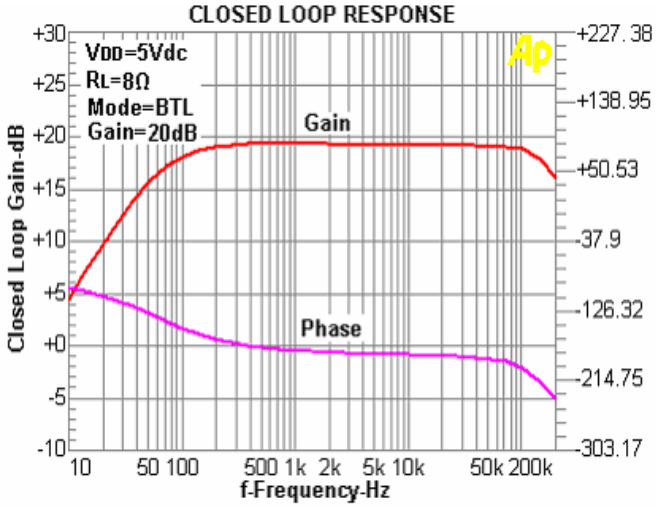


Figure 14

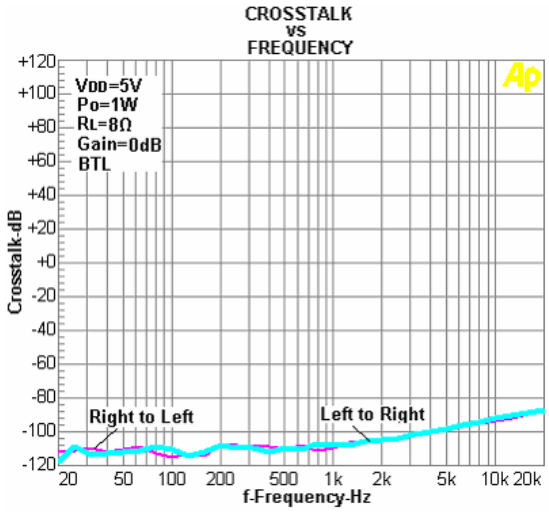


Figure 15

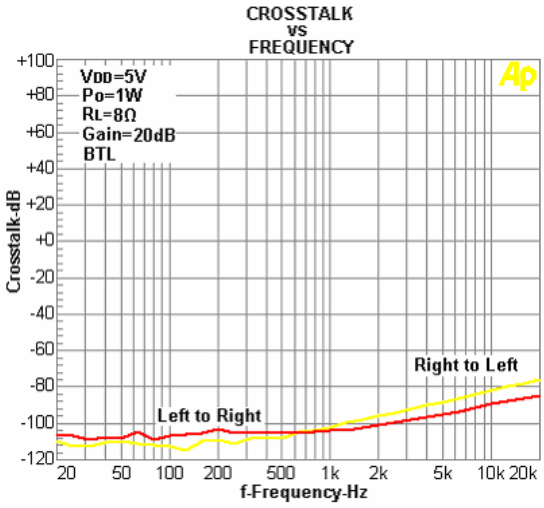


Figure 16

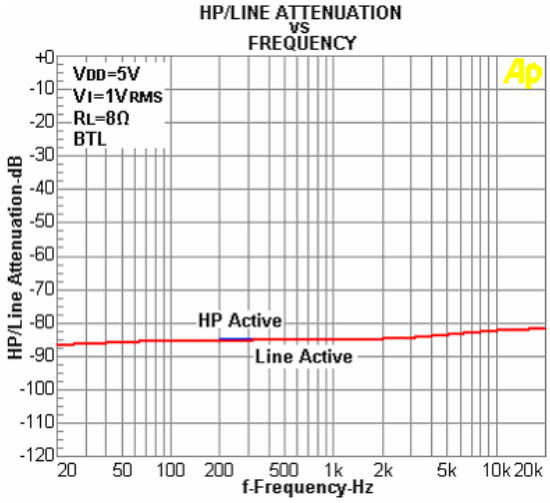


Figure 17

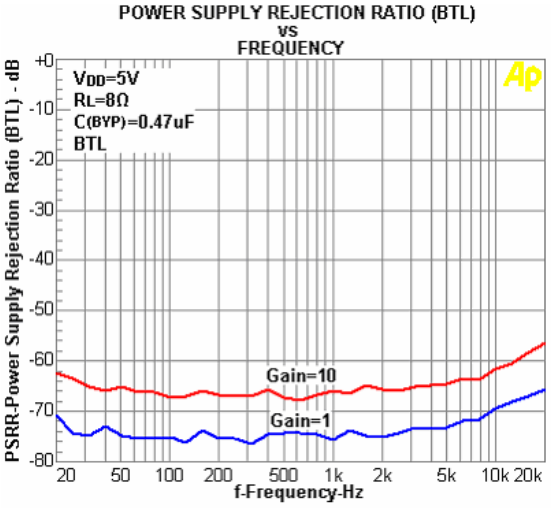


Figure 18

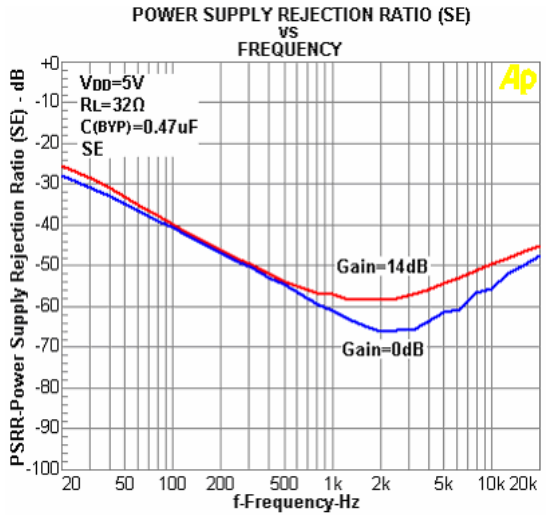


Figure 19

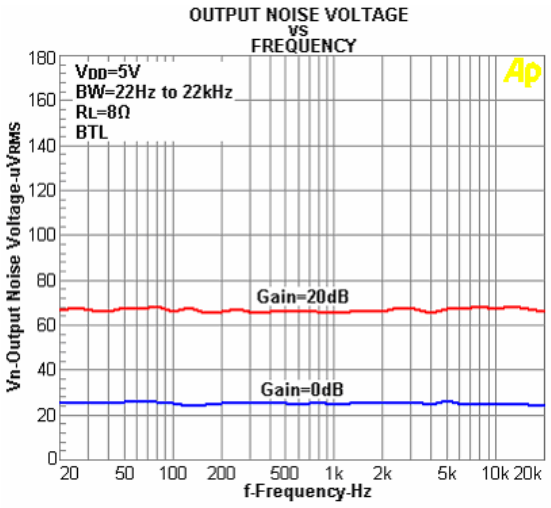


Figure 20

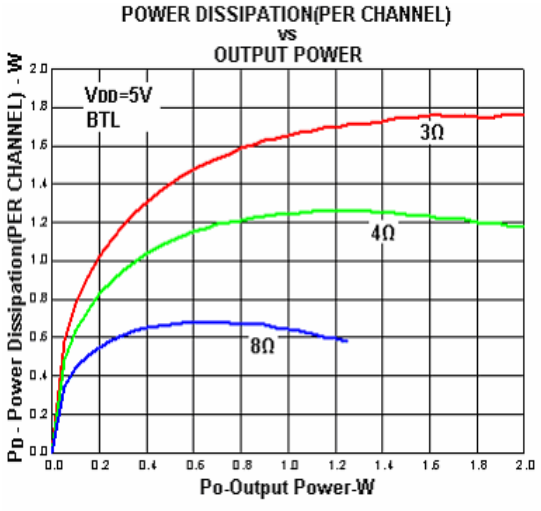


Figure 21

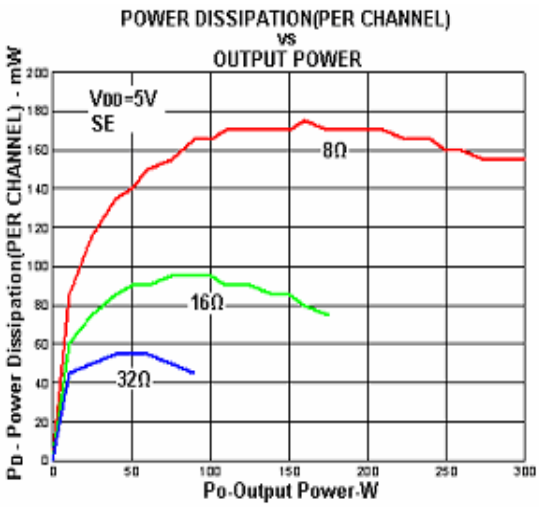


Figure 22

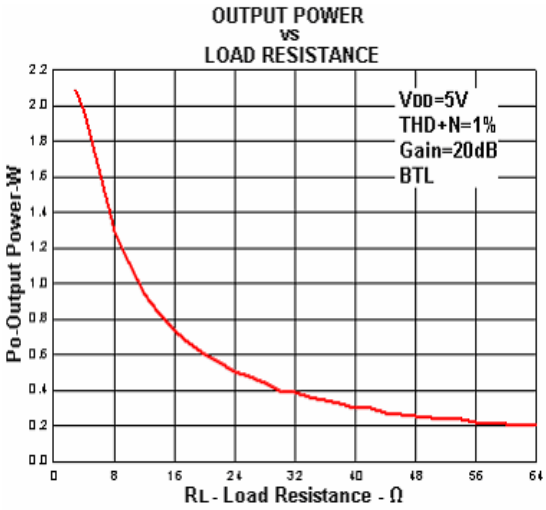


Figure 23

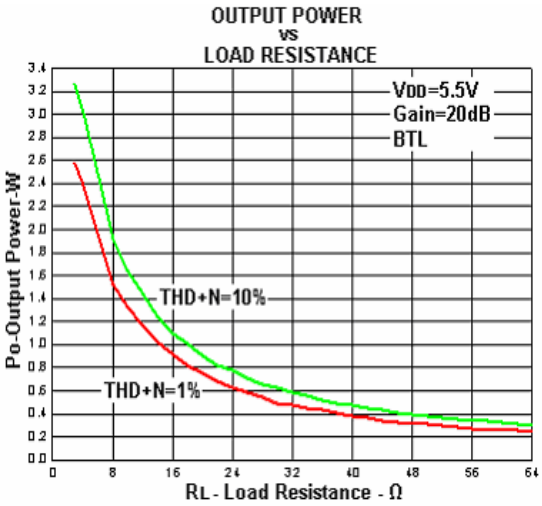


Figure 24

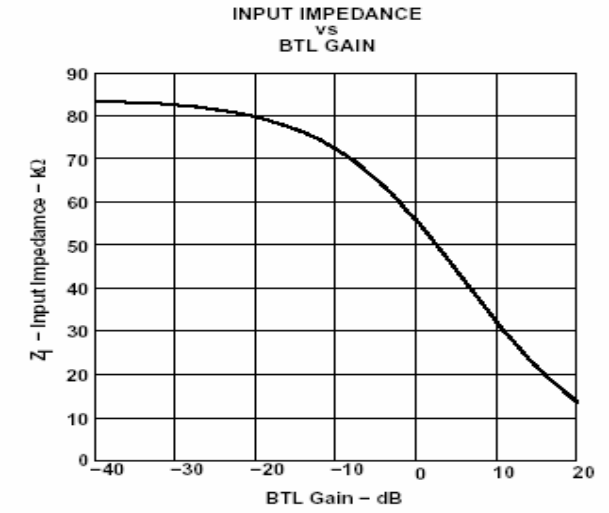


Figure 25

Application Information

VOLUME Operation

The VOLUME pin controls the BTL volume when driving speakers, and the SE volume when driving headphones. This pin is controlled with a dc voltage, which should not exceed V_{DD}.

The output volume increases in discrete steps as the dc voltage increases and decreases in discrete steps as the dc voltage decreases. There are a total of 32 discrete gain steps of the amplifier and range from -85 dB to 20 dB for BTL operation and -85 dB to 14 dB for SE operation.

A pictorial representation of the typical volume control can be found in Figure 26.

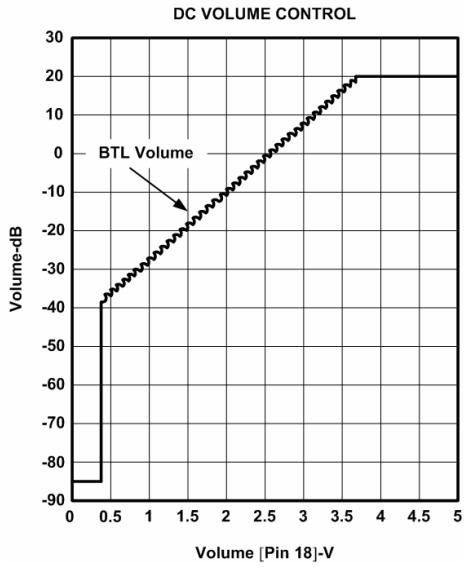


Figure 26. Typical DC Volume Control Operation

Shutdown Modes

The EUA6021A employs a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{SHUTDOWN}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SHUTDOWN}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD}=20µA. $\overline{SHUTDOWN}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 1 . $\overline{SE/BTL}$, and Shutdown Function

Inputs		Amplifier State	
$\overline{SE/BTL}$	$\overline{SHUTDOWN}$	INPUT	OUTPUT
X	Low	X	Mute
Low	High	Line	BTL
High	High	Line	SE
Low	High	HP	BTL
High	High	HP	SE

X= Do not care

$\overline{FADE}$ Operation

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

When the $\overline{FADE}$ input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the recommended operating conditions table.

When a logic low is applied to the $\overline{FADE}$ pin and a logic low is then applied on the $\overline{SHUTDOWN}$ pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58HZ,this equates to 34 ms (1/24 Hz) per step. The gain steps down until the lowest gain step is reached .The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 20dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps , and multiplying by the time per step, or 34 ms.

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of V_{DD}/2 to ground.

This time is dependent on the value of the bypass capacitor. For a 0.47-µF capacitor that is used in the application diagram in Figure 1, the time is approximately 500ms. This time scales linearly with the value of bypass capacitor. For example, if a 1-µF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47-µF capacitor, or 1 second.

When a logic high is placed on the $\overline{SHUTDOWN}$ pin and the $\overline{FADE}$ pin is still held low, the device begins the start-up process, the bypass capacitor will begin charging. Once the bypass voltage reaches the final value of $V_{DD}/2$,the gain increases in2-dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME pins.

In the fade-off mode, the output of the amplifier immediately drops to $V_{DD}/2$ and the bypass capacitor begins a smooth discharge to ground When shutdown is released, the bypass capacitor charges up to $V_{DD}/2$ and the channel gain returns immediately to the value on the VOLUME terminal.

The power-up sequence is different from the shutdown sequence and the voltage on the $\overline{FADE}$ pin does not change the power-up sequence. Upon a power-up condition, the EUA6021A begins in the lowest gain setting and steps up 2 dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME pins.

Bridged-Tied Load Versus Single-Ended Mode

Figure 27 show a Class-AB audio power amplifier (APA) in a BTL configuration. The EUA6021A BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2\times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance(see equation 1)

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad Power = \frac{V_{(rms)}^2}{R_L} \qquad \text{------(1)}$$

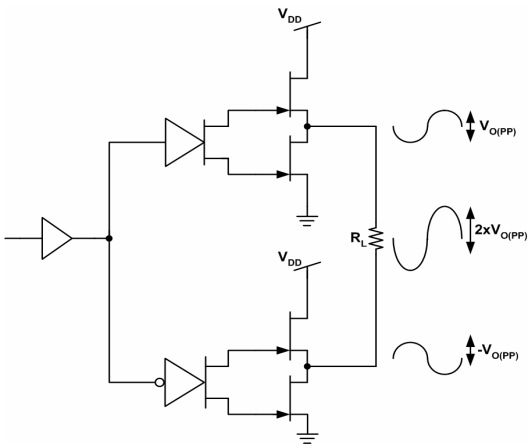


Figure 27.Bridge-Tied Load configuration

In a typical computer sound channel operating at 5V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1W. In sound power that is a 6-dB improvement, which is loudness that can be heard . In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 28.

A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33µF to 1000µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_C = \frac{1}{2\pi R_L C_C} \qquad \text{----------(2)}$$

For example, a 68µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

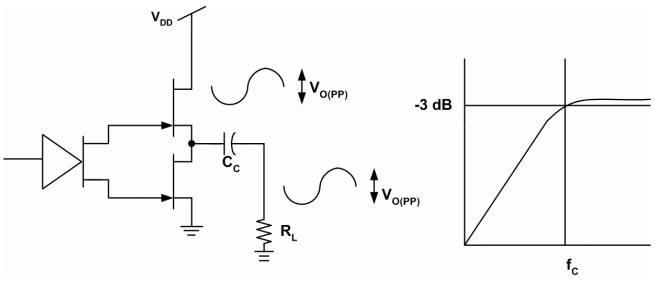


Figure 28. Single-Ended configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 X the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section**.**

Single-Ended Operation

In SE mode the load is driven from the primary amplifier output for each channel. The amplifier switches single-ended operation when the $\overline{SE}/BTL$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain to 1V/V.

SE/$\overline{\text{BTL}}$ Operation

The ability of the EUA6021A to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the EUA6021A , two separate amplifiers drive OUT+ and OUT- .The SE/$\overline{\text{BTL}}$ input control the operation of the follower amplifier that drives LOUT- and ROUT-.When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the EUA6021A is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT- amplifiers are in a high output impedance state, which configures the EUA6021A as an SE driver from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 29.

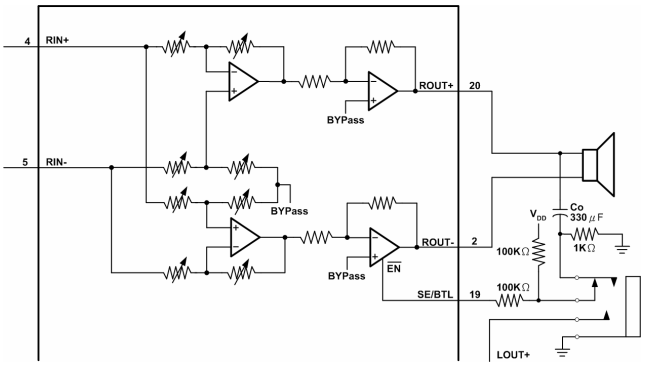


Figure 29. Resistor divider Network circuit 2

Using a readily available 1/8-in. (3.5mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ /1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute(virtually open-circuits the speaker).The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

Input Resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over 6 times that value. As a results, if a single capacitor is used in the input high-pass filter, the –3 dB or cut-off frequency will also change by over 6 times.

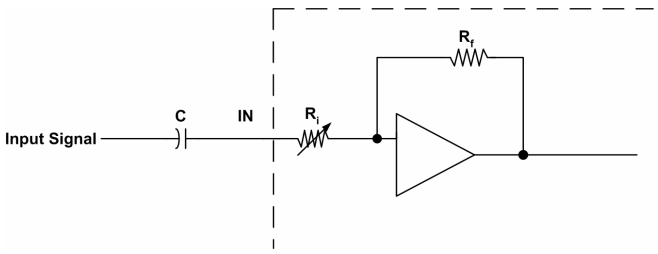


Figure 30. Input Resistor

The-3dB frequency can be calculated using equation 3:

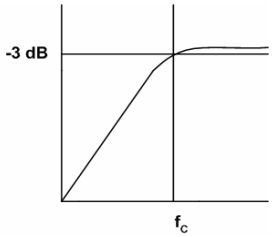
$$f_{-3dB} = \frac{1}{2\pi C (R \parallel R_i)} \quad \text{---------- (3)}$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

Input Capacitor, C_i

In the typical application an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier, Z_i, from a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi Z_i C_i} \text{----------(4)}$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 70kΩ and the specification calls for a flat bass response down to 40Hz.

$$C_i = \frac{1}{2\pi Z_i f_C} \quad \text{---------- (5)}$$

In this example, C_i is 56nF so one would likely choose a value in the range of 56nF to 1µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low- leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor, (C_S)

The EUA6021A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between
the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

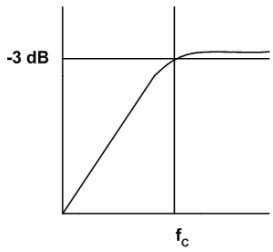
Bypass Capacitor, (C_B)

The bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N. Bypass capacitor, C_B, values of 0.47µF to 1µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Output Coupling Capacitor, (C_C)

For general signal-supply SE configuration, the output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 6.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \quad \text{---------- (6)}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a
C_C of 330µF is chosen and loads vary from 3Ω, 4Ω, 8Ω, 32Ω, 10kΩ, to 47kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances vs Low Frequency Output characteristics in SE Mode

R_L	C_C	Lowest Frequency
3Ω	330µF	161Hz
4Ω	330µF	120Hz
8Ω	330µF	60Hz
32Ω	330µF	15Hz
10000Ω	330µF	0.05Hz
47000Ω	330µF	0.01Hz

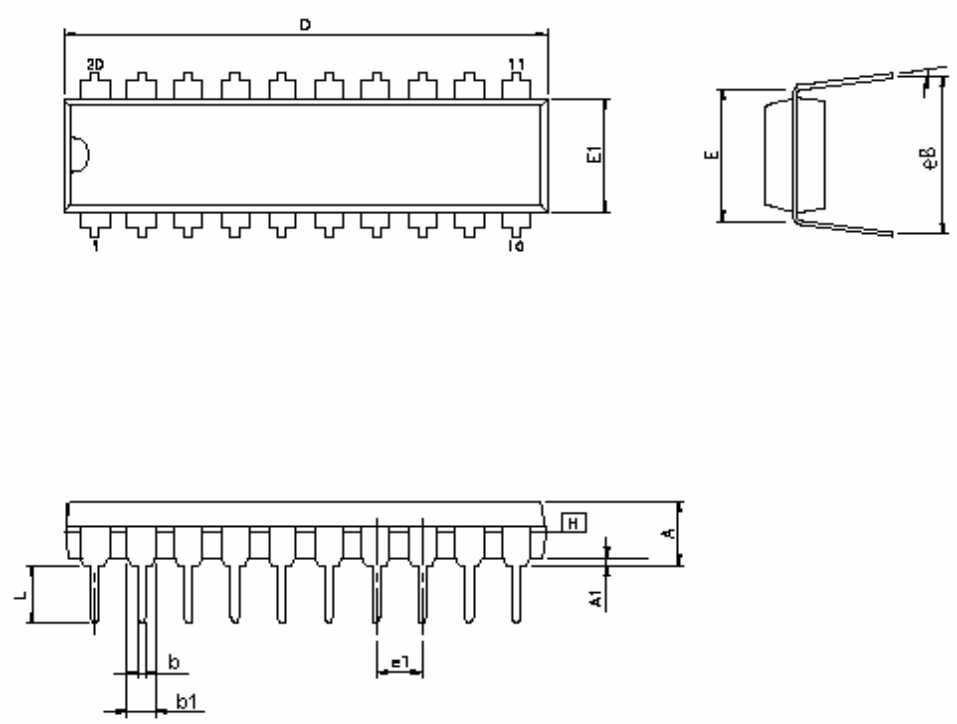
As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load and 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

Using Low- ESR Capacitors

Low- ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

Package Information

DIP-20



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	5.33	-	0.210
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b1	1.40	1.65	0.055	0.065
D	26.16		1.030	
E	7.62		0.300	
E1	6.35		0.250	
e1	2.54		0.100	
L	2.92	3.81	0.115	0.150
eB	8.51	9.53	0.335	0.375