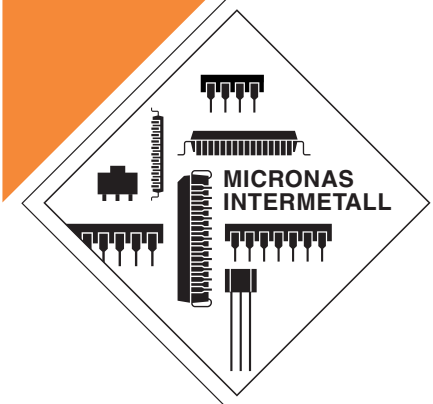



PRELIMINARY DATA SHEET

# MSP 34x1G Multistandard Sound Processor Family with Virtual Dolby Surround

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MICRONAS
INTERMETALL

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**Multistandard Sound Processor Family with Virtual Dolby Surround**

**The hardware and software description in this document is valid for the MSP 34x1G version A1 and following versions.**

## 1. Introduction

The MSP 34x1G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x1G.

The MSP 34x1G has all functions of the MSP 34x0G with the addition of a virtual surround sound feature.

Surround sound can be reproduced to a certain extent with two loudspeakers. The MSP 34x1G includes our virtualizer algorithm “3D-PANORAMA” which has been approved by the Dolby[1)] Laboratories for compliance with the "Virtual Dolby Surround" technology. In addition, the MSP 34x1G includes our “PANORAMA” algorithm.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, MICRONAS Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x1G has optimum stereo performance without any adjustments.

All MSP 34x1G versions are pin and software downward-compatible to the MSP 34x0D. The MSP 34x1G further simplifies controlling software. Standard selection requires a single $I^2C$ transmission only.

The MSP 34x1G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no $I^2C$ interaction is necessary (Automatic Sound Selection).

The ICs are produced in submicron CMOS technology. The MSP 34x1G is available in the following packages: PLCC68, PSDIP64, PSDIP52, PQFP80, and PLQFP64.

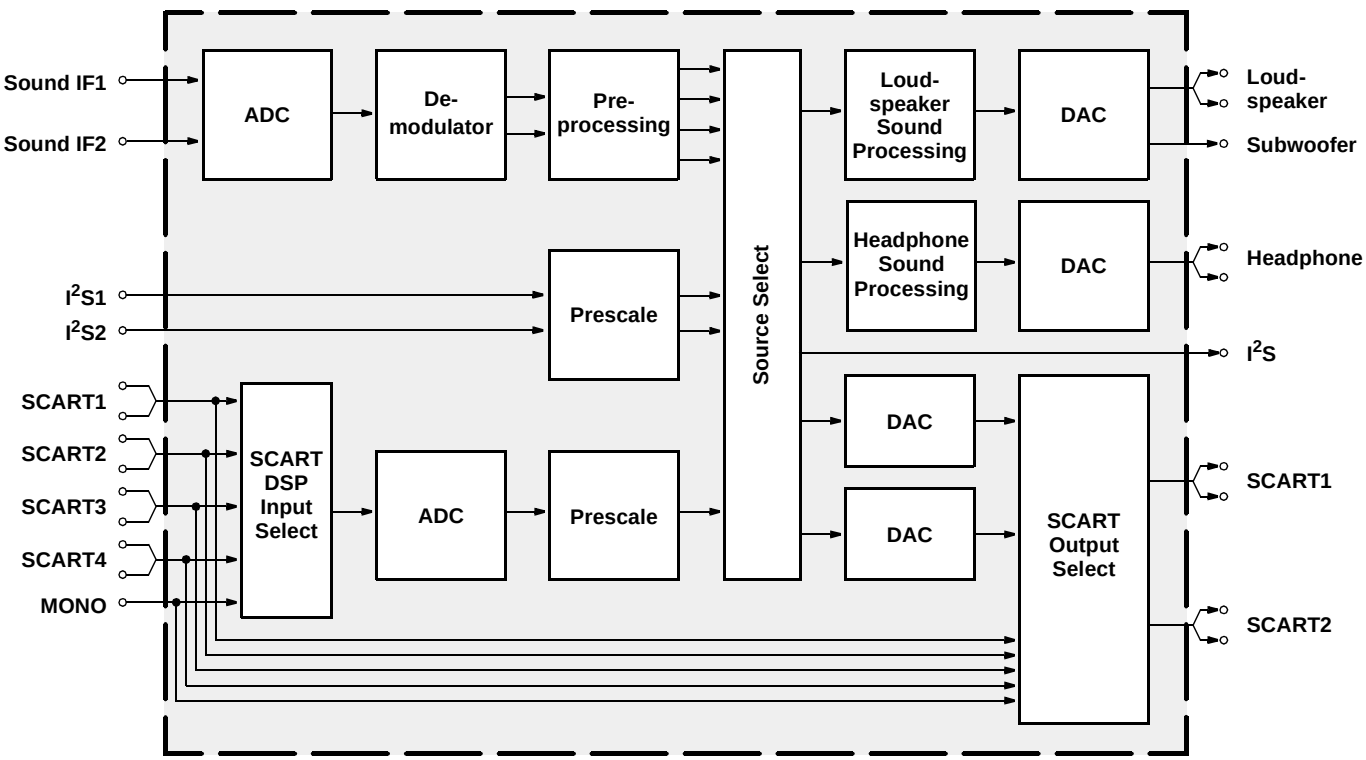



**Fig. 1–1:** Simplified functional block diagram of the MSP 34x1G

### 1.1. Features of the MSP 34x1G Family and Differences to MSP 34xxD

| **Feature** (New features not available for MSP 34xxD are shaded gray.) | **3401** | **3411** | **3421** | **3431** | **3441** | **3451** |
|---|---|---|---|---|---|---|
| 3D-PANORAMA virtualizer (approved by Dolby Laboratories) with noise generator | X | X | X | X | X | X |
| PANORAMA virtualizer algorithm | X | X | X | X | X | X |
| Standard Selection with single $I^2C$ transmission | X | X | X | X | X | X |
| Automatic Standard Detection of terrestrial TV standards | X | X | X | X | X | X |
| Automatic Sound Selection (mono/stereo/bilingual), new registers MODUS, STATUS | X | X | X | X | X | X |
| Two selectable sound IF (SIF) inputs | X | X | X | X | X | X |
| Automatic Carrier Mute function | X | X | X | X | X | X |
| Interrupt output programmable (indicating status change) | X | X | X | X | X | X |
| Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness | X | X | X | X | X | X |
| AVC: Automatic Volume Correction | X | X | X | X | X | X |
| Subwoofer output with programmable low-pass and complementary high-pass filter | X | X | X | X | X | X |
| 5-band graphic equalizer for loudspeaker channel | X | X | X | X | X | X |
| Spatial effect for loudspeaker channel; processing of all deemphasis filtering | X | X | X | X | X | X |
| Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs | X | X | X | X | X | X |
| Complete SCART in/out switching matrix | X | X | X | X | X | X |
| Two $I^2S$ inputs; one $I^2S$ output | X | X | X | X | X | X |
| All analog FM-Stereo A2 and satellite standards; AM-SECAM L standard | X | X | | | | X |
| Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM | X | X | | | | X |
| Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification) | X | X | | | | X |
| ASTRA Digital Radio (ADR) together with DRP 3510A | X | X | | | | X |
| All NICAM standards | | X | | | | X |
| Demodulation of the BTSC multiplex signal and the SAP channel | | | X | X | X | X |
| Alignment free digital DBX noise reduction for BTSC Stereo and SAP | | | | X | X | X |
| Alignment free digital MICRONAS Noise Reduction (MNR) for BTSC Stereo and SAP | | | X | | | |
| BTSC stereo separation (MSP 3421/41G also EIA-J) significantly better than spec. | | | X | X | X | X |
| SAP and stereo detection for BTSC system | | | X | X | X | X |
| Korean FM-Stereo A2 standard | X | X | X | | X | X |
| Alignment-free Japanese standard EIA-J | | | X | | X | X |
| Demodulation of the FM-Radio multiplex signal | | | X | X | X | X |

### 1.2. MSP 34x1G Version List

| **Version** | **Status** | **Description** |
|---|---|---|
| MSP 3401G | planned | FM Stereo (A2) Version |
| MSP 3411G | planned | NICAM and FM Stereo (A2) Version |
| MSP 3421G | planned | NTSC Version (A2 Korea, BTSC with MICRONAS Noise Reduction (MNR), and Japanese EIA-J system) |
| MSP 3431G | planned | BTSC Version |
| MSP 3441G | planned | NTSC Version (A2 Korea, BTSC with DBX noise reduction, and Japanese EIA-J system) |
| MSP 3451G | available | Global Version (all sound standards) |

### 1.3. MSP 34x1G Versions and their Application Fields

Table 1–1 provides an overview of TV sound standards that can be processed by the MSP 34x1G family. In addition, the MSP 34x1G is able to handle the terrestrial FM-Radio standard. With the MSP 34x1G, a complete multimedia receiver covering all TV sound standards together with terrestrial and satellite radio sound can be built; even ASTRA Digital Radio can be processed (with a DRP 3510A coprocessor).

**Table 1–1:** TV Stereo Sound Standards covered by the MSP 34x1G IC Family (details see Appendix A)

| MSP Version | | | | TV-System | Position of Sound Carrier /MHz | Sound Modulation | Color System | Broadcast e.g. in: |
|---|---|---|---|---|---|---|---|---|
| 3401 | | 3411 | 3451 | B/G | 5.5/5.7421875 | FM-Stereo (A2) | PAL | Germany |
| | | | | | 5.5/5.85 | FM-Mono/NICAM | PAL | Scandinavia, Spain |
| | | | | L | 6.5/5.85 | AM-Mono/NICAM | SECAM-L | France |
| | | | | I | 6.0/6.552 | FM-Mono/NICAM | PAL | UK, Hong Kong |
| 3401 | | | | D/K | 6.5/6.2578125 | FM-Stereo (A2, D/K1) | SECAM-East | Slovak. Rep. |
| | | | | | 6.5/6.7421875 | FM-Stereo (A2, D/K2) | PAL | currently no broadcast |
| | | | | | 6.5/5.7421875 | FM-Stereo (A2, D/K3) | SECAM-East | Poland |
| | | | | | 6.5/5.85 | FM-Mono/NICAM (D/K, NICAM) | PAL | China, Hungary |
| 3401 | | | | Satellite | 6.5<br>7.02/7.2<br>7.38/7.56<br>etc. | FM-Mono<br>FM-Stereo<br>ASTRA Digital Radio (ADR) with DRP 3510A | PAL | Europe Sat.<br>ASTRA |
| | 3421, 3441 | | | M/N | 4.5/4.724212 | FM-Stereo (A2) | NTSC | Korea |
| | | | | | 4.5 | FM-FM (EIA-J) | NTSC | Japan |
| | | 3431 | | | 4.5 | BTSC-Stereo + SAP | NTSC, PAL | USA, Argentina |
| | | | | FM-Radio | 10.7 | FM-Stereo Radio | | USA, Europe |

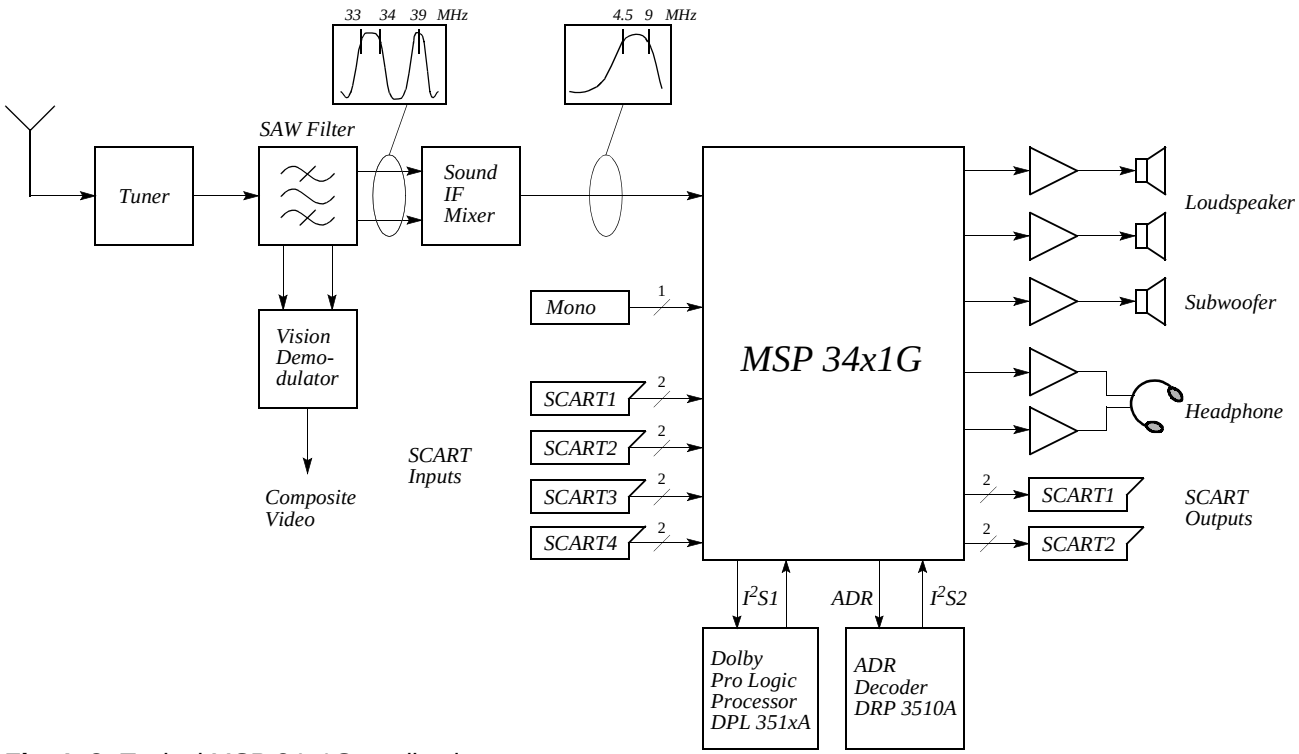



**Fig. 1–2:** Typical MSP 34x1G application

## 2. Functional Description

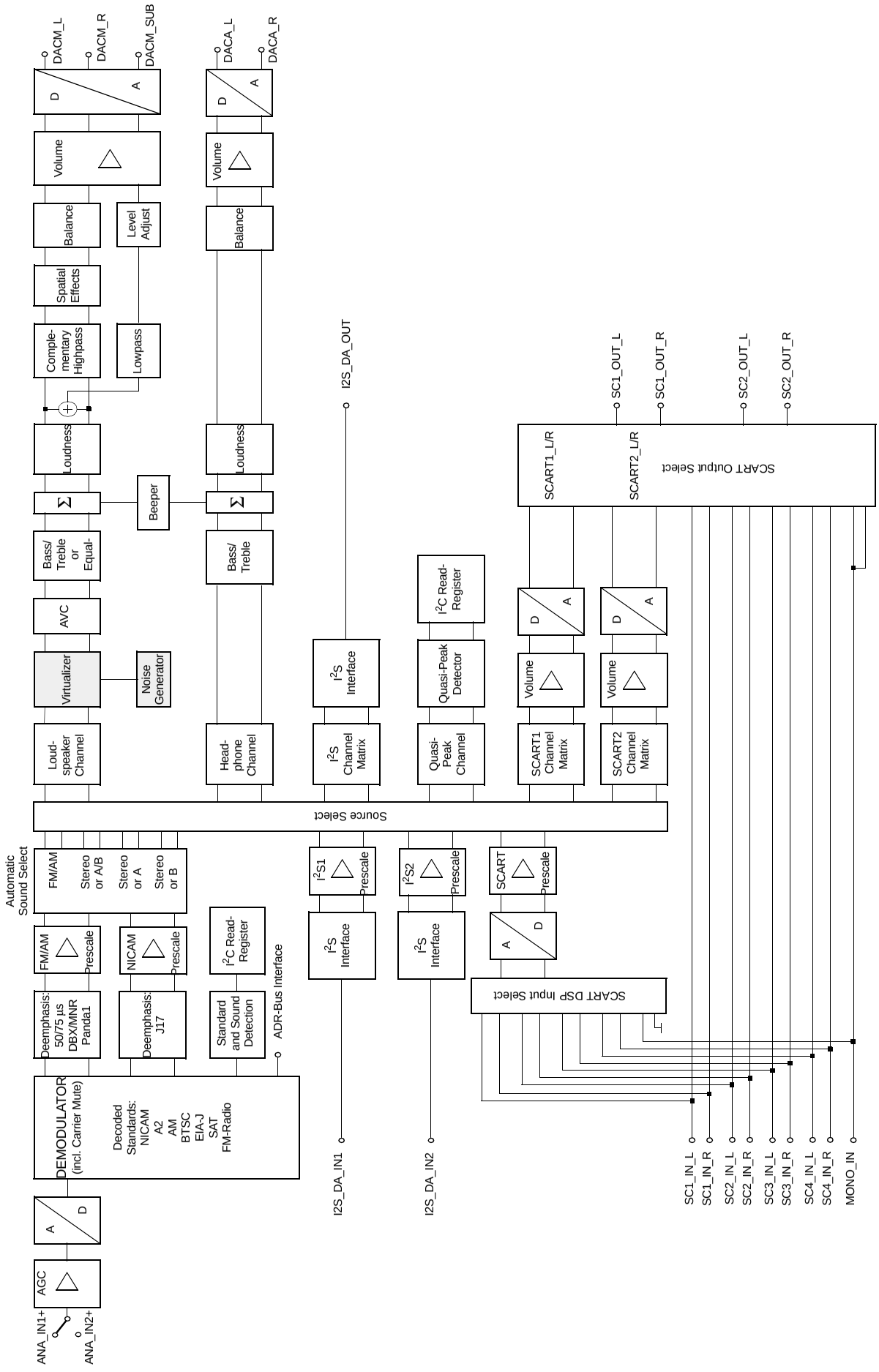



**Fig. 2–1:** Signal flow block diagram of the MSP 34x1G (input and output names correspond to pin names)

### 2.1. Architecture of the MSP 34x1G Family

Fig. 2–1 on page 9 shows a simplified block diagram of the IC. The block diagram contains all features of the MSP 3451G. Other members of the MSP 34x1G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 3411G and MSP 3451G.

### 2.2. Sound IF Processing

#### 2.2.1. Analog Sound IF Input

The input pins ANA_IN1+, ANA_IN2+, and ANA_IN– offer the possibility to connect two different sound IF (SIF) sources to the MSP 34x1G. The analog-to-digital conversion of the preselected sound IF signal is done by an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The high-pass filters formed by the coupling capacitors at pins ANA_IN1+ and ANA_IN2+ see Section 8. “Appendix E: Application Circuit” on page 100 are sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

#### 2.2.2. Demodulator: Standards and Features

The MSP 34x1G is able to demodulate all TV-sound standards worldwide including the digital NICAM system. Depending on the MSP 34x1G version, the following demodulation modes can be performed:

**A2 Systems:** Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

**NICAM Systems:** Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

**Very high deviation FM-Mono:** Detection and robust demodulation of one FM carrier with a maximum deviation of 540 kHz.

**BTSC-Stereo:** Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L–R)-carrier and detection of the SAP subcarrier. Processing of DBX noise reduction or MICRONAS Noise Reduction (MNR).

**BTSC-Mono + SAP:** Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP subcarrier. Processing of DBX noise reduction or MICRONAS Noise Reduction (MNR).

**Japan Stereo:** Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L–R)-carrier.

**FM-Satellite Sound:** Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

**FM-Stereo-Radio:** Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L–R)-carrier.

The demodulator blocks of all MSP 34x1G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 34x1G demodulator blocks are

**Standard Selection:** The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

**Automatic Standard Detection:** If the TV sound standard is unknown, the MSP 34x1G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

**Automatic Carrier Mute:** To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 34x1G offers a carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STANDARD SELECT register. If no FM carrier is available at one of the two MSP demodulator channels, the corresponding demodulator output is muted.

### 2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically set by the Automatic Sound Selection.

### 2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No $I^2C$ interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono compatible standards (standards that have the same FM mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 34x1G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2–1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (Fig 2–3). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

– **“FM/AM” channel:** Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).

– **“Stereo or A/B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).

– **“Stereo or A” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).

– **“Stereo or B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig 2–2 shows the source channel assignment of the demodulated signals in case of manual mode. If manual mode is required, more information can be found in the section “Demodulator Source Channels in Manual Mode” on page 96. Fig 2–3 and Table 2–2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

**Note:** The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the 2nd FM carrier, the L–R signal of the MPX carrier, or the SAP signal.

### 2.3. Preprocessing for SCART and $I^2S$ Input Signals

The SCART and $I^2S$ inputs need only be adjusted in level by means of the SCART and $I^2S$ prescale registers.

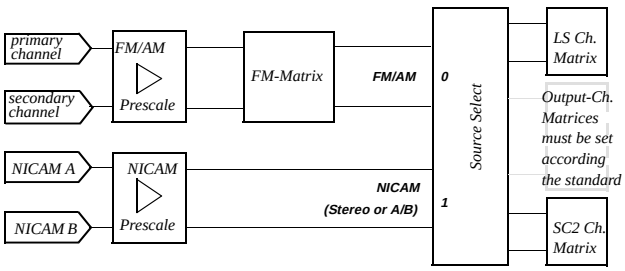



**Fig. 2–2:** Source channel assignment of demodulated signals in Manual Mode

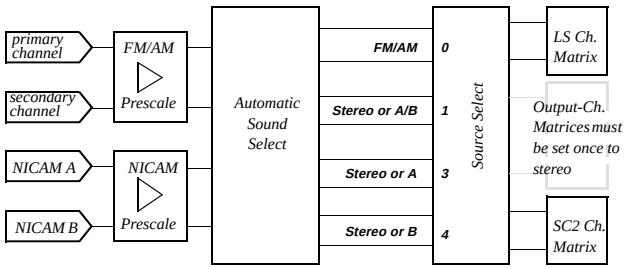



**Fig. 2–3:** Source channel assignment of demodulated signals in Automatic Sound Select Mode

**Table 2–1:** Performed actions of the Automatic Sound Selection

| Selected TV Sound Standard | Performed Actions |
|---|---|
| B/G-FM, D/K-FM, M-Korea, and M-Japan | Evaluation of the identification signal and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. Identification is acquired after 500 ms. |
| B/G-NICAM, L-NICAM, I-NICAM, and D/K-NICAM | Evaluation of NICAM-C-bits and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. NICAM detection is acquired within 150 ms. |
| | In case of bad or no NICAM reception, the MSP switches automatically to FM/AM mono and switches back to NICAM if possible. A hysteresis prevents periodical switching. |
| B/G-FM, B/G-NICAM or D/K1-FM, D/K2-FM, D/K3-FM, and D/K-NICAM | Automatic searching for stereo/bilingual-identification in case of mono transmission. Automatic and non-audible changes between Dual-FM and FM-NICAM standards while listening to the basic FM-Mono sound carrier.<br>Example: If starting with B/G-FM-Stereo, there will be a periodical alternation to B/G-NICAM in the absence of FM-Stereo/Bilingual or NICAM-identification. Once an identification is detected, the MSP keeps the corresponding standard. |
| BTSC-STEREO, FM Radio | Evaluation of the pilot signal and automatic switching to mono or stereo. Preparing four demodulator source channels according to Table 2–2. Detection of the SAP carrier. Pilot detection is acquired after 200 ms. |
| BTSC-SAP | In the absence of SAP, the MSP switches to BTSC-Stereo if available. If SAP is detected, the MSP switches automatically to SAP (see Table 2–2). |

**Table 2–2:** Sound modes for the demodulator source channels with Automatic Sound Select

| | | | Source Channels in Automatic Sound Select Mode | | | |
|---|---|---|---|---|---|---|
| **Broadcasted Sound Standard** | **Selected MSP Standard Code**[3)] | **Broadcasted Sound Mode** | **FM/AM** (source select: 0) | **Stereo or A/B** (source select: 1) | **Stereo or A** (source select: 3) | **Stereo or B** (source select: 4) |
| M-Korea<br>B/G-FM<br>D/K-FM<br>M-Japan | 02<br>03, 08[1)]<br>04, 05, 07, 0B[1)]<br>30 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |
| | | BILINGUAL:<br>Languages A and B | Left = A<br>Right = B | Left = A<br>Right = B | A | B |
| B/G-NICAM<br>L-NICAM<br>I-NICAM<br>D/K-NICAM<br>D/K-NICAM<br>(with high deviation FM) | 08, 03[2)]<br>09<br>0A<br>0B, 04[2)], 05[2)]<br>0C | NICAM not available or error rate too high | analog Mono | analog Mono | analog Mono | analog Mono |
| | | MONO | analog Mono | NICAM Mono | NICAM Mono | NICAM Mono |
| | | STEREO | analog Mono | NICAM Stereo | NICAM Stereo | NICAM Stereo |
| | | BILINGUAL:<br>Languages A and B | analog Mono | Left = NICAM A<br>Right = NICAM B | NICAM A | NICAM B |
| BTSC | 20, 21 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |
| | 20 | MONO+SAP | Mono | Mono | Mono | Mono |
| | | STEREO+SAP | Stereo | Stereo | Stereo | Stereo |
| | 21 | MONO+SAP | Left = Mono<br>Right = SAP | Left = Mono<br>Right = SAP | Mono | SAP |
| | | STEREO+SAP | Left = Mono<br>Right = SAP | Left = Mono<br>Right = SAP | Mono | SAP |
| FM Radio | 40 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |

[1)] The Automatic Sound Select process will automatically switch to the mono compatible analog standard.
[2)] The Automatic Sound Select process will automatically switch to the mono compatible digital standard.
[3)] The MSP Standard Codes are defined in Table 3–7 on page 25.

### 2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels, SCART, or $I^2S$ input) to the desired output channels (loudspeaker, headphone, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

### 2.5. Audio Baseband Processing

#### 2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The Automatic Volume Correction (AVC) solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see page 34).

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains a fixed output level of –18 dBr. Fig. 2–4 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

– SCART input/output 0 dBr = 2.0 $V_{rms}$

– Loudspeaker and Aux output 0 dBr = 1.4 $V_{rms}$

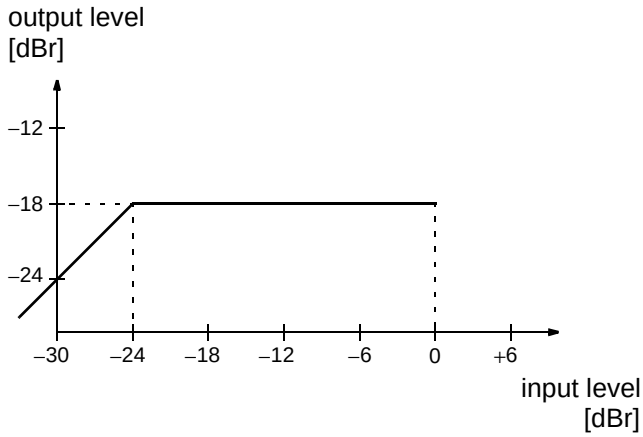



**Fig. 2–4:** Simplified AVC characteristics

#### 2.5.2. Loudspeaker and Headphone Outputs

The following baseband features are implemented in the loudspeaker and headphone output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to the loudspeaker and headphone channel. The loudspeaker channel additionally performs: equalizer (not simultaneously with bass/treble), spatial effects, and a subwoofer crossover filter.

#### 2.5.3. Subwoofer Output

The subwoofer signal is created by combining the left and right channels directly behind the loudness block using the formula (L+R)/2. Due to the division by 2, the D/A converter will not be overloaded, even with full scale input signals. The subwoofer signal is filtered by a third-order low-pass with programmable corner frequency followed by a level adjustment. At the loudspeaker channels, a complementary high-pass filter can be switched on. Subwoofer and loudspeaker output use the same volume (Loudspeaker Volume Register).

#### 2.5.4. Quasi-Peak Detector

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

attack time: 1.3 ms
decay time: 37 ms

## 2.6. Virtual Surround System Application Tips

### 2.6.1. Sweet Spot

Good results are only obtained in a rather close area along the middle axis between the two loudspeakers: the sweet spot. Moving away from this position degrades the effect.

### 2.6.2. Clipping

For the test at Dolby Labs, it is very important to have no clipping effects even with worst case signals. That is, 2 Vrms input signal may not clip. The SCART Input Prescale register has to be set to values of $19_{hex}$ ($25_{dec}$) or lower (see SCART Input Prescale on page 31).

Test signals: sine sweep with 2 $V_{RMS}$; L only, R only, L&R equal phase, L&R anti phase.

Listening tests: Dolby Trailers (train trailer, city trailer, canyon trailer...)

### 2.6.3. Loudspeaker Requirements

The loudspeakers used and their positioning inside the TV set will greatly influence the performance of the virtualizer. The algorithm works with the direct sound path. Reflected sound waves reduce the effect. So it's most important to have as much direct sound as possible, compared to indirect sound.

To obtain the approval for a TV set, Dolby Laboratories require mounting the loudspeakers in front of the set. Loudspeakers radiating to the side of the TV set will not produce convincing effects. Good directionality of the loudspeakers towards the listener is optimal.

The virtualizer was specially developed for implementation in TV sets. Even for rather small stereo TV's, sufficient sound effects can be obtained. For small sets, the loudspeaker placement should be to the side of the CRT; for large screen sets (or 16:9 sets), mounting the loudspeakers below the CRT is acceptable (large separation is preferred, low frequency speakers should be outmost to avoid cancellation effects). Using external loudspeakers with a large stereo base will not create optimal effects.

The loudspeakers should be able to reproduce a wide frequency range. The most important frequency range starts from 160 Hz and ranges up to 5 kHz.

Great care has to be taken with systems that use one common subwoofer: A single loudspeaker cannot reproduce virtual sound locations. The crossover frequency must be lower than 120 Hz.

### 2.6.4. Cabinet Requirements

During listening tests at Dolby Laboratories, **no resonances** in the cabinet should occur.

Good material to check for resonances are the Dolby Trailers or other dynamic sound tracks.

### 2.7. SCART Signal Routing

#### 2.7.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with four pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 40).

#### 2.7.2. Stand-by Mode

If the MSP 34x1G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off the 5-V, but keeping the 8-V power supply (**'Stand-by'-mode**), the SCART switches maintain their position and function. This allows the copying from selected SCART-inputs to SCART-outputs in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the 5-V supply, RESETQ going high 2 ms later), all internal registers except the ACB register (page 40) are reset to the default configuration (see Table 3–5 on page 22). The reset position of the ACB register becomes active after the first $I^2C$ transmission into the Baseband Processing part (subaddress $12_{hex}$). By transmitting the ACB register first, the reset state can be redefined.

### 2.8. $I^2S$ Bus Interface

It is possible to route in an external coprocessor for special effects, like surround processing and sound field processing. Routing can be done with each input source and output channel via the $I^2S$ inputs and outputs.

Two possible interface formats are supported:

1. The SONY format: I2S_WS changes at the word boundaries.
2. The PHILIPS format: I2S_WS changes one I2S_CL period before the word boundaries.

The $I^2S$ bus interface consists of five pins:

1. I2S_DA_IN1, I2S_DA_IN2:
   For input, four channels (two channels per line, 2*16 bits) per sampling cycle (32 kHz) are transmitted.
2. I2S_DA_OUT:
   For output, two channels (2*16 bits) per sampling cycle (32 kHz) are transmitted.
3. I2S_CL:
   Gives the timing for the transmission of $I^2S$ serial data (1.024 MHz).
4. I2S_WS:
   The I2S_WS word strobe line defines the left and right sample.

The MSP 34x1G normally serves as the master on the $I^2S$ interface. In this case, the clock and word strobe lines are driven by the MSP 34x1G. In slave mode, these lines are input to the MSP 34x1G and the master clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in this mode.

All $I^2S$ options can be set by means of the MODUS register (see page 28).

A precise $I^2S$ timing diagram is shown in Fig. 4–26 on page 70.

### 2.9. ADR Bus Interface

For the ASTRA Digital Radio System (ADR), the MSP 3401G, MSP 3411G and MSP 3451G performs preprocessing such as carrier selection and filtering. Via the 3-line ADR-bus, the resulting signals are transferred to the DRP 3510A coprocessor, where the source decoding is performed. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 34x1G should be provided on a feature connector:

– AUD_CL_OUT

– I2S_DA_IN1 or I2S_DA_IN2

– I2S_DA_OUT

– I2S_WS

– I2S_CL

– ADR_CL, ADR_WS, ADR_DA

For more details, please refer to the DRP 3510A data sheet.

### 2.10.Digital Control I/O Pins and Status Change Indication

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the $I^2C$-bus by means of the ACB register (see page 40). This enables the controlling of external hardware switches or other devices via $I^2C$-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 28). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 29).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary, $I^2C$ bus interactions are reduced to a minimum (see STATUS register on page 29 and MODUS register on page 28).

### 2.11. Clock PLL Oscillator and Crystal Specifications

The MSP 34x1G derives all internal system clocks from the 18.432-MHz oscillator. In NICAM or in $I^2S$-Slave mode, the clock is phase-locked to the corresponding source. Therefore, it is not possible to use NICAM and $I^2S$-Slave mode at the same time.

For proper performance, the MSP clock oscillator requires a 18.432-MHz crystal. Note that for the phase-locked modes (NICAM, $I^2S$-Slave), crystals with tighter tolerance are required.

**Remark on using the crystal:**
External capacitors at each crystal pin to ground are required. They are necessary for tuning the open-loop frequency of the internal PLL and for stabilizing the frequency in closed-loop operation. The higher the capacitors, the lower the resulting clock frequency. The nominal free running frequency should match 18.432 MHz as closely as possible.

Clock measurements should be done at pin AUD_CL_OUT. This pin must be activated for this purpose (see Table 3–9 on page 28).

## 3. Control Interface

### 3.1. I²C Bus Interface

#### 3.1.1. Device and Subaddresses

The MSP 34x1G is controlled via the I²C bus slave interface.

The IC is selected by transmitting one of the MSP 34x1G device addresses. In order to allow up to three MSP ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high, low, or left open, the MSP 34x1G responds to different device addresses. A device address pair is defined as a write address (80, 84, or 88 hex) and a read address (81, 85, or 89 hex) (see Table 3–1).

Writing is done by sending the device write address, followed by the subaddress byte, two address bytes, and two data bytes. Reading is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address (81, 85, or 89 hex) and reading two bytes of data. Refer to section 3.1.3. for the I²C bus protocol and to section “Programming Tips” on page 44 for proposals of MSP 34x1G I²C telegrams. See Table 3–2 for a list of available subaddresses.

Besides the possibility of hardware reset, the MSP can also be reset by means of the RESET bit in the CONTROL register by the controller via I²C bus.

Due to the internal architecture of the MSP 34x1G, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the MSP cannot accept another complete byte of data until it has performed some other function (for example, servicing an internal interrupt), it will hold the clock line I2C_CL LOW to force the transmitter into a wait state. The positions within a transmission where this may happen are indicated by ’Wait’ in section 3.1.3. The maximum wait period of the MSP during normal operation mode is less than 1 ms.

**Internal hardware error handling:**

In case of any internal hardware error (e.g. interruption of the power supply of the MSP), the MSP’s wait period is extended to 1.8 ms. After this time period elapses, the MSP releases data and clock lines.

**Indication and solving of the error status:**

**1.** MSP 34x1G**-versions until A1:** To indicate the error status, all further acknowledge bits will be left high. The MSP can then be reset by transmitting the reset condition to CONTROL while ignoring the missing acknowledge bits.

**2.** MSP 34x1G**-versions from A2 on:** To indicate the error status, the remaining acknowledge bits of the actual I²C-protocol will be left high. Additionally, bit[14] of CONTROL is set to one. The MSP can then be reset via the I²C bus by transmitting the reset condition to CONTROL.

**Indication of reset (only versions from A2 on):**

Any reset, even caused by an unstable reset line etc., is indicated in bit[15] of CONTROL.

A general timing diagram of the I²C bus is shown in Fig. 4–25 on page 68.

**Table 3–1:** I²C Bus Device Addresses

| ADR_SEL | Low | | High | | Left Open | |
|---|---|---|---|---|---|---|
| **Mode** | **Write** | **Read** | **Write** | **Read** | **Write** | **Read** |
| MSP device address | 80 hex | 81 hex | 84 hex | 85 hex | 88 hex | 89 hex |

**Table 3–2:** I²C Bus Subaddresses

| Name | Binary Value | Hex Value | Mode | Function |
|---|---|---|---|---|
| CONTROL | 0000 0000 | 00 | Read/Write | Write: Software reset of MSP (see Table 3–3)<br>Read: Hardware error status of MSP |
| TEST | 0000 0001 | 01 | Write | only for internal use |
| WR_DEM | 0001 0000 | 10 | Write | write address demodulator |
| RD_DEM | 0001 0001 | 11 | Write | read address demodulator |
| WR_DSP | 0001 0010 | 12 | Write | write address DSP |
| RD_DSP | 0001 0011 | 13 | Write | read address DSP |

### 3.1.2. Description of CONTROL Register

**Table 3–3:** CONTROL as a Write Register

| Name | Subaddress | Bit[15] (MSB) | Bits[14:0] |
|---|---|---|---|
| CONTROL | 00 hex | 1 : RESET<br>0 : normal | 0 |

**Table 3–4:** CONTROL as a Read Register (only MSP 34x1G-versions from A2 on)

| Name | Subaddress | Bit[15] (MSB) | Bit[14] | Bits[13:0] |
|---|---|---|---|---|
| CONTROL | 00 hex | Reset status after last reading of CONTROL:<br>0 : no reset occured<br>1 : reset occured | Internal hardware status:<br>0 : no error occured<br>1 : internal error occured | not of interest |
| Reading of CONTROL will reset the bits[15,14] of CONTROL. After Power-on, bit[15] of CONTROL will be set; it must be read once to be resetted. | | | | |

### 3.1.3. Protocol Description

Write to DSP or Demodulator

| S | write device address | Wait | ACK | sub-addr | ACK | addr-byte high | ACK | addr-byte low | ACK | data-byte-high | ACK | data-byte low | ACK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Read from DSP or Demodulator

| S | write device address | Wait | ACK | sub-addr | ACK | addr-byte high | ACK | addr-byte low | ACK | S | read device address | Wait | ACK | data-byte-high | ACK | data-byte low | NAK | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Write to Control or Test Registers

| S | write device address | Wait | ACK | sub-addr | ACK | data-byte high | ACK | data-byte low | ACK | P |
|---|---|---|---|---|---|---|---|---|---|---|

Note: S = $I^2C$-Bus Start Condition from master
P = $I^2C$-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= MSP, light gray) or master (= controller dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate ‘End of Read’ or from MSP indicating internal error state
Wait = $I^2C$-Clock line is held low, while the MSP is processing the $I^2C$ command. This waiting time is max. 1 ms

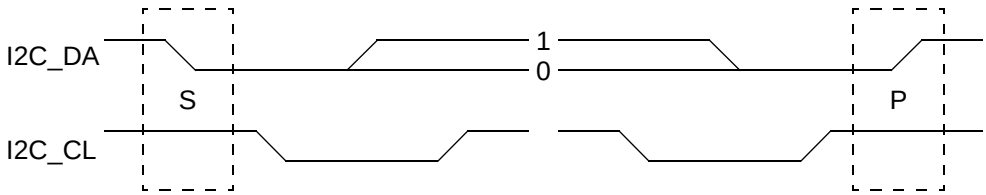



**Fig. 3–1:** $I^2C$ bus protocol (MSB first; data must be stable while clock is high)

### 3.1.4. Proposals for General MSP 34x1G I²C Telegrams

#### 3.1.4.1. Symbols

| | |
|---|---|
| daw | write device address ($80_{hex}$, $84_{hex}$ or $88_{hex}$) |
| dar | read device address ($81_{hex}$, $85_{hex}$ or $89_{hex}$) |
| < | Start Condition |
| > | Stop Condition |
| aa | Address Byte |
| dd | Data Byte |

#### 3.1.4.2. Write Telegrams

| | |
|---|---|
| <daw 00 d0 00> | write to CONTROL register |
| <daw 10 aa aa dd dd> | write data into demodulator |
| <daw 12 aa aa dd dd> | write data into DSP |

#### 3.1.4.3. Read Telegrams

| | |
|---|---|
| <daw 11 aa aa <dar dd dd> | read data from demodulator |
| <daw 13 aa aa <dar dd dd> | read data from DSP |

#### 3.1.4.4. Examples

| | |
|---|---|
| <80 00 80 00> | RESET MSP statically |
| <80 00 00 00> | Clear RESET |
| <80 10 00 20 00 03> | Set demodulator to stand. $03_{hex}$ |
| <80 11 02 00 <81 dd dd> | Read STATUS |
| <80 12 00 08 01 20> | Set loudspeaker channel source to NICAM and Matrix to STEREO |

More examples of typical application protocols are listed in section “Programming Tips” on page 44.

### 3.2. Start-Up Sequence: Power-Up and I²C Controlling

After POWER ON or RESET (see Fig. 4–24), the IC is in an inactive state. All registers are in the reset position (see tables 3–5 and 3–6), the analog outputs are muted. The controller has to initialize all registers for which a non-default setting is necessary.

### 3.3. MSP 34x1G Programming Interface

#### 3.3.1. User Registers Overview

The MSP 34x1G is controlled by means of user registers. The complete list of all user registers is given in the following tables. The registers are partitioned into the Demodulator section (Subaddress $10_{hex}$ for writing, $11_{hex}$ for reading) and the Baseband Processing sections (Subaddress $12_{hex}$ for writing, $13_{hex}$ for reading).

Write and read registers are 16-bit wide, whereby the MSB is denoted bit [15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All write registers, except the demodulator write registers, are readable.

Unused parts of the 16-bit write registers must be zero. **Addresses not given in this table must not be written.**

For reasons of software compatibility to the MSP 34x0D, an Manual/Compatibility Mode is available. More read and write registers together with a detailed description of this mode can be found in the “Appendix B: Manual/Compatibility Mode” on page 83.

An overview of all MSP 34x1G Write Registers is shown in Table 3–5; all Read Registers are given in Table 3–6.

**Table 3–5:** List of MSP 34x1G Write Registers

| Write Register | Address (hex) | Bits | Description and Adjustable Range | Reset | See Page |
|---|---|---|---|---|---|
| **$I^2C$ Subaddress = $10_{hex}$ ; Registers are *not* readable** | | | | | |
| STANDARD SELECT | 00 20 | [15..0] | Initial Programming of complete Demodulator | 00 00 | 26 |
| MODUS | 00 30 | [15..0] | Demodulator, Automatic and $I^2S$ options | 00 00 | 28 |
| **$I^2C$ Subaddress = $12_{hex}$ ; Registers are *all* readable by using $I^2C$ Subaddress = $13_{hex}$** | | | | | |
| Volume loudspeaker channel | 00 00 | [15..8] | [+12 dB ... –114 dB, MUTE] | MUTE | 33 |
| Volume / Mode loudspeaker channel | | [7..0] | 1/8 dB Steps,<br>Reduce Volume / Tone Control / Compromise | $00_{hex}$ | |
| Balance loudspeaker channel [L/R] | 00 01 | [15..8] | [0...100 / 100% and 100 / 0...100%]<br>[–127...0 / 0 and 0 / –127...0 dB] | 100%/100% | 34 |
| Balance mode loudspeaker | | [7..0] | [Linear mode / logarithmic mode] | linear mode | |
| Bass loudspeaker channel | 00 02 | [15..8] | [+20 dB ... –12 dB] | 0 dB | 35 |
| Treble loudspeaker channel | 00 03 | [15..8] | [+15 dB ... –12 dB] | 0 dB | 36 |
| Loudness loudspeaker channel | 00 04 | [15..8] | [0 dB ... +17 dB] | 0 dB | 37 |
| Loudness filter characteristic | | [7..0] | [NORMAL, SUPER_BASS] | NORMAL | |
| Spatial effect strength loudspeaker ch. | 00 05 | [15..8] | [–100%...OFF...+100%] | OFF | 38 |
| Spatial effect mode/customize | | [7..0] | [SBE, SBE+PSE] | SBE+PSE | |
| Volume headphone channel | 00 06 | [15..8] | [+12 dB ... –114 dB, MUTE] | MUTE | 33 |
| Volume / Mode headphone channel | | [7..0] | 1/8 dB Steps, Reduce Volume / Tone Control | $00_{hex}$ | |
| Volume SCART1 output channel | 00 07 | [15..8] | [+12 dB ... –114 dB, MUTE] | MUTE | 39 |
| Loudspeaker source select | 00 08 | [15..8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 32 |
| Loudspeaker channel matrix | | [7..0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 32 |
| Headphone source select | 00 09 | [15..8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 32 |
| Headphone channel matrix | | [7..0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 32 |
| SCART1 source select | 00 0A | [15..8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 32 |
| SCART1 channel matrix | | [7..0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 32 |
| $I^2S$ source select | 00 0B | [15..8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 32 |
| $I^2S$ channel matrix | | [7..0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 32 |
| Quasi-peak detector source select | 00 0C | [15..8] | [FM/AM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM/AM | 32 |
| Quasi-peak detector matrix | | [7..0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 32 |
| Prescale SCART input | 00 0D | [15..8] | [$00_{hex}$ ... $7F_{hex}$] | $00_{hex}$ | 31 |
| Prescale FM/AM | 00 0E | [15..8] | [$00_{hex}$ ... $7F_{hex}$] | $00_{hex}$ | 30 |
| FM matrix | | [7..0] | [NO_MAT, GSTEREO, KSTEREO] | NO_MAT | 31 |
| Prescale NICAM | 00 10 | [15..8] | [$00_{hex}$ ... $7F_{hex}$] (MSP 3411G, MSP 3451G only) | $00_{hex}$ | 31 |
| Prescale $I^2S2$ | 00 12 | [15..8] | [$00_{hex}$ ... $7F_{hex}$] | $10_{hex}$ | 31 |
| ACB : SCART Switches a. D_CTR_I/O | 00 13 | [15..0] | Bits [15..0] | $00_{hex}$ | 40 |
| Beeper | 00 14 | [15..0] | [$00_{hex}$ ... $7F_{hex}$]/[$00_{hex}$ ... $7F_{hex}$] | $00/00_{hex}$ | 40 |
| Prescale $I^2S1$ | 00 16 | [15..8] | [$00_{hex}$ ... $7F_{hex}$] | $10_{hex}$ | 31 |
| Mode tone control | 00 20 | [15..8] | [BASS/TREBLE, EQUALIZER] | BASS/TREB | 35 |

**Table 3–5:** List of MSP 34x1G Write Registers, continued

| Write Register | Address (hex) | Bits | Description and Adjustable Range | Reset | See Page |
|---|---|---|---|---|---|
| Equalizer loudspeaker ch. band 1 | 00 21 | [15..8] | [+12 dB ... –12 dB] | 0 dB | 36 |
| Equalizer loudspeaker ch. band 2 | 00 22 | [15..8] | [+12 dB ... –12 dB] | 0 dB | 36 |
| Equalizer loudspeaker ch. band 3 | 00 23 | [15..8] | [+12 dB ... –12 dB] | 0 dB | 36 |
| Equalizer loudspeaker ch. band 4 | 00 24 | [15..8] | [+12 dB ... –12 dB] | 0 dB | 36 |
| Equalizer loudspeaker ch. band 5 | 00 25 | [15..8] | [+12 dB ... –12 dB] | 0 dB | 36 |
| Automatic Volume Correction | 00 29 | [15..8] | [off, on, decay time] | off | 34 |
| Subwoofer level adjust | 00 2C | [15..8] | [0 dB ... –30 dB, mute] | 0 dB | 39 |
| Subwoofer corner frequency | 00 2D | [15..8] | [50 Hz ... 400 Hz] | $00_{hex}$ | 39 |
| Subwoofer complementary high-pass | | [7..0] | [off, on] | off | 39 |
| Balance headphone channel [L/R] | 00 30 | [15..8] | [0...100 / 100% and 100 / 0...100%]<br>[–127...0 / 0 and 0 / –127...0 dB] | 100 %/100 % | 34 |
| Balance mode headphone | | [7..0] | [Linear mode / logarithmic mode] | linear mode | |
| Bass headphone channel | 00 31 | [15..8] | [+20 dB ... –12 dB] | 0 dB | 35 |
| Treble headphone channel | 00 32 | [15..8] | [+15 dB ... –12 dB] | 0 dB | 36 |
| Loudness headphone channel | 00 33 | [15..8] | [0 dB ... +17 dB] | 0 dB | 37 |
| Loudness filter characteristic | | [7..0] | [NORMAL, SUPER_BASS] | NORMAL | |
| Volume SCART2 output channel | 00 40 | [15..8] | [+12 dB ... –114 dB, MUTE] | $00_{hex}$ | 39 |
| SCART2 source select | 00 41 | [15..8] | [FM, NICAM, SCART, $I^2S1$, $I^2S2$] | FM | 32 |
| SCART2 channel matrix | | [7..0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 32 |
| Virtual Surround OFF/ON switch | 00 48 | [15..8] | [OFF/ON] | $00_{hex}$ | 41 |
| Virtual Surround spatial effect strength | 00 49 | [15..8] | [0% - 100%] | $00_{hex}$ | 41 |
| Virtual Surround 3D effect strength | 00 4A | [15..8] | [0% - 100%] | $00_{hex}$ | 41 |
| Virtual Surround mode | 00 4B | [15..0] | [PANORAMA/3D-PANORAMA] | $00_{hex}$ | 41 |
| Noise generator | 00 4D | [15..0] | [OFF/ON, Noise_L, Noise_C, Noise_R, Noise_S] | $00_{hex}$ | 42 |

**Table 3–6:** List of MSP 34x1G Read Registers

| Read Register | Address (hex) | Bits | Description and Adjustable Range | See Page |
|---|---|---|---|---|
| **$I^2C$ Subaddress = $11_{hex}$ ; Registers are *not* writable** | | | | |
| STANDARD RESULT | 00 7E | [15..0] | Result of Automatic Standard Detection (see Table 3–8) | 29 |
| STATUS | 02 00 | [15..0] | Monitoring of internal settings e.g. Stereo, Mono, Mute etc. . | 29 |
| **$I^2C$ Subaddress = $13_{hex}$ ; Registers are *not* writable** | | | | |
| Quasi peak readout left | 00 19 | [15..0] | [$00_{hex}$ ... $7FFF_{hex}$]16 bit two's complement | 43 |
| Quasi peak readout right | 00 1A | [15..0] | [$00_{hex}$ ... $7FFF_{hex}$]16 bit two's complement | 43 |
| MSP hardware version code | 00 1E | [15..8] | [$00_{hex}$ ... $FF_{hex}$] | 43 |
| MSP major revision code | | [7..0] | [$00_{hex}$ ... $FF_{hex}$] | 43 |
| MSP product code | 00 1F | [15..8] | [$00_{hex}$ ... $FF_{hex}$] | 43 |
| MSP ROM version code | | [7..0] | [$00_{hex}$ ... $FF_{hex}$] | 43 |

### 3.3.2. Description of User Registers

**Table 3–7:** Standard Codes for STANDARD SELECT register

| MSP Standard Code (Data in hex) | TV Sound Standard | Sound Carrier Frequencies in MHz | MSP 34x1G Version |
|---|---|---|---|
| **Automatic Standard Detection** | | | |
| 00 01 | Start Automatic Standard Detection | | all |
| **Standard Selection** | | | |
| 00 02 | M-Dual FM-Stereo | 4.5/4.724212 | 3401, -11, -21, -41, -51 |
| 00 03 | B/G -Dual FM-Stereo[1)] | 5.5/5.7421875 | 3401, -11, -51 |
| 00 04 | D/K1-Dual FM-Stereo[2)] | 6.5/6.2578125 | |
| 00 05 | D/K2-Dual FM-Stereo[2)] | 6.5/6.7421875 | |
| 00 06 | D/K -FM-Mono with HDEV3[3)], not detectable by Automatic Standard Detection,<br>HDEV3[3)] SAT-Mono (i.e. Eutelsat, s. Table 6–17) | 6.5 | |
| 00 07 | D/K3-Dual FM-Stereo | 6.5/5.7421875 | |
| 00 08 | B/G -NICAM-FM[1)] | 5.5/5.85 | 3411, -51 |
| 00 09 | L -NICAM-AM | 6.5/5.85 | |
| 00 0A | I -NICAM-FM | 6.0/6.552 | |
| 00 0B | D/K -NICAM-FM[2)] | 6.5/5.85 | |
| 00 0C | D/K -NICAM-FM with HDEV2[4)], not detectable by Automatic Standard Detection, for China | 6.5/5.85 | |
| 00 0D | D/K -NICAM-FM with HDEV3[3)], not detectable by Automatic Standard Detection, for China | 6.5/5.85 | |
| 00 20 | BTSC-Stereo | 4.5 | 3421, -31, -41, -51 |
| 00 21 | BTSC-Mono + SAP | | |
| 00 30 | M-EIA-J Japan Stereo | 4.5 | 3421, -41, -51 |
| 00 40 | FM-Stereo Radio | 10.7 | 3421, -31, -41, -51 |
| 00 50 | SAT-Mono (s. Table 6–17) | 6.5 | 3401, -11, -51 |
| 00 51 | SAT-Stereo (s. Table 6–17) | 7.02/7.20 | |
| 00 60 | SAT ADR (Astra Digital Radio) | 7.2 | |

[1)] In case of Automatic Sound Select, the B/G-codes $3_{hex}$ and $8_{hex}$ are equivalent.
[2)] In case of Automatic Sound Select, the D/K-codes $4_{hex}$, $5_{hex}$ and $B_{hex}$ are equivalent.
[3)] HDEV3: Max. FM deviation must not exceed 540 kHz
[4)] HDEV2: Max. FM deviation must not exceed 360 kHz

#### 3.3.2.1. STANDARD SELECT Register

The TV sound standard of the MSP 34x1G demodulator is determined by the STANDARD SELECT register. There are two ways to use the STANDARD SELECT register:

– Setting up the demodulator for a TV sound standard by sending the corresponding standard code with a single $I^2C$-Bus transmission.

– Starting the Automatic Standard Detection for terrestrial TV standards. This is the most comfortable way to set up the demodulator. Within 0.5 s, the detection and set-up of the actual TV sound standard is performed. The detected standard can be read out of the STANDARD RESULT register by the control processor. This feature is recommended for the primary set-up of a TV set. Outputs should be muted during Automatic Standard Detection.

The Standard Codes are listed in Table 3–7.

Selecting a TV sound standard via the STANDARD SELECT register initializes the demodulator. This includes: AGC, tuning frequency, band-pass filters, demodulation mode (FM, AM, or NICAM), carrier mute, deemphasis, and identification mode.

If a present sound standard is impossible for a specific MSP version, it switches to the analog mono sound of this standard. In that case stereo or bilingual processing will not be possible.

For a complete setup of the TV sound processing from analog IF input to the source selection, the transmissions as shown in Section 3.5. are necessary.

**Note:** The FM matrix is set automatically if Automatic Sound Select is active (MODUS[0]=1). In this case, the FM matrix will be initialized with “Sound A Mono”. During operation, the FM matrix will be automatically selected according to the actual identification information.

For reasons of software compatibility to the MSP 34x0D, a Manual/Compatibility mode is available. A detailed description of this mode can be found on page 83.

#### 3.3.2.2. Refresh of STANDARD SELECT Register

A general refresh of the STANDARD SELECT register is not allowed. However, the following method enables watching the MSP 34x1G “alive” status and detection of accidental resets (only versions A2 and later):

– After Power-on, bit[15] of CONTROL will be set; it must be read once to enable the reset-detection feature.

– Reading of the CONTROL register and checking the reset indicator bit[15] .

– If bit[15] is “0”, any refresh of the STANDARD SELECT register **is not allowed.**

– If bit[15] is “1”, indicating a reset, a refresh of the STANDARD SELECT register and all other MSPG registers is necessary.

### 3.3.2.3. STANDARD RESULT Register

If Automatic Standard Detection is selected in the STANDARD SELECT register, status and result of the Automatic Standard Detection process can be read out of the STANDARD RESULT register. The possible results are based on the mentioned Standard Code and are listed in Table 3–8.

In cases where no sound standard has been detected (no standard present, too much noise, strong interferers, etc.) the STANDARD RESULT register contains 00 $00_{hex}$. In that case, the controller has to start further actions (for example, set the standard according to a preference list or by manual input).

As long as the STANDARD RESULT register contains a value greater than 07 $FF_{hex}$, the Automatic Standard Detection is still active. During this period, the MODUS and STANDARD SELECT register must not be written. The STATUS register will be updated when the Automatic Standard Detection has finished.

If a present sound standard is impossible for a specific MSP version, it detects and switches to the analog mono sound of this standard.

Example:
The MSPs 3431G and 3441G will detect a B/G-NICAM signal as standard 3 and will switch to the analog FM-Mono sound.

**Table 3–8:** Results of the Automatic Standard Detection

| **Broadcasted Sound Standard** | **STANDARD RESULT Register** Read $007E_{hex}$ |
|---|---|
| Automatic Standard Detection could not find a sound standard | $0000_{hex}$ |
| B/G-FM | $0003_{hex}$ |
| B/G-NICAM | $0008_{hex}$ |
| I | $000A_{hex}$ |
| FM-Radio | $0040_{hex}$ |
| M-Korea<br>M-Japan<br>M-BTSC | $0002_{hex}$ (if MODUS[14,13]=00) |
| | $0020_{hex}$ (if MODUS[14,13]=01) |
| | $0030_{hex}$ (if MODUS[14,13]=10) |
| L-AM<br>D/K1<br>D/K2 | $0009_{hex}$ (if MODUS[12]=0) |
| | $0004_{hex}$ (if MODUS[12]=1) |
| L-NICAM<br>D/K-NICAM | $0009_{hex}$ (if MODUS[12]=0) |
| | $000B_{hex}$ (if MODUS[12]=1) |
| Automatic Standard Detection still active | $>07FF_{hex}$ |

### 3.3.2.4. Write Registers on I²C Subaddress $10_{hex}$

**Table 3–9:** Write Registers on I²C Subaddress $10_{hex}$

| Register Address | Function | Name |
|---|---|---|
| **STANDARD SELECTION** | | |
| 00 $20_{hex}$ | **STANDARD SELECTION Register**<br>Defines TV Sound or FM-Radio Standard<br>bit [15:0] 00 $01_{hex}$ start Automatic Standard Detection<br>00 $02_{hex}$ Standard Codes (see Table 3–7))<br>...<br>00 $60_{hex}$ | STANDARD_SEL |
| **MODUS** | | |
| 00 $30_{hex}$ | **MODUS Register**<br>General MSP 34x1G Options<br>bit [0] 0/1 off/on: Automatic Sound Select<br>bit [1] 0/1 disable/enable STATUS change indication by means of the digital I/O pin D_CTR_I/O_1<br>Necessary condition: MODUS[3] = 0 (active)<br>bit [2] 0 undefined, must be 0<br>bit [3] state of digital output pins D_CTR_I/O_0 and _1<br>0 active: D_CTR_I/O_0 and _1 are output pins<br>(can be set by means of the ACB register.<br>see also: MODUS[1])<br>1 tristate: D_CTR_I/O_0 and _1 are input pins<br>(level can be read out of STATUS[4,3])<br>bit [4] 0/1 active/tristate state of I²S output pins<br>bit [5] 0/1 master/slave mode of I²S interface (must be set to 0 (= Master) in case of NICAM mode)<br>bit [6] 0/1 Sony/Philips format of I²S word strobe<br>bit [7] 0/1 active/tristate state of audio clock output pin AUD_CL_OUT<br>bit [8] 0/1 ANA_IN_1+/ANA_IN_2+;<br>select analog sound IF input pin<br>bit [11:9] 0 undefined, must be 0<br>Preference in Automatic Standard Detection:<br>bit [12] detected 6.5 MHz carrier is interpreted as:[1)]<br>0 standard L (SECAM)<br>1 standard D/K1, D/K2 or D/K NICAM<br>bit [14:13] detected 4.5 MHz carrier is interpreted as:[1)]<br>0 standard M (Korea)<br>1 standard M (BTSC)<br>2 standard M (Japan)<br>3 carrier at 4.5 MHz is ignored (chroma carrier)<br>bit [15] 0 undefined, must be 0 | MODUS |

[1)] Valid at the next start of Automatic Standard Detection.

### 3.3.2.5. Read Registers on $I^2C$ Subaddress $11_{hex}$

**Table 3–10:** Read Registers on $I^2C$ Subaddress $11_{hex}$

| Register Address | Function | Name |
|---|---|---|
| **STANDARD RESULT** | | |
| 00 $7E_{hex}$ | **STANDARD RESULT Register**<br><br>Readback of the detected TV Sound or FM-Radio Standard<br><br>bit [15:0] 00 $00_{hex}$ Automatic Standard Detection could not find a sound standard<br>00 $02_{hex}$ MSP Standard Codes (see Table 3–8)<br>...<br>00 $40_{hex}$<br>>07 $FF_{hex}$ Automatic Standard Detection still active | STANDARD_RES |
| **STATUS** | | |
| 02 $00_{hex}$ | **STATUS Register**<br><br>Contains all user relevant internal information about the status of the MSP<br><br>bit [0] undefined<br><br>bit [1] 0 detected primary carrier (Mono or MPX carrier)<br>1 no primary carrier detected<br><br>bit [2] 0 detected secondary carrier (2nd A2 or SAP carrier)<br>1 no secondary carrier detected<br><br>bit [3] 0/1 low/high level of digital I/O pin D_CTR_I/O_0<br><br>bit [4] 0/1 low/high level of digital I/O pin D_CTR_I/O_1<br><br>bit [5,9] 00 analog sound standard (FM or AM) active<br>01 not obtainable<br>10 digital sound (NICAM) available (MSP 3411G and MSP 3451G only)<br>11 bad reception condition of digital sound (NICAM) due to:<br>a. high error rate<br>b. unimplemented sound code<br>c. data transmission only<br><br>bit [6] 0/1 mono/stereo indication<br><br>bit [7] 0/1 “1” indicates independent mono sound (only for NICAM on MSP 3411G and MSP 3451G)<br><br>bit [8] 0/1 “1” indicates bilingual sound mode or SAP present<br><br>bit [15:10] undefined<br><br>If STATUS change indication is activated by means of MODUS[1]: Each change in the STATUS register sets the digital I/O pin D_CTR_I/O_1 to high level. Reading the STATUS register resets D_CTR_I/O_1. | STATUS |

### 3.3.2.6. Write Registers on I²C Subaddress $12_{hex}$

**Table 3–11:** Write Registers on I²C Subaddress $12_{hex}$

| Register Address | Function | Name |
|---|---|---|
| **PREPROCESSING** | | |
| 00 $0E_{hex}$ | **FM/AM Prescale**<br>bit [15:8] $00_{hex}$ Defines the input prescale gain for the demodulated<br>... FM or AM signal<br>$7F_{hex}$<br>$00_{hex}$ off (RESET condition)<br><br>For all FM modes except satellite FM and AM-mode, the combinations of prescale value and FM deviation listed below lead to internal full scale.<br><br>FM mode<br>bit [15:8] $7F_{hex}$ 28 kHz FM deviation<br>$48_{hex}$ 50 kHz FM deviation<br>$30_{hex}$ 75 kHz FM deviation<br>$24_{hex}$ 100 kHz FM deviation<br>$18_{hex}$ 150 kHz FM deviation<br>$13_{hex}$ 180 kHz FM deviation (limit)<br><br>FM high deviation mode (HDEV2, MSP Standard Code = $C_{hex}$)<br>bit [15:8] $30_{hex}$ 150 kHz FM deviation<br>$14_{hex}$ 360 kHz FM deviation (limit)<br><br>FM very high deviation mode (HDEV3, MSP Standard Code = 6 and $D_{hex}$)<br>bit [15:8] $20_{hex}$ 450 kHz FM deviation<br>$1A_{hex}$ 540 kHz FM deviation (limit)<br><br>Satellite FM with adaptive deemphasis<br>bit [15:8] $10_{hex}$ recommendation<br><br>AM mode (MSP Standard Code = 9)<br>bit [15:8] $7C_{hex}$ recommendation for SIF input levels from 0.1 $V_{pp}$ to 0.8 $V_{pp}$<br><br>(Due to the AGC being switched on, the AM-output level remains stable and independent of the actual SIF-level in the mentioned input range) | PRE_FM |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| (continued)<br><br>00 $0E_{hex}$ | **FM Matrix Modes**<br><br>Defines the dematrix function for the demodulated FM signal<br><br>bit [7:0] $00_{hex}$ no matrix (used for bilingual and unmatrixed stereo sound)<br>$01_{hex}$ German stereo (Standard B/G)<br>$02_{hex}$ Korean stereo (also used for BTSC, EIA-J and FM Radio)<br>$03_{hex}$ sound A mono (left and right channel contain the mono sound of the FM/AM mono carrier)<br>$04_{hex}$ sound B mono<br><br>In case of **Automatic Sound Select**, the FM Matrix Mode is set automatically, i.e. the low-part of any $I^2C$ transmission to the register 00 $0E_{hex}$ is ignored.<br><br>To enable a **Forced Mono Mode** for all analog stereo systems by overriding the internal pilot or identification evaluation, the following steps must be transmitted:<br><br>1. MODUS with bit[0] = 0 (Automatic Sound Select off)<br>2. FM Presc./Matrix with FM Matrix = Sound A Mono (SAP: Sound B Mono)<br>3. Select FM/AM source channel, with channel matrix set to “Stereo” (transparent) | FM_MATRIX |
| 00 $10_{hex}$ | **NICAM Prescale**<br><br>Defines the input prescale value for the digital NICAM signal<br><br>bit [15:8] $00_{hex}$ ... $7F_{hex}$ prescale gain<br><br>examples:<br>$00_{hex}$ off<br>$20_{hex}$ 0 dB gain<br>$5A_{hex}$ 9 dB gain (recommendation)<br>$7F_{hex}$ +12 dB gain (maximum gain) | PRE_NICAM |
| 00 $16_{hex}$<br>00 $12_{hex}$ | **I2S1 Prescale**<br>**I2S2 Prescale**<br><br>Defines the input prescale value for digital $I^2S$ input signals<br><br>bit [15:8] $00_{hex}$ ... $7F_{hex}$ prescale gain<br><br>examples:<br>$00_{hex}$ off<br>$10_{hex}$ 0 dB gain (recommendation)<br>$7F_{hex}$ +18 dB gain (maximum gain) | PRE_I2S1<br>PRE_I2S2 |
| 00 $0D_{hex}$ | **SCART Input Prescale**<br><br>Defines the input prescale value for the analog SCART input signal<br><br>bit [15:8] $00_{hex}$ ... $7F_{hex}$ prescale gain<br><br>examples:<br>$00_{hex}$ off<br>$19_{hex}$ 0 dB gain (2 $V_{RMS}$ input leads to digital full scale)<br>Due to the Dolby requirements, this is the **maximum value** allowed to prohibit clipping of a 2 $V_{RMS}$ input signal.<br>$7F_{hex}$ +14 dB gain (400 $mV_{RMS}$ input leads to digital full scale) | PRE_SCART |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **SOURCE SELECT AND OUTPUT CHANNEL MATRIX** | | |
| 00 $08_{hex}$<br>00 $09_{hex}$<br>00 $0A_{hex}$<br>00 $41_{hex}$<br>00 $0B_{hex}$<br>00 $0C_{hex}$ | **Source for:**<br>**Loudspeaker Output**<br>**Headphone Output**<br>**SCART1 DA Output**<br>**SCART2 DA Output**<br>**$I^2S$ Output**<br>**Quasi-Peak Detector**<br><br>bit [15:8] 0 “FM/AM”: demodulated FM or AM mono signal<br>1 “Stereo or A/B”: demodulator Stereo or A/B signal (in manual mode, this source is identical to the NICAM source in the MSP 3410D)<br>3 “Stereo or A”: demodulator Stereo Sound or Language A (only defined for Automatic Sound Select)<br>4 “Stereo or B”: demodulator Stereo Sound or Language B (only defined for Automatic Sound Select)<br>2 SCART input<br>5 $I^2S1$ input<br>6 $I^2S2$ input<br><br>For demodulator sources, see Table 2–2. | SRC_MAIN<br>SRC_AUX<br>SRC_SCART1<br>SRC_SCART2<br>SRC_I2S<br>SRC_QPEAK |
| 00 $08_{hex}$<br>00 $09_{hex}$<br>00 $0A_{hex}$<br>00 $41_{hex}$<br>00 $0B_{hex}$<br>00 $0C_{hex}$ | **Matrix Mode for:**<br>**Loudspeaker Output**<br>**Headphone Output**<br>**SCART1 DA Output**<br>**SCART2 DA Output**<br>**$I^2S$ Output**<br>**Quasi-Peak Detector**<br><br>bit [7:0] $00_{hex}$ Sound A Mono (or Left Mono)<br>$10_{hex}$ Sound B Mono (or Right Mono)<br>$20_{hex}$ Stereo (transparent mode)<br>$30_{hex}$ Mono (sum of left and right inputs divided by 2)<br>special modes are available (see Section 6.5.1. on page 95)<br><br>In Automatic Sound Select mode, the demodulator source channels are set according to Table 2–2. Therefore, the matrix modes of the corresponding output channels should be set to “Stereo” (transparent). | MAT_MAIN<br>MAT_AUX<br>MAT_SCART1<br>MAT_SCART2<br>MAT_I2S<br>MAT_QPEAK |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **LOUDSPEAKER AND HEADPHONE PROCESSING** | | |
| 00 $00_{hex}$<br>00 $06_{hex}$ | **Volume Loudspeaker**<br>**Volume Headphone**<br><br>bit [15:8] volume table with 1 dB step size<br>$7F_{hex}$ +12 dB (maximum volume)<br>$7E_{hex}$ +11 dB<br>...<br>$74_{hex}$ +1 dB<br>$73_{hex}$ 0 dB<br>$72_{hex}$ –1 dB<br>...<br>$02_{hex}$ –113 dB<br>$01_{hex}$ –114 dB<br>$00_{hex}$ Mute (reset condition)<br>$FF_{hex}$ Fast Mute (needs about 75 ms until the signal is completely ramped down)<br><br>bit [7:5] higher resolution volume table<br>0 +0 dB<br>1 +0.125 dB increase in addition to the volume table<br>...<br>7 +0.875 dB increase in addition to the volume table<br><br>bit [4] 0 must be set to 0<br><br>bit [3:0] clipping mode<br>0 reduce volume<br>1 reduce tone control<br>2 compromise mode<br><br>With large scale input signals, positive volume settings may lead to signal clipping.<br><br>The MSP 34x1G loudspeaker and headphone volume function is divided into a digital and an analog section. With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. To turn volume on again, the volume step that has been used before Fast Mute was activated must be transmitted.<br><br>If the clipping mode is set to “Reduce Volume”, the following rule is used: To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB.<br><br>If the clipping mode is “Reduce Tone Control”, the bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB.<br><br>If the clipping mode is “Compromise Mode”, the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced half and half, where amplification together with volume exceeds 12 dB.<br><br>Example: Vol.: +6 dB / Bass: +9 dB / Treble: +5 dB<br>Red. Volume 3 / 9 / 5<br>Red. Tone Con. 6 / 6 / 5<br>Compromise 4.5 / 7.5 / 5 | VOL_MAIN<br>VOL_AUX |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| 00 $29_{hex}$ | **Automatic Volume Correction (AVC) Loudspeaker Channel**<br><br>bit [15:12] $00_{hex}$ AVC off (and reset internal variables)<br>$08_{hex}$ AVC on<br><br>bit [11:8] $08_{hex}$ 8 sec decay time<br>$04_{hex}$ 4 sec decay time<br>$02_{hex}$ 2 sec decay time<br>$01_{hex}$ 20 ms decay time (intended for quick adaptation to the average volume level after channel change)<br><br>**Note:** To reset the internal variables, the AVC should be switched off and then on again during any channel or source change. For standard applications, the recommended decay time is 4 sec.<br><br>**Note:** AVC should not be used in any Dolby Prologic mode (with DPL 35xx), except in PANORAMA or 3D-PANORAMA mode, when only the loudspeaker output is active. | AVC |
| 00 $01_{hex}$<br>00 $30_{hex}$ | **Balance Loudspeaker Channel**<br>**Balance Headphone Channel**<br><br>bit [3:0] Balance Mode<br>$0_{hex}$ linear<br>$1_{hex}$ logarithmic<br><br>bit [15:8] Linear Mode<br>$7F_{hex}$ Left muted, Right 100%<br>$7E_{hex}$ Left 0.8%, Right 100%<br>...<br>$01_{hex}$ Left 99.2%, Right 100%<br>$00_{hex}$ Left 100%, Right 100%<br>$FF_{hex}$ Left 100%, Right 99.2%<br>...<br>$82_{hex}$ Left 100%, Right 0.8%<br>$81_{hex}$ Left 100%, Right muted<br><br>bit [15:8] Logarithmic Mode<br>$7F_{hex}$ Left –127 dB, Right 0 dB<br>$7E_{hex}$ Left –126 dB, Right 0 dB<br>...<br>$01_{hex}$ Left –1 dB, Right 0 dB<br>$00_{hex}$ Left 0 dB, Right 0 dB<br>$FF_{hex}$ Left 0 dB, Right –1 dB<br>...<br>$81_{hex}$ Left 0 dB, Right –127 dB<br>$80_{hex}$ Left 0 dB, Right –128 dB<br><br>Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected. | BAL_MAIN<br>BAL_AUX |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| 00 $20_{hex}$ | **Tone Control Mode Loudspeaker Channel**<br><br>bit [15:8] $00_{hex}$ bass and treble is active<br>$FF_{hex}$ equalizer is active<br><br>Defines whether Bass/Treble or Equalizer is activated for the loudspeaker channel. Bass and Equalizer cannot work simultaneously. If Equalizer is used, Bass, and Treble coefficients must be set to zero and vice versa. | TONE_MODE |
| 00 $02_{hex}$<br>00 $31_{hex}$ | **Bass Loudspeaker Channel**<br>**Bass Headphone Channel**<br><br>bit [15:8] normal range<br>$60_{hex}$ +12 dB<br>$58_{hex}$ +11 dB<br>...<br>$08_{hex}$ +1 dB<br>$00_{hex}$ 0 dB<br>$F8_{hex}$ –1 dB<br>...<br>$A8_{hex}$ –11 dB<br>$A0_{hex}$ –12 dB<br>bit [15:8] extended range<br>$7F_{hex}$ +20 dB<br>$78_{hex}$ +18 dB<br>$70_{hex}$ +16 dB<br>$68_{hex}$ +14 dB<br><br>Higher resolution is possible: an LSB step in the normal range results in a gain step of about 1/8 dB, in the extended range about 1/4 dB.<br><br>With positive bass settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain. | BASS_MAIN<br>BASS_AUX |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| 00 $03_{hex}$<br>00 $32_{hex}$ | **Treble Loudspeaker Channel**<br>**Treble Headphone Channel**<br><br>bit [15:8] $78_{hex}$ +15 dB<br>$70_{hex}$ +14 dB<br>...<br>$08_{hex}$ +1 dB<br>$00_{hex}$ 0 dB<br>$F8_{hex}$ –1 dB<br>...<br>$A8_{hex}$ –11 dB<br>$A0_{hex}$ –12 dB<br><br>Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB.<br><br>With positive treble settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain. | TREB_MAIN<br>TREB_AUX |
| 00 $21_{hex}$<br>00 $22_{hex}$<br>00 $23_{hex}$<br>00 $24_{hex}$<br>00 $25_{hex}$ | **Equalizer Loudspeaker Channel Band 1 (below 120 Hz)**<br>**Equalizer Loudspeaker Channel Band 2 (center: 500 Hz)**<br>**Equalizer Loudspeaker Channel Band 3 (center: 1.5 kHz)**<br>**Equalizer Loudspeaker Channel Band 4 (center: 5 kHz)**<br>**Equalizer Loudspeaker Channel Band 5 (above: 10 kHz)**<br><br>bit [15:8] $60_{hex}$ +12 dB<br>$58_{hex}$ +11 dB<br>...<br>$08_{hex}$ +1 dB<br>$00_{hex}$ 0 dB<br>$F8_{hex}$ –1 dB<br>...<br>$A8_{hex}$ –11 dB<br>$A0_{hex}$ –12 dB<br><br>Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB.<br><br>With positive equalizer settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain. | EQUAL_BAND1<br>EQUAL_BAND2<br>EQUAL_BAND3<br>EQUAL_BAND4<br>EQUAL_BAND5 |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| 00 $04_{hex}$<br>00 $33_{hex}$ | **Loudness Loudspeaker Channel**<br>**Loudness Headphone Channel**<br><br>bit [15:8] Loudness Gain<br>$44_{hex}$ +17 dB<br>$40_{hex}$ +16 dB<br>...<br>$04_{hex}$ +1 dB<br>$00_{hex}$ 0 dB<br><br>bit [7:0] Loudness Mode<br>$00_{hex}$ normal (constant volume at 1 kHz)<br>$04_{hex}$ Super Bass (constant volume at 2 kHz)<br><br>Higher resolution of Loudness Gain is possible: An LSB step results in a gain step of about 1/4 dB.<br><br>Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1-kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain.<br><br>The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz. | LOUD_MAIN<br>LOUD_AUX |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| 00 $05_{hex}$ | **Spatial Effects Loudspeaker Channel**<br><br>bit [15:8] Effect Strength<br>$7F_{hex}$ Enlargement 100%<br>$3F_{hex}$ Enlargement 50%<br>...<br>$01_{hex}$ Enlargement 1.5%<br>$00_{hex}$ Effect off<br>$FF_{hex}$ reduction 1.5%<br>...<br>$C0_{hex}$ reduction 50%<br>$80_{hex}$ reduction 100%<br><br>bit [7:4] Spatial Effect Mode<br>$0_{hex}$ Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)<br>$2_{hex}$ Stereo Basewidth Enlargement (SBE) only. (Mode B)<br><br>bit [3:0] Spatial Effect High-Pass Gain<br>$0_{hex}$ max. high-pass gain<br>$2_{hex}$ 2/3 high-pass gain<br>$4_{hex}$ 1/3 high-pass gain<br>$6_{hex}$ min. high-pass gain<br>$8_{hex}$ automatic<br><br>Spatial effects **should not be used** together with 3D-PANORAMA or PANORAMA.<br><br>There are several spatial effect modes available:<br><br>In mode A (low byte = $00_{hex}$), the spatial effect depends on the source mode. If the incoming signal is mono, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended.<br><br>In mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.<br><br>It is worth mentioning, that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of $0_{hex}$ yields a flat response for center signals (L = R), but a high-pass function for L or R only signals. A value of $6_{hex}$ has a flat response for L or R only signals, but a low-pass function for center signals. By using $8_{hex}$, the frequency response is automatically adapted to the sound material by choosing an optimal high-pass gain. | SPAT_MAIN |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **SUBWOOFER OUTPUT CHANNEL** | | |
| 00 $2C_{hex}$ | **Subwoofer Level Adjustment**<br><br>bit [15:8] $00_{hex}$ 0 dB<br>$FF_{hex}$ –1 dB<br>...<br>$E3_{hex}$ –29 dB<br>$E2_{hex}$ –30 dB<br>...<br>$80_{hex}$ Mute | SUBW_LEVEL |
| 00 $2D_{hex}$ | **Subwoofer Corner Frequency**<br><br>bit [15:8] 5...40 corner frequency in 10-Hz steps (range: 50...400 Hz)<br><br>**Subwoofer Complementary High-Pass Filter**<br>bit [7:0] $00_{hex}$ loudspeaker channel unfiltered<br>$01_{hex}$ a complementary high-pass is processed in the loudspeaker output channel | SUBW_FREQ<br><br>SUBW_HP |
| **SCART OUTPUT CHANNEL** | | |
| 00 $07_{hex}$<br>00 $40_{hex}$ | **Volume SCART1 Output Channel**<br>**Volume SCART2 Output Channel**<br><br>bit [15:8] volume table with 1 dB step size<br>$7F_{hex}$ +12 dB (maximum volume)<br>$7E_{hex}$ +11 dB<br>...<br>$74_{hex}$ +1 dB<br>$73_{hex}$ 0 dB<br>$72_{hex}$ –1 dB<br>...<br>$02_{hex}$ –113 dB<br>$01_{hex}$ –114 dB<br>$00_{hex}$ Mute (reset condition)<br>bit [7:5] higher resolution volume table<br>0 +0 dB<br>1 +0.125 dB increase in addition to the volume table<br>...<br>7 +0.875 dB increase in addition to the volume table<br>bit [4:0] $01_{hex}$ this must be $01_{hex}$ | VOL_SCART1<br>VOL_SCART2 |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **SCART SWITCHES AND DIGITAL I/O PINS** | | |
| 00 $13_{hex}$ | **ACB Register**<br><br>Defines the level of the digital output pins and the position of the SCART switches<br><br>bit [15] 0/1 low/high of digital output pin D_CTR_I/O_0 (MODUS[3]=0)<br><br>bit [14] 0/1 low/high of digital output pin D_CTR_I/O_1 (MODUS[3]=0)<br><br>bit [13:5] SCART DSP Input Select<br>xxxx00xx0 SCART1 to DSP input (RESET position)<br>xxxx01xx0 MONO to DSP input (Sound A Mono must be selected in the channel matrix mode for the corresponding output channels)<br>xxxx10xx0 SCART2 to DSP input<br>xxxx11xx0 SCART3 to DSP input<br>xxxx00xx1 SCART4 to DSP input<br>xxxx11xx1 mute DSP input<br><br>bit [13:5] SCART1 Output Select<br>xx00xxx0x SCART3 input to SCART1 output (RESET position)<br>xx01xxx0x SCART2 input to SCART1 output<br>xx10xxx0x MONO input to SCART1 output<br>xx11xxx0x SCART1 DA to SCART1 output<br>xx00xxx1x SCART2 DA to SCART1 output<br>xx01xxx1x SCART1 input to SCART1 output<br>xx10xxx1x SCART4 input to SCART1 output<br>xx11xxx1x mute SCART1 output<br><br>bit [13:5] SCART2 Output Select<br>00xxxx0xx SCART1 DA to SCART2 output (RESET position)<br>01xxxx0xx SCART1 input to SCART2 output<br>10xxxx0xx MONO input to SCART2 output<br>00xxxx1xx SCART2 DA to SCART2 output<br>01xxxx1xx SCART2 input to SCART2 output<br>10xxxx1xx SCART3 input to SCART2 output<br>11xxxx1xx SCART4 input to SCART2 output<br>11xxxx0xx mute SCART2 output<br><br>The RESET position becomes active at the time of the first write transmission on the control bus to the audio processing part. By writing to the ACB register first, the RESET state can be redefined. | ACB_REG |
| **BEEPER** | | |
| 00 $14_{hex}$ | **Beeper Volume and Frequency**<br><br>bit [15:8] Beeper Volume<br>$00_{hex}$ off<br>$7F_{hex}$ maximum volume<br><br>bit [7:0] Beeper Frequency<br>$01_{hex}$ 16 Hz (lowest)<br>$40_{hex}$ 1 kHz<br>$FF_{hex}$ 4 kHz | BEEPER |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **VIRTUAL SURROUND PROCESSING** | | |
| 00 $48_{hex}$ | **Virtual Surround OFF/ON Switch**<br><br>bit [15:8]<br>$00_{hex}$ virtual surround sound off (normal baseband processing)<br>$01_{hex}$ virtual surround processing<br><br>bit [7:0] $00_{hex}$ must be 0<br><br>Be sure to switch off Spatial Effects Loudspeaker Channel (register $0005_{hex}$) if 3D-PANORAMA is in use. | VIRT_ON |
| 00 $49_{hex}$ | **Virtual Surround Spatial Effects**<br><br>bit [15:8] Spatial Effect Strength<br>$7F_{hex}$ Enlargement 100%<br>$3F_{hex}$ Enlargement 50%<br>...<br>$01_{hex}$ Enlargement 1.5%<br>$00_{hex}$ Effect off<br><br>bit [7:0] $00_{hex}$ must be 0<br><br>Increases the perceived basewidth of the reproduced left and right front channels. **Recommended value: 50% = $40_{hex}$**. In contrast to the spatial effect for the loudspeaker channel, the surround spatial effect is optimized for virtual surround. | VIRT_SPAT |
| 00 $4A_{hex}$ | **Virtual Surround 3D Effect Strength**<br><br>bit [15:8] Virtual Surround Effect Strength<br>$7F_{hex}$ Effect 100%<br>$3F_{hex}$ Effect 50%<br>...<br>$01_{hex}$ Effect 1.5%<br>$00_{hex}$ Effect off<br><br>bit [7:0] $00_{hex}$ must be 0<br><br>Strength of the surround effect in PANORAMA or 3D-PANORAMA mode. **Recommended value: 66% = $54_{hex}$**. | VIRT_3DEFF |
| 00 $4B_{hex}$ | **Virtual Surround Mode**<br><br>bit [15:8] $00_{hex}$ must be 0<br><br>bit [7:0] $50_{hex}$ PANORAMA virtualizer<br>$60_{hex}$ 3D-PANORAMA virtualizer | VIRT_MODE |

**Table 3–11:** Write Registers on $I^2C$ Subaddress $12_{hex}$, continued

| Register Address | Function | Name |
|---|---|---|
| **NOISE GENERATOR** | | |
| 00 $4D_{hex}$ | **Noise Generator**<br><br>bit [15:8] $00_{hex}$ Noise generator off<br>$80_{hex}$ Noise generator on<br><br>bit [7:0] $A0_{hex}$ Noise on left channel<br>$B0_{hex}$ Noise on center channel<br>$C0_{hex}$ Noise on right channel<br>$D0_{hex}$ Noise on surround channel<br><br>Determines the active channel for the noise generator. | NOISE_CHAN |

### 3.3.2.7. Read Registers on $I^2C$ Subaddress $13_{hex}$

**Table 3–12:** Read Registers on $I^2C$ Subaddress $13_{hex}$

| Register Address | Function | Name |
|---|---|---|
| **QUASI-PEAK DETECTOR READOUT** | | |
| 00 $19_{hex}$<br>00 $1A_{hex}$ | **Quasi-Peak Detector Readout Left**<br>**Quasi-Peak Detector Readout Right**<br><br>bit [15..0] $0_{hex}$... $7FFF_{hex}$ values are 16 bit two's complement (only positive) | QPEAK_L<br>QPEAK_R |
| **MSP 34X1G VERSION READOUT REGISTERS** | | |
| 00 $1E_{hex}$ | **MSP Hardware Version Code**<br><br>bit [15..8] $01_{hex}$ MSP 34x1G - A1<br><br>A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint.<br><br>**MSP Major Revision Code**<br><br>bit [7..0] $07_{hex}$ MSP 34x1G - A1<br><br>The major revision code of the MSP 34x1G is 7. | MSP_HARD<br><br><br><br><br><br>MSP_REVISION |
| 00 $1F_{hex}$ | **MSP Product Code**<br><br>bit [15..8] $01_{hex}$ MSP 3401G - A1<br>$0B_{hex}$ MSP 3411G - A1<br>$1F_{hex}$ MSP 3431G - A1<br>$29_{hex}$ MSP 3441G - A1<br>$33_{hex}$ MSP 3451G - A1<br><br>By means of the MSP-Product Code, the control processor is able to decide which TV sound standards have to be considered.<br><br>**MSP ROM Version Code**<br><br>bit [7..0] $41_{hex}$ MSP 34x1G - A1<br>$42_{hex}$ MSP 34x1G - A2<br><br>A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new MSP 34x1G versions according to this number.<br><br>To avoid compatibility problems with MSP 3410B and MSP 34x0D, an offset of $40_{hex}$ is added to the ROM version code of the chip's imprint. | MSP_PRODUCT<br><br><br><br><br><br><br><br><br><br><br><br>MSP_ROM |

### 3.4. Programming Tips

This section describes the preferred method for initializing the MSP 34x1G. The initialization is grouped into four sections: analog signal path, demodulator input, input processing for SCART and I²S, and output processing. See Fig. 2–1 on page 9 for a complete signal flow.

#### SCART Signal Path

1. Select analog input for the SCART baseband processing (SCART DSP Input Select) by means of the ACB register.
2. Select the source for each analog SCART output (SCART Output Select) by means of the ACB register.

#### Demodulator Input

For a complete setup of the TV sound processing from analog IF input to the source selection, the following steps must be performed:

1. Set MODUS register to the preferred mode and Sound IF input.
2. Choose preferred prescale (FM and NICAM) values.
3. Write STANDARD SELECT register.

If Automatic Sound Select is not active, the following step has to be done repeatedly:

4. Choose FM matrix according to the sound mode indicated in the STATUS register.

#### SCART and I²S Inputs

1. Select preferred prescale for SCART.
2. Select preferred prescale for I²S inputs (set to 0 dB after RESET).

#### Output Channels

1. Select the source channel and matrix for each output channel.
2. Set audio baseband processing.
3. Select volume for each output channel.

### 3.5. Examples of Minimum Initialization Codes

Initialization of the MSP 34x1G according to these listings reproduces sound of the selected standard on the loudspeaker output. All numbers are hexadecimal. The examples have the following structure:

1. Perform an I²C controlled reset of the IC.
2. Write MODUS register (with Automatic Sound Select).
3. Set Source Selection for loudspeaker channel (with matrix set to STEREO).
4. Set Prescale (FM and/or NICAM and dummy FM matrix).
5. Write STANDARD SELECT register.
6. Set Volume loudspeaker channel to 0 dB.

#### 3.5.1. SCART1 Input to Loudspeaker in Stereo Sound

```
<80 00 00 00 80 00>     // reset
<80 00 00 00 00 00>
<80 12 00 08 02 20>     // source loudspeaker = scart, stereo
<80 12 00 0d 19 00>     // prescale scart
<80 12 00 00 73 00>     // volume main = 0dB
```

#### 3.5.2. SCART1 Input to Loudspeaker in 3D-PANORAMA Sound

```
<80 00 00 00 80 00>     // reset
<80 00 00 00 00 00>
<80 12 00 08 02 20>     // source loudspeaker = scart, stereo
<80 12 00 0d 19 00>     // prescale scart
<80 12 00 00 73 00>     // volume main = 0dB
<80 12 00 48 01 00>     // virtual surround sound: on
<80 12 00 49 40 00>     // Surround spatial effect = 50%
<80 12 00 4a 54 00>     // panorama sound effect = 66%
<80 12 00 4b 00 60>     // Surround mode = 3d_panorama
<80 12 00 4d 00 00>     // Noise Sequencer = off
```

#### 3.5.3. Noise Sequencer for 3D-PANORAMA Sound

```
// switch into 3D-PANORAMA sound (s.a.). Then:
<80 12 00 4d 80 a0>     // noise L
[wait for 2 seconds]
<80 12 00 4d 80 b0>     // noise C
[wait for 2 seconds]
<80 12 00 4d 80 c0>     // noise R
[wait for 2 seconds]
<80 12 00 4d 80 d0>     // noise S
[wait for 2 seconds]

// switch back to normal operation
<80 12 00 4d 00 00>     // Noise Sequencer = off
```

### 3.5.4. B/G-FM (A2 or NICAM)

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24hex,
                          FM-Matrix = MONO/SOUNDA
<80 12 00 10 00 5A>    // NICAM-Prescale = 5A(hex)
<80 10 00 20 00 03>    // Standard Select: A2 B/G or NICAM B/G
          or
<80 10 00 20 00 08>
<80 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

### 3.5.5. BTSC-Stereo

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24(hex),
                          FM-Matrix = Sound A Mono
<80 10 00 20 00 20>    // Standard Select: BTSC-STEREO
<80 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

### 3.5.6. BTSC-SAP with SAP at Loudspeaker Channel

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 04 20>    // Source Sel. = (St or B) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24(hex),
                          FM-Matrix = Sound A Mono
<80 10 00 20 00 21>    // Standard Select: BTSC-SAP
<80 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

### 3.5.7. FM-Stereo Radio

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24(hex),
                          FM-Matrix = Sound A Mono
<80 10 00 20 00 40>    // Standard Select: FM-STEREO-RADIO
<80 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

### 3.5.8. Automatic Standard Detection

A detailed software flow diagram is shown in Fig. 3–2 on page 46.

```
<80 00 80 00>          // Softreset
<80 00 00 00>
<80 10 00 30 20 03>    // MODUS-Register: Automatic = on
<80 12 00 08 03 20>    // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03>    // FM/AM-Prescale = 24(hex),
                          FM-Matrix = Sound A Mono
<80 12 00 10 00 5A>    // NICAM-Prescale = 5A(hex)
<80 10 00 20 00 01>    // Standard Select:
                          Automatic Standard Detection
// Wait till STANDARD RESULT contains a value ≤ 07FF
// IF STANDARD RESULT contains 0000
                       // do some error handling
// ELSE
<80 12 00 00 73 00>    // Loudspeaker Volume 0 dB
```

### 3.5.9. Software Flow for Interrupt driven STATUS Check

A detailed software flow diagram is shown in Fig. 3–2 on page 46.

If the D_CTR_I/O_1 pin of the MSP 34x1G is connected to an interrupt input pin of the controller, the following interrupt handler can be applied to be automatically called with each status change of the MSP 34x1G. The interrupt handler may adjust the TV display according to the new status information.

Interrupt Handler:

```
<80 11 02 00 <81 dd dd>  // Read STATUS
// adjust TV display with given status information
// Return from Interrupt
```

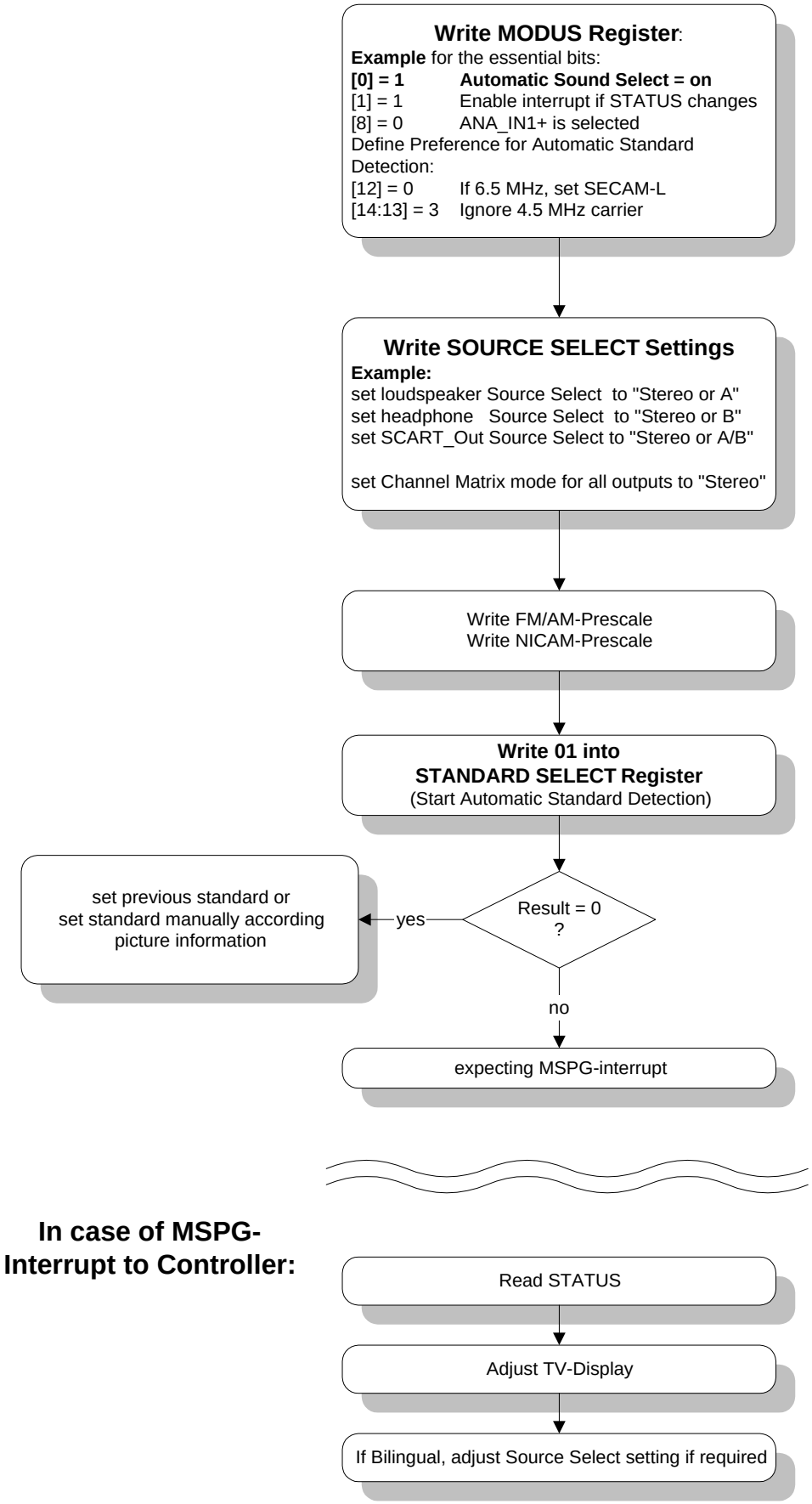



**Fig. 3–2:** Software flow diagram for a Minimum demodulator setup for a European Multistandard TV set applying the Automatic Sound Select feature

## 4. Specifications

### 4.1. Outline Dimensions

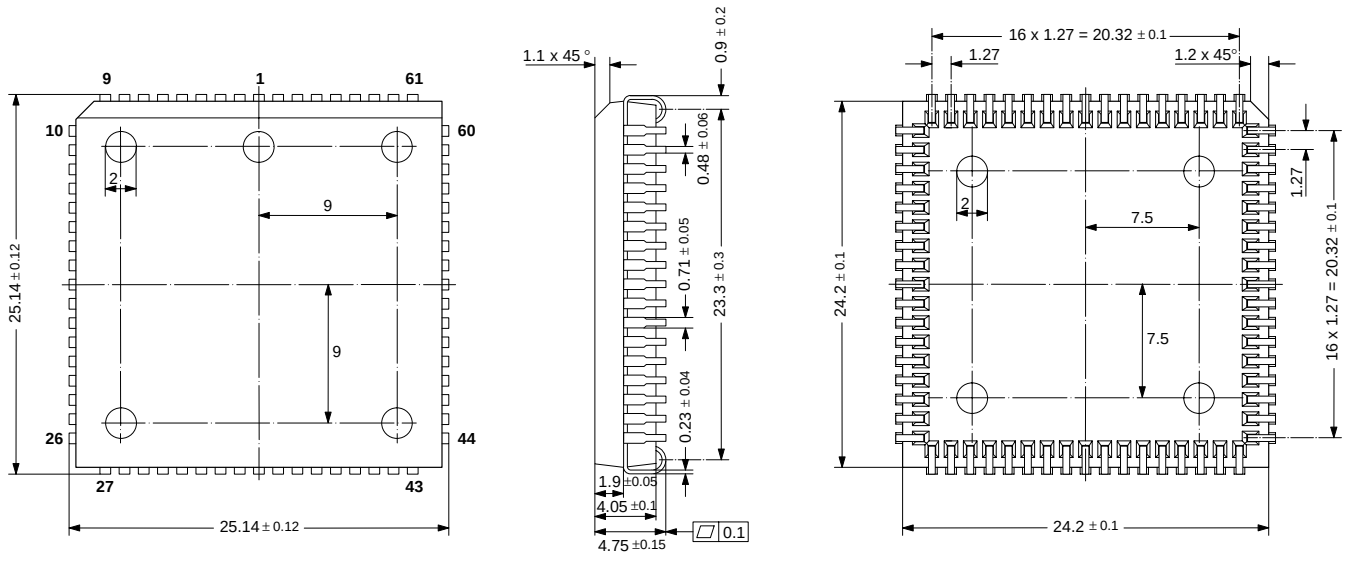



**Fig. 4–1:**
68-Pin Plastic Leaded Chip Carrier Package
**(PLCC68)**
Weight approximately 4.8 g
Dimensions in mm

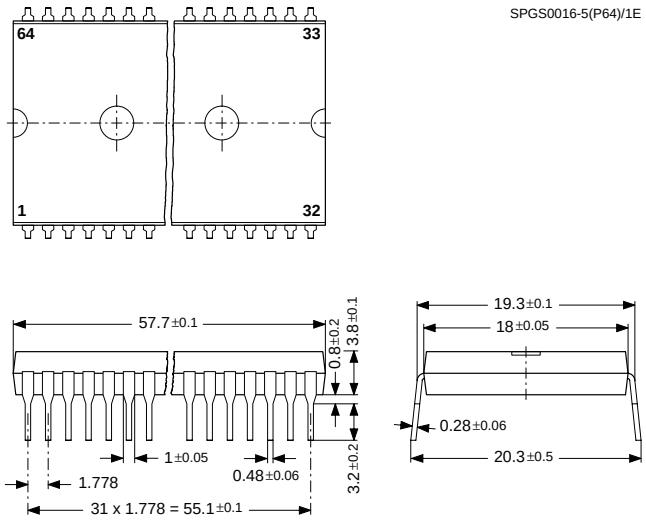



**Fig. 4–2:**
64-Pin Plastic Shrink Dual-Inline Package
**(PSDIP64)**
Weight approximately 9.0 g
Dimensions in mm

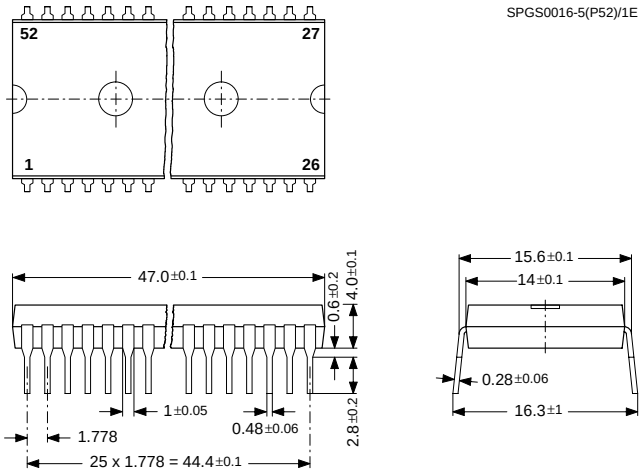



**Fig. 4–3:**
52-Pin Plastic Shrink Dual-Inline Package
**(PSDIP52)**
Weight approximately 5.5 g
Dimensions in mm

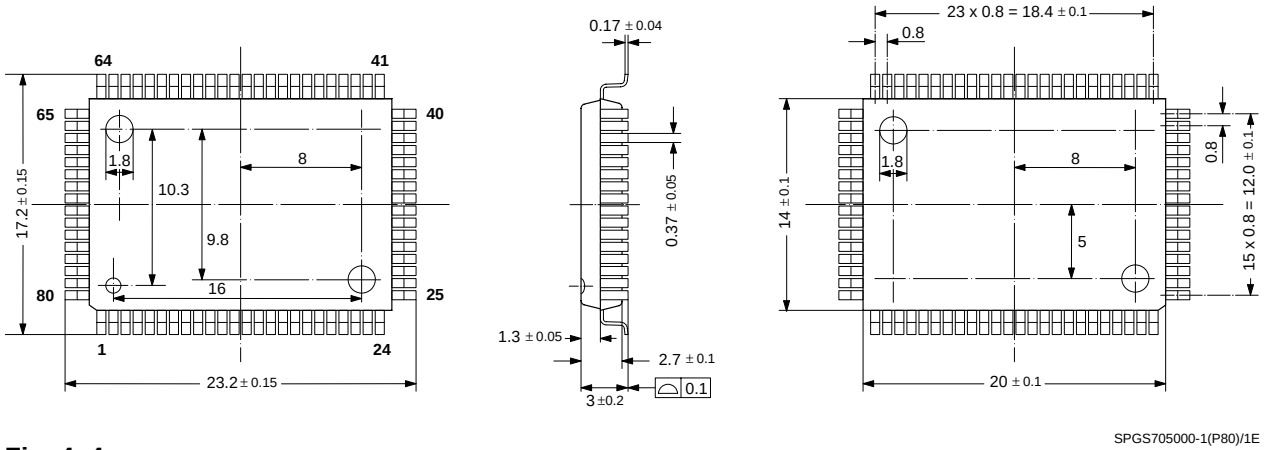



**Fig. 4–4:**
80-Pin Plastic Quad Flat Pack
**(PQFP80)**
Weight approximately 1.61 g
Dimensions in mm

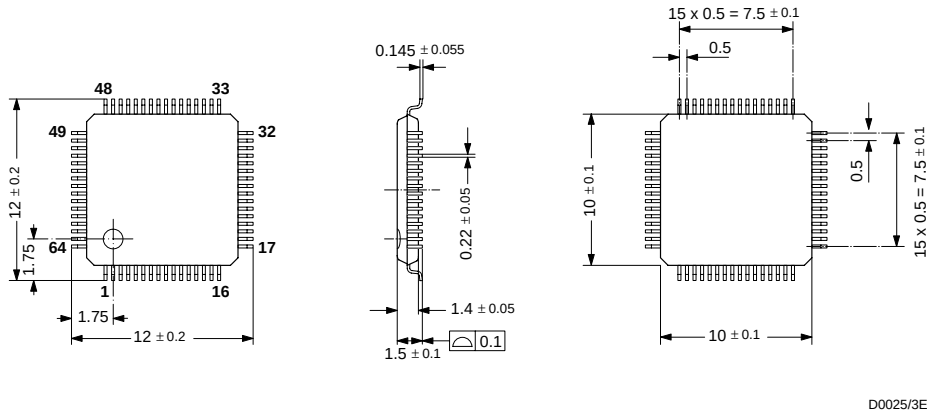



**Fig. 4–5:**
64-Pin Plastic Low-Profile Quad Flat Pack
**(PLQFP64)**
Weight approximately 3.5 g
Dimensions in mm

### 4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram
DVSS: if not used, connect to DVSS
AHVSS: connect to AHVSS

| Pin No. | | | | | Pin Name | Type | Connection (if not used) | Short Description |
|---|---|---|---|---|---|---|---|---|
| PLCC 68-pin | PSDIP 64-pin | PSDIP 52-pin | PQFP 80-pin | PLQFP 64-pin | | | | |
| 1 | 16 | 14 | 9 | 8 | ADR_WS | OUT | LV | ADR word strobe |
| 2 | – | – | – | – | NC | | LV | Not connected |
| 3 | 15 | 13 | 8 | 7 | ADR_DA | OUT | LV | ADR data output |
| 4 | 14 | 12 | 7 | 6 | I2S_DA_IN1 | IN | LV | $I^2S$1 data input |
| 5 | 13 | 11 | 6 | 5 | I2S_DA_OUT | OUT | LV | $I^2S$ data output |
| 6 | 12 | 10 | 5 | 4 | I2S_WS | IN/OUT | LV | $I^2S$ word strobe |
| 7 | 11 | 9 | 4 | 3 | I2S_CL | IN/OUT | LV | $I^2S$ clock |
| 8 | 10 | 8 | 3 | 2 | I2C_DA | IN/OUT | OBL | $I^2C$ data |
| 9 | 9 | 7 | 2 | 1 | I2C_CL | IN/OUT | OBL | $I^2C$ clock |
| 10 | 8 | – | 1 | 64 | NC | | LV | Not connected |
| 11 | 7 | 6 | 80 | 63 | STANDBYQ | IN | OBL | Stand-by (low-active) |
| 12 | 6 | 5 | 79 | 62 | ADR_SEL | IN | OBL | $I^2C$ Bus address select |
| 13 | 5 | 4 | 78 | 61 | D_CTR_I/O_0 | IN/OUT | LV | D_CTR_I/O_0 |
| 14 | 4 | 3 | 77 | 60 | D_CTR_I/O_1 | IN/OUT | LV | D_CTR_I/O_1 |
| 15 | 3 | – | 76 | 59 | NC | | LV | Not connected |
| 16 | 2 | – | 75 | 58 | NC | | LV | Not connected |
| 17 | – | – | – | – | NC | | LV | Not connected |
| 18 | 1 | 2 | 74 | 57 | AUD_CL_OUT | OUT | LV | Audio clock output (18.432 MHz) |
| 19 | 64 | 1 | 73 | 56 | TP | | LV | Test pin |
| 20 | 63 | 52 | 72 | 55 | XTAL_OUT | OUT | OBL | Crystal oscillator |
| 21 | 62 | 51 | 71 | 54 | XTAL_IN | IN | OBL | Crystal oscillator |
| 22 | 61 | 50 | 70 | 53 | TESTEN | IN | OBL | Test pin |
| 23 | 60 | 49 | 69 | 52 | ANA_IN2+ | IN | AVSS via 56 pF / LV | IF input 2 (can be left vacant, only if IF input 1 is also not in use) |
| 24 | 59 | 48 | 68 | 51 | ANA_IN– | IN | AVSS via 56 pF / LV | IF common (can be left vacant, only if IF input 1 is also not in use) |

| Pin No. | | | | | Pin Name | Type | Connection (if not used) | Short Description |
|---|---|---|---|---|---|---|---|---|
| PLCC 68-pin | PSDIP 64-pin | PSDIP 52-pin | PQFP 80-pin | PLQFP 64-pin | | | | |
| 25 | 58 | 47 | 67 | 50 | ANA_IN1+ | IN | LV | IF input 1 |
| 26 | 57 | 46 | 66 | 49 | AVSUP | | OBL | Analog power supply 5 V |
| – | – | – | 65 | – | AVSUP | | OBL | Analog power supply 5 V |
| – | – | – | 64 | – | NC | | LV | Not connected |
| – | – | – | 63 | – | NC | | LV | Not connected |
| 27 | 56 | 45 | 62 | 48 | AVSS | | OBL | Analog ground |
| – | – | – | 61 | – | AVSS | | OBL | Analog ground |
| 28 | 55 | 44 | 60 | 47 | MONO_IN | IN | LV | Mono input |
| – | – | – | 59 | – | NC | | LV | Not connected |
| 29 | 54 | 43 | 58 | 46 | VREFTOP | | OBL | Reference voltage IF A/D converter |
| 30 | 53 | 42 | 57 | 45 | SC1_IN_R | IN | LV | SCART 1 input, right |
| 31 | 52 | 41 | 56 | 44 | SC1_IN_L | IN | LV | SCART 1 input, left |
| 32 | 51 | – | 55 | 43 | ASG1 | | AHVSS | Analog Shield Ground 1 |
| 33 | 50 | 40 | 54 | 42 | SC2_IN_R | IN | LV | SCART 2 input, right |
| 34 | 49 | 39 | 53 | 41 | SC2_IN_L | IN | LV | SCART 2 input, left |
| 35 | 48 | – | 52 | 40 | ASG2 | | AHVSS | Analog Shield Ground 2 |
| 36 | 47 | 38 | 51 | 39 | SC3_IN_R | IN | LV | SCART 3 input, right |
| 37 | 46 | 37 | 50 | 38 | SC3_IN_L | IN | LV | SCART 3 input, left |
| 38 | 45 | – | 49 | 37 | ASG4 | | AHVSS | Analog Shield Ground 4 |
| 39 | 44 | – | 48 | 36 | SC4_IN_R | IN | LV | SCART 4 input, right |
| 40 | 43 | – | 47 | 35 | SC4_IN_L | IN | LV | SCART 4 input, left |
| 41 | – | – | 46 | – | NC | | LV or AHVSS | Not connected |
| 42 | 42 | 36 | 45 | 34 | AGNDC | | OBL | Analog reference voltage |
| 43 | 41 | 35 | 44 | 33 | AHVSS | | OBL | Analog ground |
| – | – | – | 43 | – | AHVSS | | OBL | Analog ground |
| – | – | – | 42 | – | NC | | LV | Not connected |
| – | – | – | 41 | – | NC | | LV | Not connected |
| 44 | 40 | 34 | 40 | 32 | CAPL_M | | OBL | Volume capacitor MAIN |
| 45 | 39 | 33 | 39 | 31 | AHVSUP | | OBL | Analog power supply 8 V |
| 46 | 38 | 32 | 38 | 30 | CAPL_A | | OBL | Volume capacitor AUX |

| Pin No. | | | | | Pin Name | Type | Connection (if not used) | Short Description |
|---|---|---|---|---|---|---|---|---|
| PLCC 68-pin | PSDIP 64-pin | PSDIP 52-pin | PQFP 80-pin | PLQFP 64-pin | | | | |
| 47 | 37 | 31 | 37 | 29 | SC1_OUT_L | OUT | LV | SCART output 1, left |
| 48 | 36 | 30 | 36 | 28 | SC1_OUT_R | OUT | LV | SCART output 1, right |
| 49 | 35 | 29 | 35 | 27 | VREF1 | | OBL | Reference ground 1 |
| 50 | 34 | 28 | 34 | 26 | SC2_OUT_L | OUT | LV | SCART output 2, left |
| 51 | 33 | 27 | 33 | 25 | SC2_OUT_R | OUT | LV | SCART output 2, right |
| 52 | – | – | 32 | – | NC | | LV | Not connected |
| 53 | 32 | – | 31 | 24 | NC | | LV | Not connected |
| 54 | 31 | 26 | 30 | 23 | DACM_SUB | OUT | LV | Subwoofer output |
| 55 | 30 | – | 29 | 22 | NC | | LV | Not connected |
| 56 | 29 | 25 | 28 | 21 | DACM_L | OUT | LV | Loudspeaker out, left |
| 57 | 28 | 24 | 27 | 20 | DACM_R | OUT | LV | Loudspeaker out, right |
| 58 | 27 | 23 | 26 | 19 | VREF2 | | OBL | Reference ground 2 |
| 59 | 26 | 22 | 25 | 18 | DACA_L | OUT | LV | Headphone out, left |
| 60 | 25 | 21 | 24 | 17 | DACA_R | OUT | LV | Headphone out, right |
| – | – | – | 23 | – | NC | | LV | Not connected |
| – | – | – | 22 | – | NC | | LV | Not connected |
| 61 | 24 | 20 | 21 | 16 | RESETQ | IN | OBL | Power-on-reset |
| 62 | 23 | – | 20 | 15 | NC | | LV | Not connected |
| 63 | 22 | – | 19 | 14 | NC | | LV | Not connected |
| 64 | 21 | 19 | 18 | 13 | NC | | LV | Not connected |
| 65 | 20 | 18 | 17 | 12 | I2S_DA_IN2 | IN | LV | $I^2S$2-data input |
| 66 | 19 | 17 | 16 | 11 | DVSS | | OBL | Digital ground |
| – | – | – | 15 | – | DVSS | | OBL | Digital ground |
| – | – | – | 14 | – | DVSS | | OBL | Digital ground |
| 67 | 18 | 16 | 13 | 10 | DVSUP | | OBL | Digital power supply 5 V |
| – | – | – | 12 | – | DVSUP | | OBL | Digital power supply 5 V |
| – | – | – | 11 | – | DVSUP | | OBL | Digital power supply 5 V |
| 68 | 17 | 15 | 10 | 9 | ADR_CL | OUT | LV | ADR clock |

[1)] Due to the compatibility with MSP 3410B, it is possible to connect with DVSS as well.

### 4.3. Pin Descriptions

Pin numbers refer to the 80-pin PQFP package.

Pin 1, **NC** – Pin not connected.

Pin 2, **I2C_CL** – $I^2C$ Clock Input/Output (Fig. 4–12)
Via this pin, the $I^2C$-bus clock signal has to be supplied. The signal can be pulled down by the MSP in case of wait conditions.

Pin 3, **I2C_DA** – $I^2C$ Data Input/Output (Fig. 4–12)
Via this pin, the $I^2C$-bus data is written to or read from the MSP.

Pin 4, **I2S_CL** – $I^2S$ Clock Input/Output (Fig. 4–15)
Clock line for the $I^2S$ bus. In master mode, this line is driven by the MSP; in slave mode, an external $I^2S$ clock has to be supplied.

Pin 5, **I2S_WS** – $I^2S$ Word Strobe Input/Output (Fig. 4–15)
Word strobe line for the $I^2S$ bus. In master mode, this line is driven by the MSP; in slave mode, an external $I^2S$ word strobe has to be supplied.

Pin 6, **I2S_DA_OUT** – $I^2S$ Data Output (Fig. 4–11)
Output of digital serial sound data of the MSP on the $I^2S$ bus.

Pin 7, **I2S_DA_IN1** – $I^2S$ Data Input 1 (Fig. 4–13)
First input of digital serial sound data to the MSP via the $I^2S$ bus.

Pin 8, **ADR_DA** – ADR Bus Data Output (Fig. 4–11)
Output of digital serial data to the DRP 3510A via the ADR bus.

Pin 9, **ADR_WS** – ADR Bus Word Strobe Output (Fig. 4–11)
Word strobe output for the ADR bus.

Pin 10, **ADR_CL** – ADR Bus Clock Output (Fig. 4–11)
Clock line for the ADR bus.

Pins 11, 12, 13, **DVSUP*** – Digital Supply Voltage
Power supply for the digital circuitry of the MSP. Must be connected to a +5 V power supply.

Pins 14, 15, 16, **DVSS*** – Digital Ground
Ground connection for the digital circuitry of the MSP.

Pin 17, **I2S_DA_IN2** – $I^2S$ Data Input 2 (Fig. 4–13)
Second input of digital serial sound data to the MSP via the $I^2S$ bus.

Pins 18, 19, 20, **NC** – Pins not connected.

Pin 21, **RESETQ** – Reset Input (Fig. 4–13)
In the steady state, high level is required. A low level resets the MSP 34x1G.

Pins 22, 23, **NC** – Pins not connected.

Pins 24, 25, **DACA_R/L** – Headphone Outputs (Fig. 4–21)
Output of the headphone signal. A 1-nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected headphone volume.

Pin 26, **VREF2** – Reference Ground 2
Reference analog ground. This pin must be connected separately to the single ground point (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the loudspeaker and headphone outputs.

Pins 27, 28, **DACM_R/L** – Loudspeaker Outputs (Fig. 4–21)
Output of the loudspeaker signal. A 1-nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected loudspeaker volume.

Pin 29, **NC** – Pin not connected.

Pin 30, **DACM_SUB** – Subwoofer Output (Fig. 4–21)
Output of the subwoofer signal. A 1-nF capacitor to AHVSS must be connected to this pin. Due to the low frequency content of the subwoofer output, the value of the capacitor may be increased for better suppression of high-frequency noise. The DC offset on this pin depends on the selected loudspeaker volume.

Pins 31, 32 **NC** – Pin not connected.

Pins 33, 34, **SC2_OUT_R/L** – SCART2 Outputs (Fig. 4–23)
Output of the SCART2 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 35, **VREF1** – Reference Ground 1
Reference analog ground. This pin must be connected separately to the single ground point (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the SCART outputs.

Pins 36, 37, **SC1_OUT_R/L** – SCART1 Outputs (Fig. 4–23)
Output of the SCART1 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 38, **CAPL_A** – Volume Capacitor Headphone (Fig. 4–18)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for headphone volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1-µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pin 39, **AHVSUP*** – Analog Power Supply High Voltage
Power is supplied via this pin for the analog circuitry of the MSP (except IF input). This pin must be connected to the +8 V supply.

Pin 40, **CAPL_M** – Volume Capacitor Loudspeaker (Fig. 4–18)
A 10-µF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for loudspeaker volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1 µF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pins 41, 42, **NC** – Pins not connected.

Pins 43, 44, **AHVSS*** – Analog Power Supply High Voltage
Ground connection for the analog circuitry of the MSP (except IF input).

Pin 45, **AGNDC** – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3-µF and a 100-nF capacitor in parallel. This pins shows a DC level of typically 3.73 V.

Pin 46, **NC** – Pin not connected.

Pins 47, 48, **SC4_IN_L/R** – SCART4 Inputs (Fig. 4–20)
The analog input signal for SCART4 is fed to this pin. Analog input connection must be AC-coupled.

Pin 49, **ASG4** – Analog Shield Ground 4
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 50, 51, **SC3_IN_L/R** – SCART3 Inputs (Fig. 4–20)
The analog input signal for SCART3 is fed to this pin. Analog input connection must be AC-coupled.

Pin 52, **ASG2** – Analog Shield Ground 2
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 53, 54 **SC2_IN_L/R** – SCART2 Inputs (Fig. 4–20)
The analog input signal for SCART2 is fed to this pin. Analog input connection must be AC-coupled.

Pin 55, **ASG1** – Analog Shield Ground 1
Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 56, 57 **SC1_IN_L/R** – SCART1 Inputs (Fig. 4–20)
The analog input signal for SCART1 is fed to this pin. Analog input connection must be AC-coupled.

Pin 58, **VREFTOP** – Reference Voltage IF A/D Converter (Fig. 4–17)
Via this pin, the reference voltage for the IF A/D converter is decoupled. It must be connected to AVSS pins with a 10-µF and a 100-nF capacitor in parallel. Traces must be kept short.

Pin 59, **NC** – Pin not connected.

Pin 60 **MONO_IN** – Mono Input (Fig. 4–20)
The analog mono input signal is fed to this pin. Analog input connection must be AC-coupled.

Pins 61, 62, **AVSS*** – Analog Power Supply Voltage
Ground connection for the analog IF input circuitry of the MSP.

Pins 63, 64, **NC** – Pins not connected.

Pins 65, 66, **AVSUP*** – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MSP. This pin must be connected to the +5 V supply.

Pin 67, **ANA_IN1**+ – IF Input 1 (Fig. 4–17)
The analog sound IF signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN1+ is internally connected to one input of a symmetrical op amp, ANA_IN- to the other.

Pin 68, **ANA_IN**– – IF Common (Fig. 4–17)
This pins serves as a common reference for ANA_IN1/2+ inputs.

Pin 69, **ANA_IN2**+ – IF Input 2 (Fig. 4–17)
The analog sound if signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN2+ is internally connected to one input of a symmetrical op amp, ANA_IN– to the other.

Pin 70, **TESTEN** – Test Enable Pin (Fig. 4–13)
This pin enables factory test modes. For normal operation, it must be connected to ground.

Pins 71, 72 **XTAL_IN, XTAL_OUT** – Crystal Input and Output Pins (Fig. 4–16)
These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. An external clock can be fed into XTAL_IN. The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

Pin 73, **TP** – This pin enables factory test modes. For normal operation, it must be left vacant.

Pin 74, **AUD_CL_OUT** – Audio Clock Output
(Fig. 4–16)
This is the 18.432 MHz main clock output.

Pins 75, 76, **NC** – Pins not connected.

Pins 77, 78, **D_CTR_I/O_1/0** – Digital Control Input/ Output Pins (Fig. 4–15)
These pins serve as general purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

Pin 79, **ADR_SEL** – $I^2C$ Bus Address Select
(Fig. 4–14)
By means of this pin, one of three device addresses for the MSP can be selected. The pin can be connected to ground ($I^2C$ device addresses $80/81_{hex}$), to +5 V supply ($84/85_{hex}$), or left open ($88/89_{hex}$).

Pin 80, **STANDBYQ** – Stand-by
In normal operation, this pin must be High. If the MSP 34x1G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off the 5 V, but keeping the 8-V power supply (**'Stand-by'-mode**), the SCART switches maintain their position and function.

*** Application Note:**
All ground pins should be connected to one low-resistive ground plane. All supply pins should be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as closely as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 µF. The capacitor with the lowest value should be placed nearest to the DVSUP and DVSS pins.

### 4.4. Pin Configurations

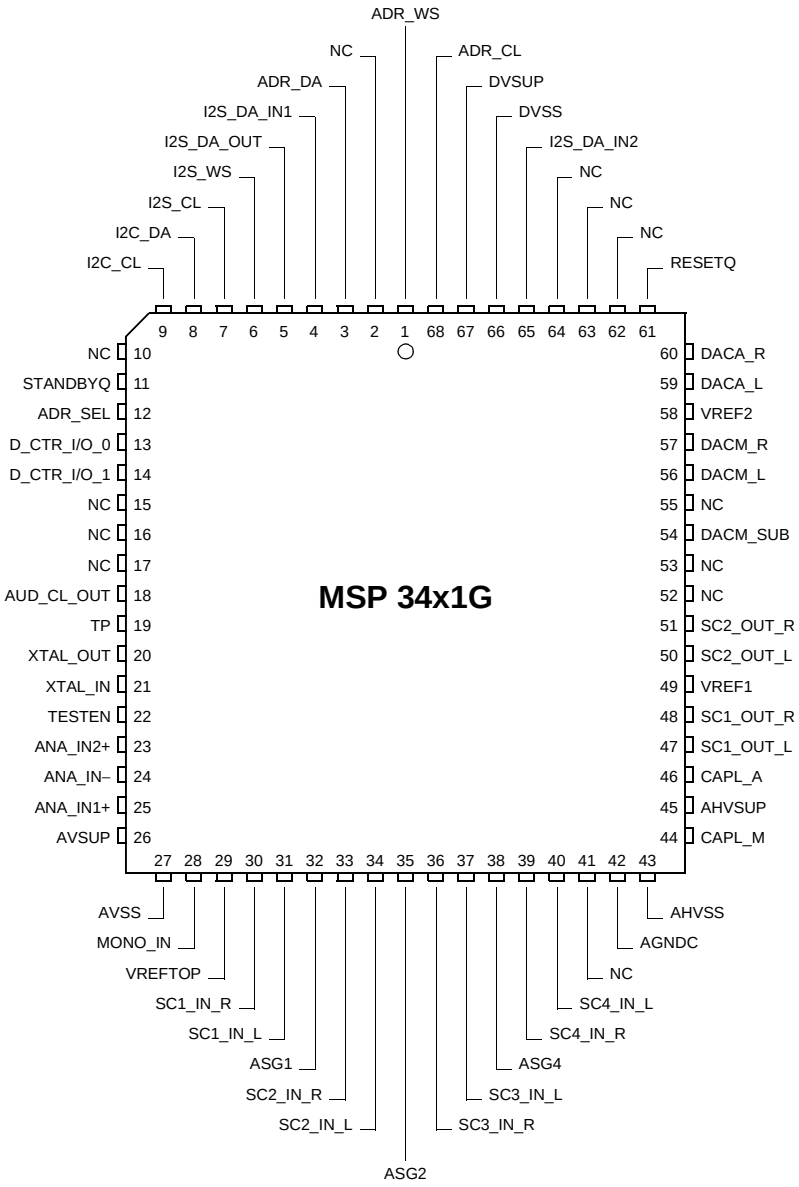



**Fig. 4–6:** 68-pin PLCC package

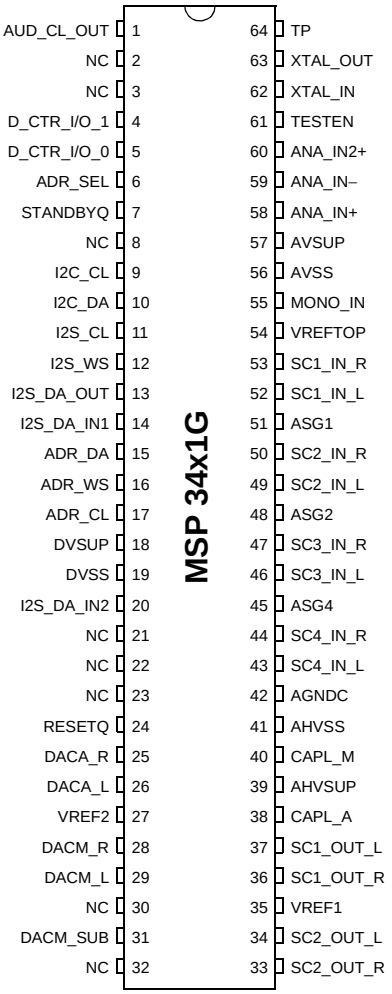



**Fig. 4–7:** 64-pin PSDIP package

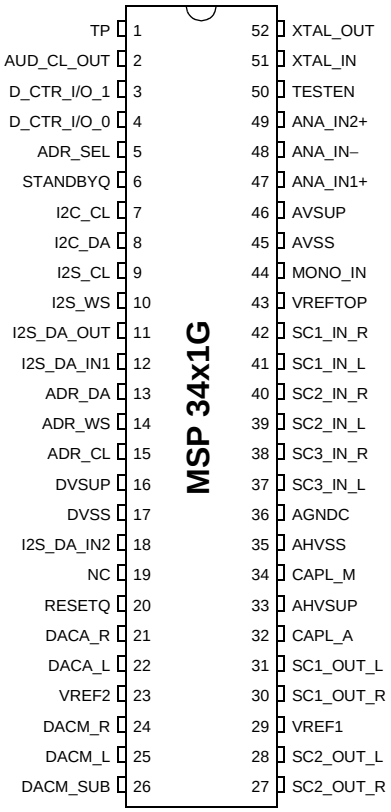



**Fig. 4–8:** 52-pin PSDIP package

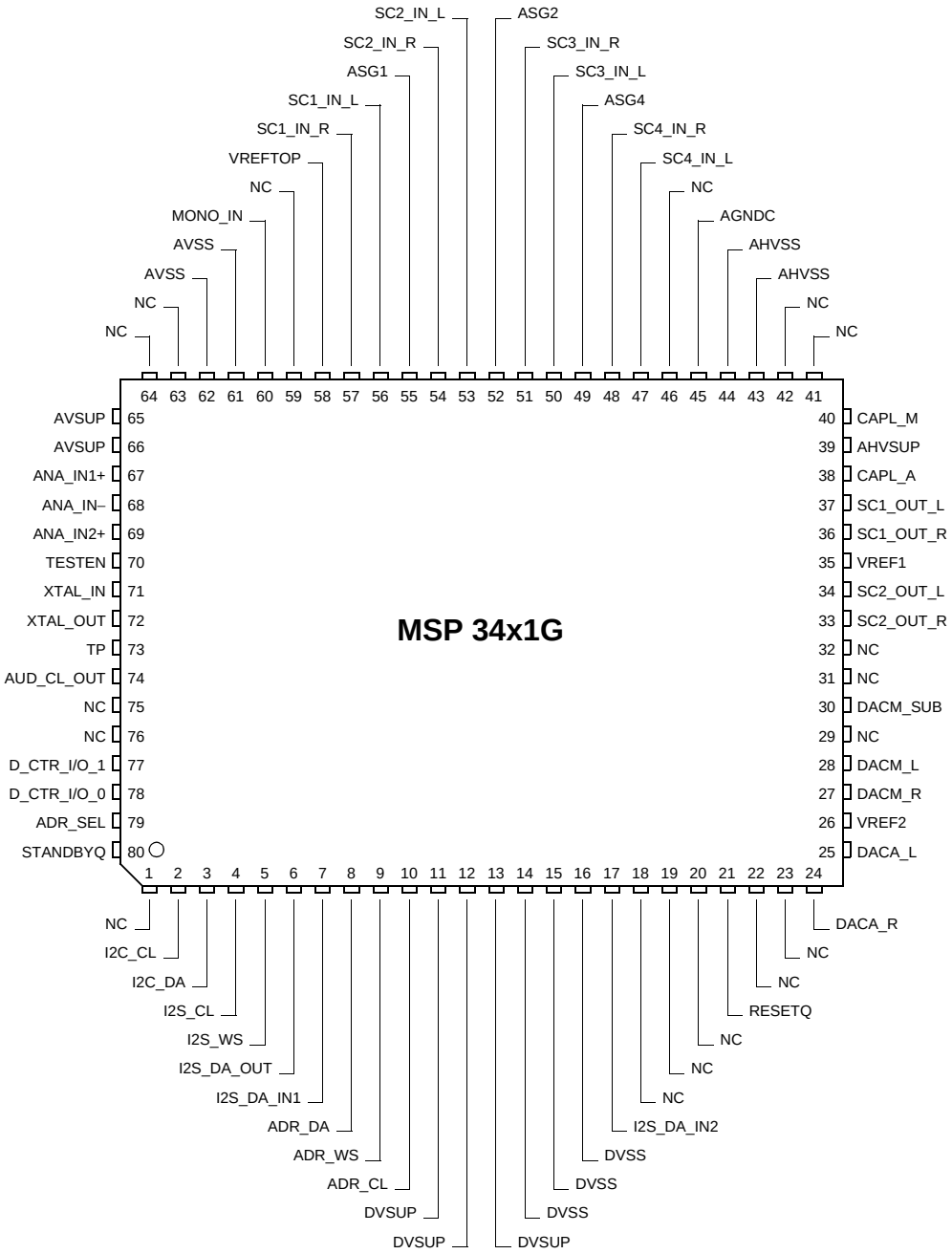



**Fig. 4–9:** 80-pin PQFP package

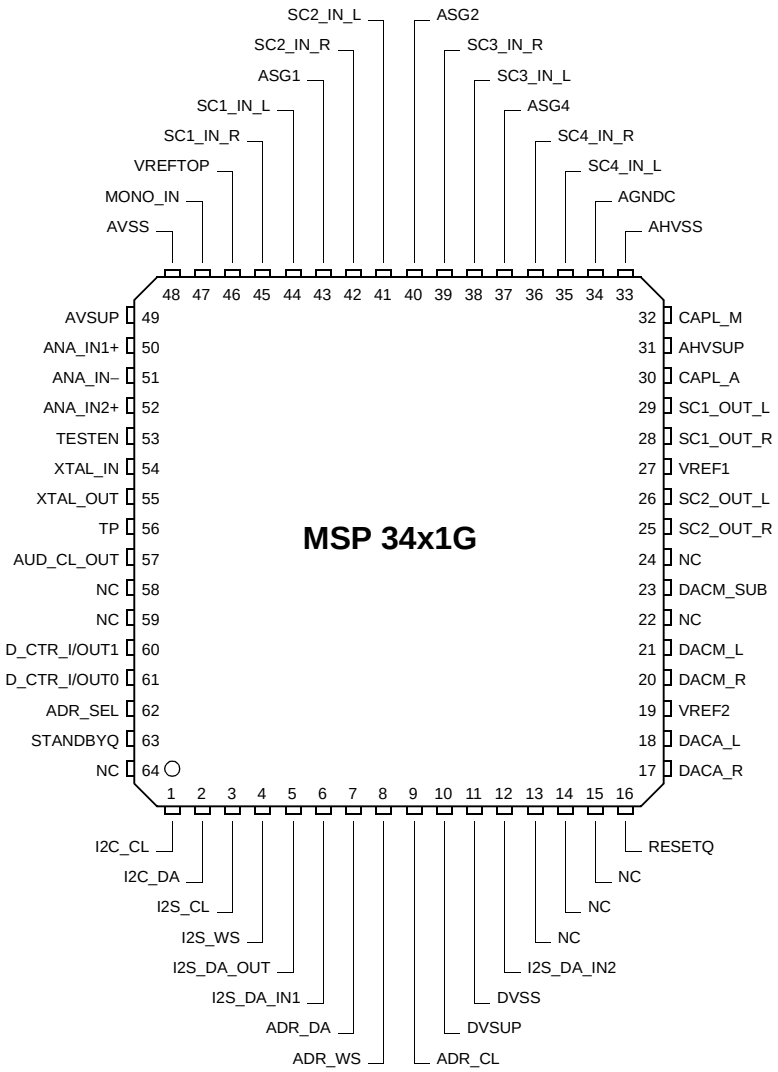



**Fig. 4–10:** 64-pin PLQFP package

### 4.5. Pin Circuits

Pin numbers refer to the PQFP80 package.

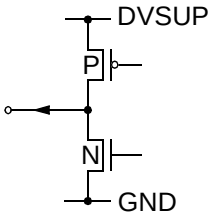



**Fig. 4–11:** Output Pins 6, 8, 9, and 10
**(I2S_DA_OUT, ADR_DA, ADR_WS, ADR_CL)**

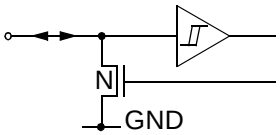



**Fig. 4–12:** Input/Output Pins 2 and 3
**(I2C_CL, I2C_DA)**

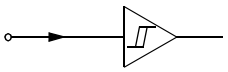


**Fig. 4–13:** Input Pins 7, 17, 21, 70, and 80
**(I2S_DA_IN1, I2S_DA_IN2, RESETQ, TESTEN, STANDBYQ**)

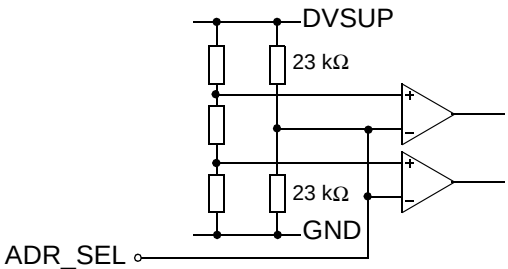



**Fig. 4–14:** Input Pin 79 **(ADR_SEL)**

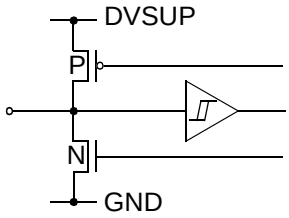



**Fig. 4–15:** Input/Output Pins 4, 5, 77, and 78
**(I2S_CL, I2S_WS, D_CTR_I/O_1, D_CTR_I/O_0)**

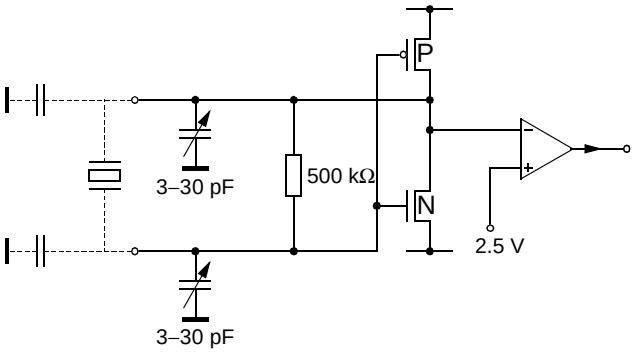



**Fig. 4–16:** Output/Input Pins 71, 72, and 74
**(XTAL_IN, XTAL_OUT, AUD_CL_OUT)**

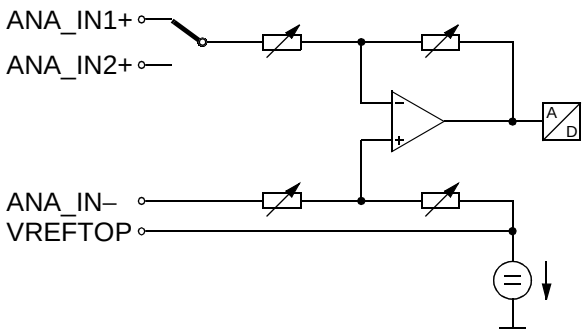



**Fig. 4–17:** Input Pins 58, 67, 68, and 69
**(VREFTOP, ANA_IN1+, ANA_IN-, ANA_IN2+)**

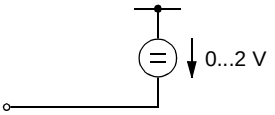



**Fig. 4–18:** Capacitor Pins 38 and 40 **(CAPL_A, CAPL_M)**

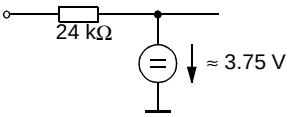



**Fig. 4–19:** Input Pin 60 **(MONO_IN**)

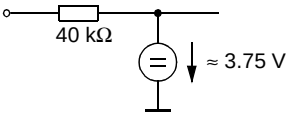



**Fig. 4–20:** Input Pins 47, 48, 50, 51, 53, 54, 56, and 57 **(SC4-1_IN_L/R)**

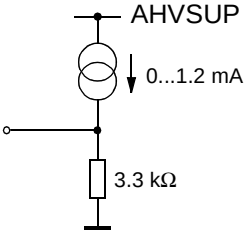



**Fig. 4–21:** Output Pins 24, 25, 27, 28 and 30 **(DACA_R/L, DACM_R/L, DACM_SUB)**

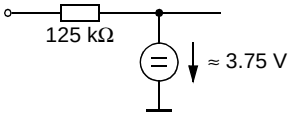



**Fig. 4–22:** Pin 45 **(AGNDC)**

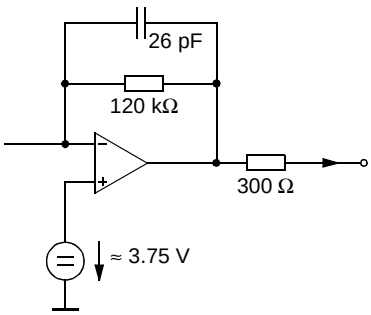



**Fig. 4–23:** Output Pins 33, 34, 36, and 37 **(SC_2_OUT_R/L, SC_1_OUT_R/L)**

### 4.6. Electrical Characteristics

#### 4.6.1. Absolute Maximum Ratings

| Symbol | Parameter | Pin Name | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | – | 0 | 70[1)] | °C |
| $T_S$ | Storage Temperature | – | –40 | 125 | °C |
| $V_{SUP1}$ | First Supply Voltage | AHVSUP | –0.3 | 9.0 | V |
| $V_{SUP2}$ | Second Supply Voltage | DVSUP | –0.3 | 6.0 | V |
| $V_{SUP3}$ | Third Supply Voltage | AVSUP | –0.3 | 6.0 | V |
| $dV_{SUP23}$ | Voltage between AVSUP and DVSUP | AVSUP, DVSUP | –0.5 | 0.5 | V |
| $P_{TOT}$ | Power Dissipation<br>PLCC68<br>PSDIP64<br>PSDIP52<br>PQFP80<br>PLQFP64 | AHVSUP, DVSUP, AVSUP | | <br>1200<br>1300<br>1200<br>1000<br>960[1)] | <br>mW<br>mW<br>mW<br>mW<br>mW |
| $V_{Idig}$ | Input Voltage, all Digital Inputs | | –0.3 | $V_{SUP2}$+0.3 | V |
| $I_{Idig}$ | Input Current, all Digital Pins | – | –20 | +20 | mA[2)] |
| $V_{Iana}$ | Input Voltage, all Analog Inputs | SCn_IN_s,[3)] MONO_IN | –0.3 | $V_{SUP1}$+0.3 | V |
| $I_{Iana}$ | Input Current, all Analog Inputs | SCn_IN_s,[3)] MONO_IN | –5 | +5 | mA[2)] |
| $I_{Oana}$ | Output Current, all SCART Outputs | SCn_OUT_s[3)] | [4), 5)] | [4), 5)] | |
| $I_{Oana}$ | Output Current, all Analog Outputs except SCART Outputs | DACp_s[3)] | [4)] | [4)] | |
| $I_{Cana}$ | Output Current, other pins connected to capacitors | CAPL_p,[3)] AGNDC | [4)] | [4)] | |

1) PLQFP64: 65 °C
2) positive value means current flowing into the circuit
3) “n” means “1”, “2”, “3”, or “4”, “s” means “L” or “R”, “p” means “M” or “A”
4) The analog outputs are short-circuit proof with respect to First Supply Voltage and ground.
5) Total chip power dissipation must not exceed absolute maximum rating.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

### 4.6.2. Recommended Operating Conditions ($T_A$ = 0 to 70 °C)

#### 4.6.2.1. General Recommended Operating Conditions

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SUP1}$ | First Supply Voltage (8-V Operation) | AHVSUP | 7.6 | 8.0 | 8.7 | V |
| | First Supply Voltage (5-V Operation) | | 4.75 | 5.0 | 5.25 | V |
| $V_{SUP2}$ | Second Supply Voltage | DVSUP | 4.75 | 5.0 | 5.25 | V |
| $V_{SUP3}$ | Third Supply Voltage | AVSUP | 4.75 | 5.0 | 5.25 | V |
| $t_{STBYQ1}$ | STANDBYQ Setup Time before Turn-off of Second Supply Voltage | STANDBYQ, DVSUP | 1 | | | µs |

#### 4.6.2.2. Analog Input and Output Recommendations

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{AGNDC}$ | AGNDC-Filter-Capacitor | AGNDC | –20% | 3.3 | | µF |
| | Ceramic Capacitor in Parallel | | –20% | 100 | | nF |
| $C_{inSC}$ | DC-Decoupling Capacitor in front of SCART Inputs | SCn_IN_s[1)] | –20% | 330 | | nF |
| $V_{inSC}$ | SCART Input Level | | | | 2.0 | $V_{RMS}$ |
| $V_{inMONO}$ | Input Level, Mono Input | MONO_IN | | | 2.0 | $V_{RMS}$ |
| $R_{LSC}$ | SCART Load Resistance | SCn_OUT_s[1)] | 10 | | | kΩ |
| $C_{LSC}$ | SCART Load Capacitance | | | | 6.0 | nF |
| $C_{VMA}$ | Main/AUX Volume Capacitor | CAPL_M, CAPL_A | | 10 | | µF |
| $C_{FMA}$ | Main/AUX Filter Capacitor | DACM_s, DACA_s[1)] | –10% | 1 | +10% | nF |

[1)] “n” means “1”, “2”, or “3”, “s” means “L” or “R”, “p” means “M” or “A”

#### 4.6.2.3. Recommendations for Analog Sound IF Input Signal

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{VREFTOP}$ | VREFTOP-Filter-Capacitor | VREFTOP | –20 % | 10 | | µF |
| | Ceramic Capacitor in Parallel | | –20 % | 100 | | nF |
| $F_{IF_FMTV}$ | Analog Input Frequency Range for TV Applications | ANA_IN1+, ANA_IN2+, ANA_IN– | 0 | | 9 | MHz |
| $F_{IF_FMRADIO}$ | Analog Input Frequency for FM-Radio Applications | | | 10.7 | | MHz |
| $V_{IF_FM}$ | Analog Input Range FM/NICAM | | 0.1 | 0.8 | 3 | $V_{pp}$ |
| $V_{IF_AM}$ | Analog Input Range AM/NICAM | | 0.1 | 0.45 | 0.8 | $V_{pp}$ |
| $R_{FMNI}$ | Ratio: NICAM Carrier/FM Carrier (unmodulated carriers)<br>BG:<br>I: | | <br><br>–20<br>–23 | <br><br>–7<br>–10 | <br><br>0<br>0 | <br><br>dB<br>dB |
| $R_{AMNI}$ | Ratio: NICAM Carrier/AM Carrier (unmodulated carriers) | | –25 | –11 | 0 | dB |
| $R_{FM}$ | Ratio: FM-Main/FM-Sub Satellite | | | 7 | | dB |
| $R_{FM1/FM2}$ | Ratio: FM1/FM2 German FM-System | | | 7 | | dB |
| $R_{FC}$ | Ratio: Main FM Carrier/ Color Carrier | | 15 | – | – | dB |
| $R_{FV}$ | Ratio: Main FM Carrier/ Luma Components | | 15 | – | – | dB |
| $PR_{IF}$ | Passband Ripple | | – | – | ±2 | dB |
| $SUP_{HF}$ | Suppression of Spectrum above 9.0 MHz (not for FM Radio) | | 15 | | – | dB |
| $FM_{MAX}$ | Maximum FM-Deviation (approx.)<br>normal mode<br>HDEV2: high deviation mode<br>HDEV3: very high deviation mode | | | | <br>±180<br>±360<br>±540 | <br>kHz<br>kHz<br>kHz |

#### 4.6.2.4. Crystal Recommendations

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General Crystal Recommendations** | | | | | | |
| $f_P$ | Crystal Parallel Resonance Frequency at 12 pF Load Capacitance | | | 18.432 | | MHz |
| $R_R$ | Crystal Series Resistance | | | 8 | 25 | Ω |
| $C_0$ | Crystal Shunt (Parallel) Capacitance | | | 6.2 | 7.0 | pF |
| $C_L$ | External Load Capacitance[1)] | XTAL_IN, XTAL_OUT | PSDIP<br>PLCC<br>P(L)QFP | approx. 1.5<br>approx. 3.3<br>approx. 3.3 | | pF<br>pF<br>pF |
| **Crystal Recommendations for Master-Slave Applications** (MSP-clock must perform synchronization to $I^2S$ clock) | | | | | | |
| $f_{TOL}$ | Accuracy of Adjustment | | –20 | | +20 | ppm |
| $D_{TEM}$ | Frequency Variation versus Temperature | | –20 | | +20 | ppm |
| $C_1$ | Motional (Dynamic) Capacitance | | 19 | 24 | | fF |
| $f_{CL}$ | Required Open Loop Clock Frequency ($T_{amb}$ = 25 °C) | AUD_CL_OUT | 18.431 | | 18.433 | MHz |
| **Crystal Recommendations for FM / NICAM Applications** (No MSP-clock synchronization to $I^2S$ clock possible) | | | | | | |
| $f_{TOL}$ | Accuracy of Adjustment | | –30 | | +30 | ppm |
| $D_{TEM}$ | Frequency Variation versus Temperature | | –30 | | +30 | ppm |
| $C_1$ | Motional (Dynamic) Capacitance | | 15 | | | fF |
| $f_{CL}$ | Required Open Loop Clock Frequency ($T_{amb}$ = 25 °C) | AUD_CL_OUT | 18.4305 | | 18.4335 | MHz |
| **Crystal Recommendations for all analog FM/AM Applications** (No MSP-clock synchronization to $I^2S$ clock possible) | | | | | | |
| $f_{TOL}$ | Accuracy of Adjustment | | –100 | | +100 | ppm |
| $D_{TEM}$ | Frequency Variation versus Temperature | | –50 | | +50 | ppm |
| $f_{CL}$ | Required Open Loop Clock Frequency ($T_{amb}$ = 25 °C) | AUD_CL_OUT | 18.429 | | 18.435 | MHz |
| **Amplitude Recommendation for Operation with External Clock Input** ($C_{load}$ after reset typ. 22 pF) | | | | | | |
| $V_{XCA}$ | External Clock Amplitude | XTAL_IN | 0.7 | | | $V_{pp}$ |

[1)] External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation.
Due to different layouts, the accurate capacitor size should be determined with the customer PCB. The suggested values (1.5...3.3 pF) are figures based on experience and should serve as “start value”.

To define the capacitor size, reset the MSP without transmitting any further I2C telegrams. Measure the frequency at AUD_CL_OUT-pin. Change the capacitor size until the free running frequency matches 18.432 MHz as closely as possible. The higher the capacity, the lower the resulting clock frequency.

### 4.6.3. Characteristics

at $T_A$ = 0 to 70 °C, $f_{CLOCK}$ = 18.432 MHz, $V_{SUP1}$ = 7.6 to 8.7 V, $V_{SUP2}$ = 4.75 to 5.25 V for min./max. values
at $T_A$ = 60 °C, $f_{CLOCK}$ = 18.432 MHz, $V_{SUP1}$ = 8 V, $V_{SUP2}$ = 5 V for typical values,
$T_J$ = Junction Temperature
MAIN (M) = Loudspeaker Channel, AUX (A) = Headphone Channel

#### 4.6.3.1. General Characteristics

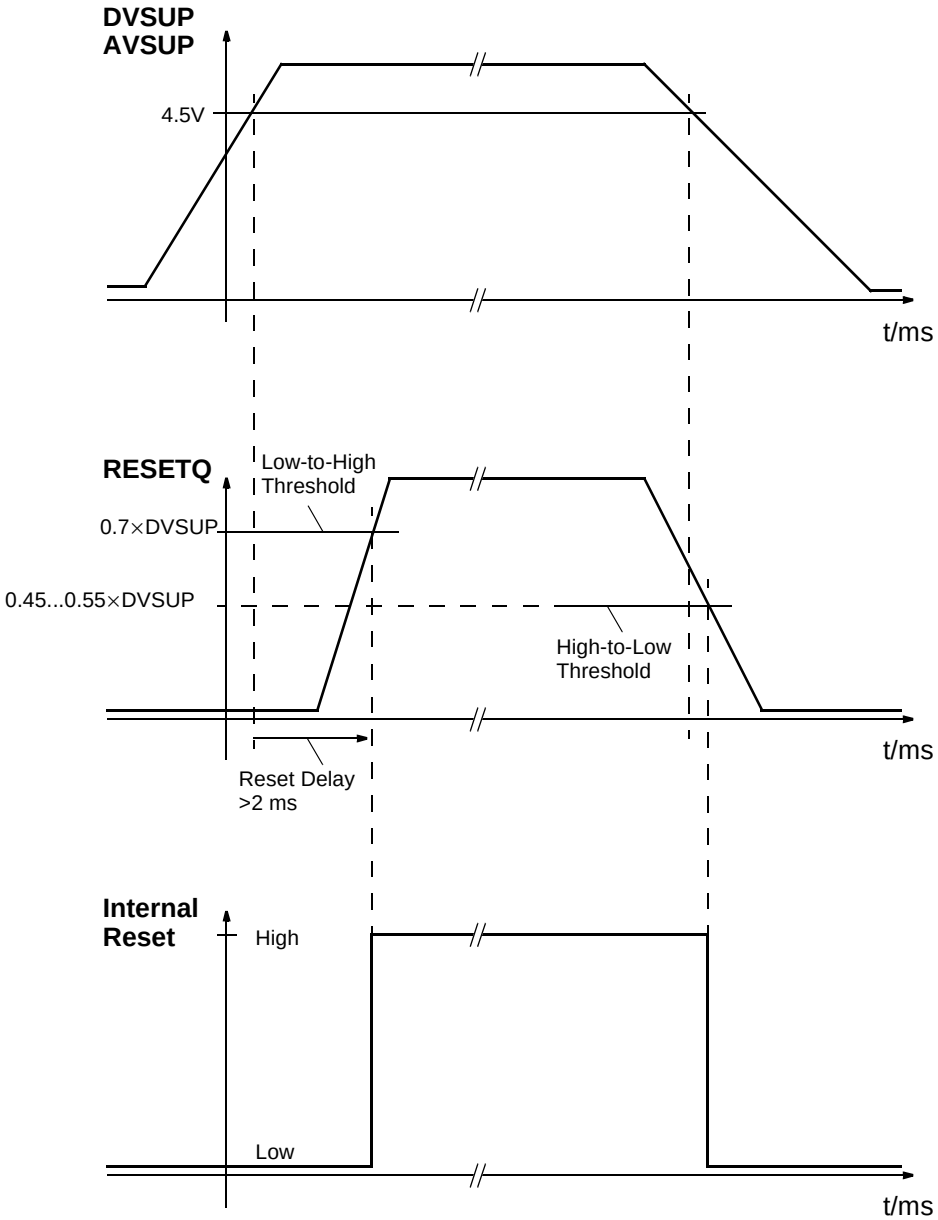
| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| $I_{SUP1A}$ | First Supply Current (active) (8-V Operation)<br>Analog Volume for Main and Aux at 0 dB<br>Analog Volume for Main and Aux at –30 dB | AHVSUP | <br>9.6<br>6.3 | <br>17.1<br>11.2 | <br>24.6<br>16.1 | <br>mA<br>mA | |
| | First Supply Current (active) (5-V Operation)<br>Analog Volume for Main and Aux at 0 dB<br>Analog Volume for Main and Aux at –30 dB | | <br>6.4<br>4.2 | <br>11.4<br>7.5 | <br>16.4<br>10.7 | <br>mA<br>mA | |
| $I_{SUP2A}$ | Second Supply Current (active) | DVSUP | 50 | 65 | 85 | mA | |
| $I_{SUP3A}$ | Third Supply Current (active) | AVSUP | 20 | 35 | 45 | mA | |
| $I_{SUP1S}$ | First Supply Current (8-V Operation) (standby mode) at $T_j$ = 27 °C | AHVSUP | 3.5 | 5.6 | 7.7 | mA | STANDBYQ = low |
| | First Supply Current (5-V Operation) (standby mode) at $T_j$ = 27 °C | | 2.3 | 3.7 | 5.1 | mA | STANDBYQ = low |
| **Clock** | | | | | | | |
| $f_{CLOCK}$ | Clock Input Frequency | XTAL_IN | | 18.432 | | MHz | |
| $D_{CLOCK}$ | Clock High to Low Ratio | | 45 | | 55 | % | |
| $t_{JITTER}$ | Clock Jitter (Verification not provided in Production Test) | | | | 50 | ps | |
| $V_{xtalDC}$ | DC-Voltage Oscillator | | | 2.5 | | V | |
| $t_{Startup}$ | Oscillator Startup Time at VDD Slew-rate of 1 V/1 µs | XTAL_IN, XTAL_OUT | | 0.4 | 2 | ms | |
| $V_{ACLKAC}$ | Audio Clock Output AC Voltage | AUD_CL_OUT | 1.2 | 1.8 | | $V_{pp}$ | load = 40 pF |
| $V_{ACLKDC}$ | Audio Clock Output DC Voltage | | 0.4 | | 0.6 | $V_{SUP3}$ | $I_{max}$ = 0.2 mA |
| $r_{outHF_ACL}$ | HF Output Resistance | | | 140 | | Ω | |

### 4.6.3.2. Digital Inputs, Digital Outputs

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Digital Input Levels** | | | | | | | |
| $V_{DIGIL}$ | Digital Input Low Voltage | STANDBYQ<br>D_CTR_I/O_0/1 | | | 0.2 | $V_{SUP2}$ | |
| $V_{DIGIH}$ | Digital Input High Voltage | | 0.5 | | | $V_{SUP2}$ | |
| $Z_{DIGI}$ | Input Impedance | | | | 5 | pF | |
| $I_{DLEAK}$ | Digital Input Leakage Current | | –1 | | 1 | µA | 0 V < $U_{INPUT}$< DVSUP<br>D_CTR_I/O_0/1: tri-state |
| $V_{DIGIL}$ | Digital Input Low Voltage | ADR_SEL | | | 0.2 | $V_{SUP2}$ | |
| $V_{DIGIH}$ | Digital Input High Voltage | | 0.8 | | | $V_{SUP2}$ | |
| $I_{ADRSEL}$ | Input Current Address Select Pin | | –500 | –220 | | µA | $U_{ADR_SEL}$= DVSS |
| | | | | 220 | 500 | µA | $U_{ADR_SEL}$= DVSUP |
| **Digital Output Levels** | | | | | | | |
| $V_{DCTROL}$ | Digital Output Low Voltage | D_CTR_I/O_0<br>D_CTR_I/O_1 | | | 0.4 | V | IDDCTR = 1 mA |
| $V_{DCTROH}$ | Digital Output High Voltage | | 4.0 | | | V | IDDCTR = –1 mA |

### 4.6.3.3. Reset Input and Power-Up

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **RESETQ Input Levels** | | | | | | | |
| $V_{RHL}$ | Reset High-Low Transition Voltage | RESETQ | 0.45 | | 0.55 | $V_{SUP2}$ | |
| $V_{RLH}$ | Reset Low-High Transition Voltage | | 0.7 | | 0.8 | $V_{SUP2}$ | |
| $Z_{RES}$ | Input Impedance | | | | 5 | pF | |
| $I_{RES}$ | Input Pin Leakage Current | | -1 | | 1 | µA | 0 V < $U_{INPUT}$< DVSUP |




**Note:** The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

0.7 x DVSUP means 3.5 Volt with DVSUP = 5.0 V

**Fig. 4–24:** Power-up sequence

### 4.6.3.4. I²C-Bus Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{I2CIL}$ | I²C-Bus Input Low Voltage | I2C_CL, I2C_DA | | | 0.3 | $V_{SUP2}$ | |
| $V_{I2CIH}$ | I²C-Bus Input High Voltage | | 0.6 | | | $V_{SUP2}$ | |
| $t_{I2C1}$ | I²C Start Condition Setup Time | | 120 | | | ns | |
| $t_{I2C2}$ | I²C Stop Condition Setup Time | | 120 | | | ns | |
| $t_{I2C5}$ | I²C-Data Setup Time before Rising Edge of Clock | | 55 | | | ns | |
| $t_{I2C6}$ | I²C-Data Hold Time after Falling Edge of Clock | | 55 | | | ns | |
| $t_{I2C3}$ | I²C-Clock Low Pulse Time | I2C_CL | 500 | | | ns | |
| $t_{I2C4}$ | I²C-Clock High Pulse Time | | 500 | | | ns | |
| $f_{I2C}$ | I²C-BUS Frequency | | | | 1.0 | MHz | |
| $V_{I2COL}$ | I²C-Data Output Low Voltage | I2C_CL, I2C_DA | | | 0.4 | V | $I_{I2COL}$ = 3 mA |
| $I_{I2COH}$ | I²C-Data Output High Leakage Current | | | | 1.0 | µA | $V_{I2COH}$ = 5 V |
| $t_{I2COL1}$ | I²C-Data Output Hold Time after Falling Edge of Clock | | 15 | | | ns | |
| $t_{I2COL2}$ | I²C-Data Output Setup Time before Rising Edge of Clock | | 100 | | | ns | $f_{I2C}$ = 1 MHz |

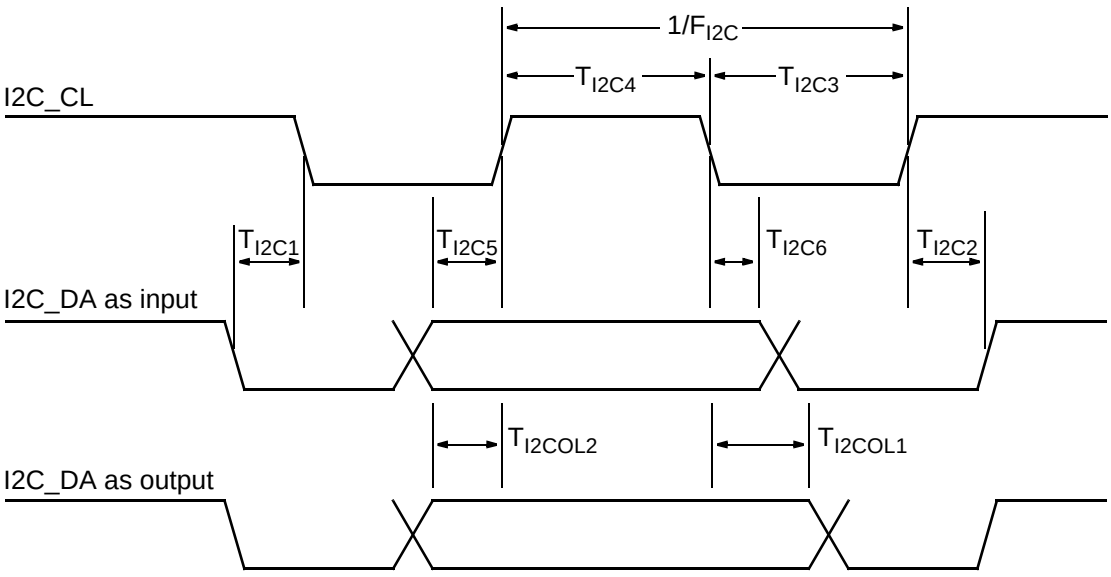



**Fig. 4–25:** I²C bus timing diagram

### 4.6.3.5. I²S-Bus Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{I2SIL}$ | Input Low Voltage | I2S_DA_IN1/2 I2S_CL I2S_WS | | | 0.2 | $V_{SUP2}$ | |
| $V_{I2SIH}$ | Input High Voltage | | 0.5 | | | $V_{SUP2}$ | |
| $Z_{I2SI}$ | Input Impedance | | | | 5 | pF | |
| $I_{DLEAKI2SI}$ | Input Leakage Current | | –1 | | 1 | µA | 0 V < $U_{INPUT}$< DVSUP I²S slave mode |
| $t_{I2S1}$ | I²S-Data Input Setup Time before Rising Edge of Clock | I2S_DA_IN1/2, I2S_CL | 20 | | | ns | |
| $t_{I2S2}$ | I²S-Data Input Hold Time after Falling Edge of Clock | | 0 | | | ns | |
| $f_{I2SWS}$ | I²S-Word Strobe Input Frequency when MSP in I²S-Slave Mode | I2S_WS | | 32.0 | | kHz | |
| $f_{I2SCL}$ | I²S-Clock Input Frequency when MSP in I²S-Slave-Mode | I2S_CL | | 1.024 | | MHz | |
| $R_{I2SCL}$ | I²S-Clock Input Ratio when MSP in I²S-Slave-Mode | | 0.9 | | 1.1 | | |
| $t_{I2SWS1}$ | I²S-Word Strobe Input Setup Time before Rising Edge of Clock when MSP in I²S-Slave-Mode | I2S_WS, I2S_CL | 60 | | | ns | |
| $t_{I2SWS2}$ | I²S-Word Strobe Input Hold Time after Falling Edge of Clock when MSP in I²S-Slave-Mode | | 0 | | | ns | |
| $V_{I2SOL}$ | I²S Output Low Voltage | I2S_WS, I2S_CL, I2S_DA_OUT | | | 0.4 | V | $I_{I2SOL}$ = 1 mA |
| $V_{I2SOH}$ | I²S Output High Voltage | | 4.0 | | | V | $I_{I2SOH}$ = –1 mA |
| $f_{I2SWS}$ | I²S-Word Strobe Output Frequency | I2S_WS | | 32.0 | | kHz | NICAM-PLL closed |
| $f_{I2SCL}$ | I²S-Clock Output Frequency | I2S_CL | | 1024 | | kHz | |
| $t_{I2S1/I2S2}$ | I²S-Clock High/Low-Ratio | | 0.9 | 1.0 | 1.1 | | |
| $t_{I2S3}$ | I²S-Data Setup Time before Rising Edge of Clock | I2S_CL, I2S_DA_OUT | 200 | | | ns | $C_L$ = 30 pF |
| $t_{I2S4}$ | I²S-Data Hold Time after Falling Edge of Clock | | | | 180 | ns | |
| $t_{I2S5}$ | I²S-Word Strobe Setup Time before Rising Edge of Clock | I2S_CL, I2S_WS | 200 | | | ns | |
| $t_{I2S6}$ | I²S-Word Strobe Hold Time after Falling Edge of Clock | | | | 180 | ns | |

(Data: MSB first)

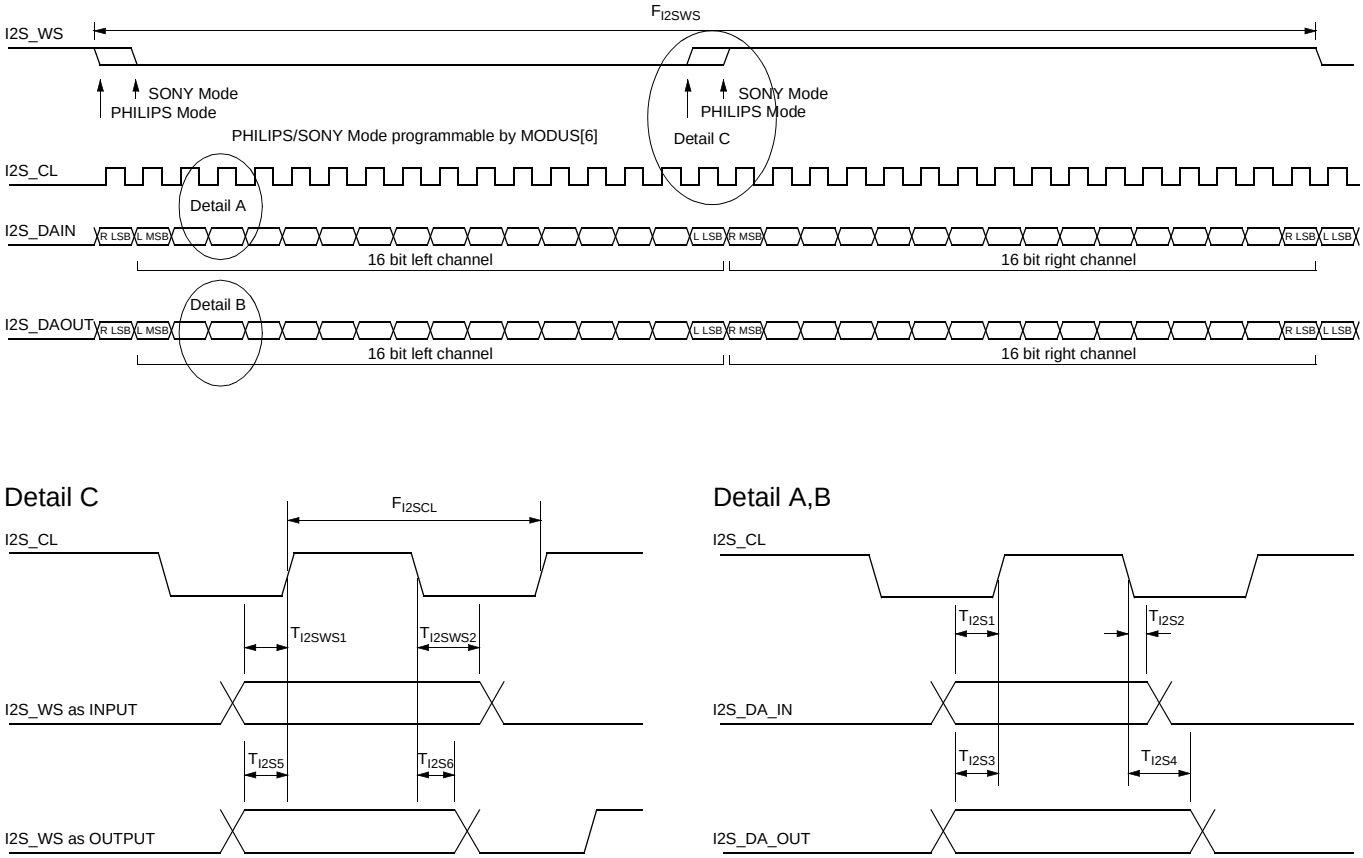



**Fig. 4–26:** $I^2S$ bus timing diagram

### 4.6.3.6. Analog Baseband Inputs and Outputs, AGNDC

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Analog Ground** | | | | | | | |
| $V_{AGNDC0}$ | AGNDC Open Circuit Voltage (8-V Operation) | AGNDC | 3.67 | 3.77 | 3.87 | V | $R_{load} \geq 10\ M\Omega$ |
| | AGNDC Open Circuit Voltage (5-V Operation) | | 2.41 | 2.51 | 2.61 | V | |
| $R_{outAGN}$ | AGNDC Output Resistance (8-V Operation) | | 70 | 125 | 180 | kΩ | $3\ V \leq V_{AGNDC} \leq 4\ V$ |
| | AGNDC Output Resistance (5-V Operation) | | 47 | 83 | 120 | kΩ | |
| **Analog Input Resistance** | | | | | | | |
| $R_{inSC}$ | SCART Input Resistance from $T_A$ = 0 to 70 °C | SCn_IN_s[1)] | 25 | 40 | 58 | kΩ | $f_{signal}$ = 1 kHz, I = 0.05 mA |
| $R_{inMONO}$ | MONO Input Resistance from $T_A$ = 0 to 70 °C | MONO_IN | 15 | 24 | 35 | kΩ | $f_{signal}$ = 1 kHz, I = 0.1 mA |

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Audio Analog-to-Digital-Converter** | | | | | | | |
| $V_{AICL}$ | Effective Analog Input Clipping Level for Analog-to-Digital-Conversion (8-V Operation) | SCn_IN_s,[1] MONO_IN | 2.00 | | 2.25 | $V_{RMS}$ | $f_{signal}$ = 1 kHz |
| | Effective Analog Input Clipping Level for Analog-to-Digital-Conversion (5-V Operation) | | 1.13 | | 1.51 | $V_{RMS}$ | |
| **SCART Outputs** | | | | | | | |
| $R_{outSC}$ | SCART Output Resistance at $T_j$ = 27 °C<br>from $T_A$ = 0 to 70 °C | SCn_OUT_s[1] | 200<br>200 | 330 | 460<br>500 | Ω<br>Ω | $f_{signal}$ = 1 kHz, I = 0.1 mA |
| $dV_{OUTSC}$ | Deviation of DC-Level at SCART Output from AGNDC Voltage | | −70 | | +70 | mV | |
| $A_{SCtoSC}$ | Gain from Analog Input to SCART Output | SCn_IN_s,[1] MONO_IN → SCn_OUT_s[1] | −1.0 | | +0.5 | dB | $f_{signal}$ = 1 kHz |
| $f_{rSCtoSC}$ | Frequency Response from Analog Input to SCART Output Bandwidth: 0 to 20000 Hz | | −0.5 | | +0.5 | dB | with resp. to 1 kHz |
| $V_{outSC}$ | Effective Signal Level at SCART-Output during full-scale Digital Input Signal from $I^2S$ (8-V Operation) | SCn_OUT_s[1] | 1.8 | 1.9 | 2.0 | $V_{RMS}$ | $f_{signal}$ = 1 kHz |
| | Effective Signal Level at SCART-Output during full-scale Digital Input Signal from $I^2S$ (5-V Operation) | | 1.17 | 1.27 | 1.37 | $V_{RMS}$ | |
| **Main and AUX Outputs** | | | | | | | |
| $R_{outMA}$ | Main/AUX Output Resistance at $T_j$ = 27 °C<br>from $T_A$ = 0 to 70 °C | DACp_s[1] | 2.1<br>2.1 | 3.3 | 4.6<br>5.0 | kΩ<br>kΩ | $f_{signal}$ = 1 kHz, I = 0.1 mA |
| $V_{outDCMA}$ | DC-Level at Main/AUX-Output for Analog Volume at 0 dB<br>for Analog Volume at −30 dB (8-V Operation) | | 1.80 | 2.04<br>61 | 2.28 | V<br>mV | |
| | DC-Level at Main/AUX-Output for Analog Volume at 0 dB<br>for Analog Volume at −30 dB (5-V Operation) | | 1.12 | 1.36<br>40 | 1.60 | V<br>mV | |
| $V_{outMA}$ | Effective Signal Level at Main/AUX-Output during full-scale Digital Input Signal from $I^2S$ for Analog Volume at 0 dB (8-V Operation) | | 1.23 | 1.37 | 1.51 | $V_{RMS}$ | $f_{signal}$ = 1 kHz |
| | Effective Signal Level at Main/AUX-Output during full-scale Digital Input Signal from $I^2S$ for Analog Volume at 0 dB (5-V Operation) | | 0.76 | 0.90 | 1.04 | $V_{RMS}$ | |

[1] “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

### 4.6.3.7. Sound IF Inputs

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $R_{IFIN}$ | Input Impedance | ANA_IN1+,<br>ANA_IN2+,<br>ANA_IN– | 1.5<br>6.8 | 2<br>9.1 | 2.5<br>11.4 | kΩ<br>kΩ | Gain AGC = 20 dB<br>Gain AGC = 3 dB |
| $DC_{VREFTOP}$ | DC Voltage at VREFTOP | VREFTOP | 2.45 | 2.65 | 2.75 | V | |
| $DC_{ANA_IN}$ | DC Voltage on IF Inputs | ANA_IN1+,<br>ANA_IN2+,<br>ANA_IN– | 1.3 | 1.5 | 1.7 | V | |
| $XTALK_{IF}$ | Crosstalk Attenuation | ANA_IN1+,<br>ANA_IN2+,<br>ANA_IN– | 40 | | | dB | $f_{signal}$ = 1 MHz<br>Input Level = –2 dBr |
| $BW_{IF}$ | 3 dB Bandwidth | | 10 | | | MHz | |
| AGC | AGC Step Width | | | 0.85 | | dB | |

### 4.6.3.8. Power Supply Rejection

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **PSRR: Rejection of Noise on AHVSUP at 1 kHz** | | | | | | | |
| PSRR | AGNDC | AGNDC | | 80 | | dB | |
| | From Analog Input to $I^2S$ Output | MONO_IN,<br>SCn_IN_s[1)] | | 70 | | dB | |
| | From Analog Input to SCART Output | MONO_IN,<br>SCn_IN_s[1)]<br>SCn_OUT_s[1)] | | 70 | | dB | |
| | From $I^2S$ Input to SCART Output | SCn_OUT_s[1)] | | 60 | | dB | |
| | From $I^2S$ Input to MAIN or AUX Output | DACp_s[1)] | | 80 | | dB | |

[1)] “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

### 4.6.3.9. Analog Performance

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Specifications for 8-V Operation** | | | | | | | |
| SNR | Signal-to-Noise Ratio | | | | | | |
| | from Analog Input to $I^2S$ Output | MONO_IN, SCn_IN_s[1)] | 85 | 88 | | dB | Input Level = –20 dB with resp. to $V_{AICL}$, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s[1)] → SCn_OUT_s[1)] | 93 | 96 | | dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...20 kHz |
| | from $I^2S$ Input to SCART Output | SCn_OUT_s[1)] | 85 | 88 | | dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...15 kHz |
| | from $I^2S$ Input to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB | DACp_s[1)] | 85 78 | 88 83 | | dB dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...15 kHz |
| THD | Total Harmonic Distortion | | | | | | |
| | from Analog Input to $I^2S$ Output | MONO_IN, SCn_IN_s[1)] | | 0.01 | 0.03 | % | Input Level = –3 dBr with resp. to $V_{AICL}$, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s → SCn_OUT_s[1)] | | 0.01 | 0.03 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...20 kHz |
| | from $I^2S$ Input to SCART Output | SCn_OUT_s[1)] | | 0.01 | 0.03 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |
| | from $I^2S$ Input to Main or AUX Output | DACA_s, DACM_s[1)] | | 0.01 | 0.03 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |

[1)] “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **Specifications for 5-V Operation** | | | | | | | |
| SNR | Signal-to-Noise Ratio | | | | | | |
| | from Analog Input to $I^2S$ Output | MONO_IN, SCn_IN_s[1)] | 82 | 85 | | dB | Input Level = –20 dB with resp. to $V_{AICL}$, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s[1)] → SCn_OUT_s[1)] | 90 | 93 | | dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...20 kHz |
| | from $I^2S$ Input to SCART Output | SCn_OUT_s[1)] | 82 | 85 | | dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...15 kHz |
| | from $I^2S$ Input to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB | DACp_s[1)] | 82 75 | 85 80 | | dB dB | Input Level = –20 dB, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...15 kHz |
| THD | Total Harmonic Distortion | | | | | | |
| | from Analog Input to $I^2S$ Output | MONO_IN, SCn_IN_s[1)] | | 0.03 | 0.1 | % | Input Level = –3 dBr with resp. to $V_{AICL}$, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s → SCn_OUT_s[1)] | | | 0.1 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...20 kHz |
| | from $I^2S$ Input to SCART Output | SCn_OUT_s[1)] | | | 0.1 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |
| | from $I^2S$ Input to Main or AUX Output | DACA_s, DACM_s[1)] | | | 0.1 | % | Input Level = –3 dBr, $f_{sig}$ = 1 kHz, equally weighted 20 Hz...16 kHz |

[1)] “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **XTALK Specifications for 8-V and 5-V Operation** | | | | | | | |
| XTALK | Crosstalk Attenuation<br>– PLCC68<br>– PSDIP64 | | | | | | Input Level = –3 dB, $f_{sig}$ = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ |
| | between left and right channel within SCART Input/Output pair (L→R, R→L) | | | | | | equally weighted 20 Hz...20 kHz |
| | SCn_IN → SCn_OUT[1)] | PLCC68<br>PSDIP64 | 80<br>80 | | | dB<br>dB | |
| | SC1_IN or SC2_IN → $I^2S$ Output | PLCC68<br>PSDIP64 | 80<br>80 | | | dB<br>dB | |
| | SC3_IN → $I^2S$ Output | PLCC68<br>PSDIP64 | 80<br>80 | | | dB<br>dB | |
| | $I^2S$ Input → SCn_OUT[1)] | PLCC68<br>PSDIP64 | 80<br>80 | | | dB<br>dB | |
| | between left and right channel within Main or AUX Output pair | | | | | | equally weighted 20 Hz...16 kHz |
| | $I^2S$ Input → DACp[1)] | PLCC68<br>PSDIP64 | 80<br>75 | | | dB<br>dB | |
| | between SCART Input/Output pairs<br>D = disturbing program<br>O = observed program | | | | | | (equally weighted 20 Hz...20 kHz same signal source on left and right disturbing channel, effect on each observed output channel |
| | D: MONO/SCn_IN → SCn_OUT<br>O: MONO/SCn_IN → SCn_OUT[1)] | PLCC68<br>PSDIP64 | 100<br>100 | | | dB<br>dB | |
| | D: MONO/SCn_IN → SCn_OUT or unsel.<br>O: MONO/SCn_IN → $I^2S$ Output | PLCC68<br>PSDIP64 | 100<br>95 | | | dB<br>dB | |
| | D: MONO/SCn_IN → SCn_OUT<br>O: $I^2S$ Input → SCn_OUT[1)] | PLCC68<br>PSDIP64 | 100<br>100 | | | dB<br>dB | |
| | D: MONO/SCn_IN → unselected<br>O: $I^2S$ Input → SC1_OUT[1)] | PLCC68<br>PSDIP64 | 100<br>100 | | | dB<br>dB | |
| | Crosstalk between Main and AUX Output pairs<br>$I^2S$ Input → DACp[1)] | PLCC68<br>PSDIP64 | 95<br>90 | | | dB<br>dB | (equally weighted 20 Hz...16 kHz) same signal source on left and right disturbing channel, effect on each observed output channel |
| XTALK | Crosstalk from Main or AUX Output to SCART Output and vice versa<br>D = disturbing program<br>O = observed program | | | | | | (equally weighted 20 Hz...20 kHz) same signal source on left and right disturbing channel, effect on each observed output channel |
| | D: MONO/SCn_IN/DSP → SCn_OUT<br>O: $I^2S$ Input → DACp[1)] | PLCC68<br>PSDIP64 | 85<br>80 | | | dB<br>dB | SCART output load resistance 10 kΩ |
| | D: MONO/SCn_IN/DSP → SCn_OUT<br>O: $I^2S$ Input → DACp[1)] | PLCC68<br>PSDIP64 | 90<br>85 | | | dB<br>dB | SCART output load resistance 30 kΩ |
| | D: $I^2S$ Input → DACp<br>O: MONO/SCn_IN → SCn_OUT[1)] | PLCC68<br>PSDIP64 | 100<br>95 | | | dB<br>dB | |
| | D: $I^2S$ Input → DACM<br>O: $I^2S$ Input → SCn_OUT[1)] | PLCC68<br>PSDIP64 | 100<br>95 | | | dB<br>dB | |

1) "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

### 4.6.3.10. Sound Standard Dependent Characteristics

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **NICAM Characteristics (MSP Standard Code = 8)** | | | | | | | |
| $dV_{NICAMOUT}$ | Tolerance of Output Voltage of NICAM Baseband Signal | DACp_s, SCn_OUT_s[1)] | –1.5 | | +1.5 | dB | 2.12 kHz, Modulator input level = 0 dBref |
| $S/N_{NICAM}$ | S/N of NICAM Baseband Signal | | 72 | | | dB | NICAM: –6 dB, 1 kHz, RMS unweighted<br>0 to 15 kHz, Vol = 9 dB<br>NIC_Presc = $7F_{hex}$<br>Output level 1 $V_{RMS}$ at DACp_s |
| $THD_{NICAM}$ | Total Harmonic Distortion + Noise of NICAM Baseband Signal | | | | 0.1 | % | 2.12 kHz, Modulator input level = 0 dBref |
| $BER_{NICAM}$ | NICAM: Bit Error Rate | | | | 1 | $10^{-7}$ | FM+NICAM, norm conditions |
| $fR_{NICAM}$ | NICAM Frequency Response , 20...15000 Hz | | –1.0 | | +1.0 | dB | Modulator input level = –12 dB dBref; RMS |
| $XTALK_{NICAM}$ | NICAM Crosstalk Attenuation (Dual) | | 80 | | | dB | |
| $SEP_{NICAM}$ | NICAM Channel Separation (Stereo) | | 80 | | | dB | |
| **FM Characteristics (MSP Standard Code = 3)** | | | | | | | |
| $dV_{FMOUT}$ | Tolerance of Output Voltage of FM Demodulated Signal | DACp_s, SCn_OUT_s[1)] | –1.5 | | +1.5 | dB | 1 FM-carrier, 50 µs, 1 kHz, 40 kHz deviation; RMS |
| $S/N_{FM}$ | S/N of FM Demodulated Signal | | 73 | | | dB | 1 FM-carrier 5.5 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS, unweighted<br>0 to 15 kHz (for S/N);<br>full input range, FM-Prescale = $46_{hex}$, Vol = 0 dB<br>→ Output Level 1 $V_{RMS}$ at DACp_s |
| $THD_{FM}$ | Total Harmonic Distortion + Noise of FM Demodulated Signal | | | | 0.1 | % | |
| $fR_{FM}$ | FM Frequency Response 20...15000 Hz | | –1.0 | | +1.0 | dB | 1 FM-carrier 5.5 MHz, 50 µs, Modulator input level = –14.6 dBref; RMS |
| $XTALK_{FM}$ | FM Crosstalk Attenuation (Dual) | | 80 | | | dB | 2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; Bandpass 1 kHz |
| $SEP_{FM}$ | FM Channel Separation (Stereo) | DACp_s, SCn_OUT_s[1)] | 50 | | | dB | 2 FM-carriers 5.5/5.74 MHz, 50 µs, 1 kHz, 40 kHz deviation; RMS |
| **AM Characteristics (MSP Standard Code = 9)** | | | | | | | |
| $S/N_{AM(1)}$ | S/N of AM Demodulated Signal measurement condition: RMS/Flat<br>MSP 34x1G Version A1<br>MSP 34x1G Version A2 and later | DACp_s, SCn_OUT_s[1)] | <br>44<br>55 | | | <br>dB<br>dB | SIF level: 0.1–0.8 $V_{pp}$<br>AM-carrier 54% at 6.5 MHz<br>Vol = 0 dB, FM/AM prescaler set for output = 0.5 $V_{RMS}$ at Loudspeaker out;<br>Standard Code = $09_{hex}$<br>no video/chroma components |
| $S/N_{AM(2)}$ | S/N of AM Demodulated Signal measurement condition: QP/CCIR<br>MSP 34x1G Version A1<br>MSP 34x1G Version A2 and later | | <br>35<br>45 | | | <br>dB<br>dB | |
| $THD_{AM}$ | Total Harmonic Distortion + Noise of AM Demodulated Signal<br>MSP 34x1G Version A1<br>MSP 34x1G Version A2 and later | | | | <br>0.8<br>0.6 | <br>%<br>% | |
| $fR_{RM}$ | RM Frequency Response 50...12000 Hz | | –2.5 | | +1.0 | dB | |

1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “Loudspeaker (Main)’’ or ‘‘Headphone (AUX)’’

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **BTSC Characteristics (MSP Standard Code = $20_{hex}$, $21_{hex}$)** | | | | | | | |
| $S/N_{BTSC}$ | S/N of BTSC Stereo Signal<br>S/N of BTSC-SAP Signal | DACp_s, SCn_OUT_s[1] | 68<br>57 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{BTSC}$ | THD+N of BTSC Stereo Signal<br>THD+N of BTSC SAP Signal | | | | 0.1<br>0.5 | %<br>% | 1 kHz L or R or SAP, 100% 75 µs EIM[2], DBX NR, RMS unweighted 0 to 15 kHz |
| $fR_{BTSC}$ | Frequency Response of BTSC Stereo, 50 Hz...12 kHz<br>Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | –0.5<br>–1.0 | | 0.5<br>0.6 | dB<br>dB | L or R or SAP, 1%...66% EIM[2], DBX NR |
| $XTALK_{BTSC}$ | Stereo → SAP<br>SAP → Stereo | | 76<br>80 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz |
| $SEP_{BTSC}$ | Stereo Separation<br>50 Hz...10 kHz<br>50 Hz...12 kHz | | <br>35<br>30 | | | <br>dB<br>dB | L or R 1%...66% EIM[2], DBX NR |
| $FM_{pil}$ | Pilot deviation threshold<br>Stereo off → on<br>Stereo on → off | ANA_IN1+, ANA_IN2+ | <br>3.2<br>1.2 | | <br>3.5<br>1.5 | <br>kHz<br>kHz | 4.5 MHz carrier modulated with $f_h$ = 15.743 kHz<br>SIF level = 100 $mV_{pp}$<br>indication: STATUS Bit[6] |
| $f_{Pilot}$ | Pilot Frequency Range | ANA_IN1+<br>ANA_IN2+ | 15.563 | | 15.843 | kHz | standard BTSC stereo signal, sound carrier only |
| **BTSC Characteristics (MSP Standard Code = $20_{hex}$, $21_{hex}$) with a minimum IF input signal level of 70 mVpp (measured without any video/chroma signal components)** | | | | | | | |
| $S/N_{BTSC}$ | S/N of BTSC Stereo Signal<br>S/N of BTSC-SAP Signal | DACp_s, SCn_OUT_s[1] | 64<br>55 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{BTSC}$ | THD+N of BTSC Stereo Signal<br>THD+N of BTSC SAP Signal | | | | 0.15<br>0.8 | %<br>% | 1 kHz L or R or SAP, 100% 75 µs EIM[2], DBX NR, RMS unweighted 0 to 15 kHz |
| $fR_{BTSC}$ | Frequency Response of BTSC Stereo, 50 Hz...12 kHz<br>Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | –0.5<br>–1.0 | | 0.5<br>0.6 | dB<br>dB | L or R or SAP, 1%...66% EIM[2], DBX NR |
| $XTALK_{BTSC}$ | Stereo → SAP<br>SAP → Stereo | | 75<br>75 | | | dB<br>dB | 1 kHz L or R or SAP, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz |
| $SEP_{BTSC}$ | Stereo Separation<br>50 Hz...10 kHz<br>50 Hz...12 kHz | | <br>35<br>30 | | | <br>dB<br>dB | L or R 1%...66% EIM[2], DBX NR |

[1] "n" means "1", "2", "3", or "4"; "s" means "L" or "R"; "p" means "M" or "A"

[2] EIM refers to 75-µs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-µs preemphasis network.

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| **EIA-J Characteristics (MSP Standard Code = $30_{hex}$)** | | | | | | | |
| $S/N_{EIAJ}$ | S/N of EIA-J Stereo Signal<br>S/N of EIA-J Sub-Channel | DACp_s, SCn_OUT_s[1)] | 60<br>60 | | | dB<br>dB | 1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{EIAJ}$ | THD+N of EIA-J Stereo Signal<br>THD+N of EIA-J Sub-Channel | | | | 0.2<br>0.3 | %<br>% | |
| $fR_{EIAJ}$ | Frequency Response of EIA-J Stereo, 50 Hz...12 kHz<br>Frequency Response of EIA-J Sub-Channel, 50 Hz...12 kHz | | –0.5<br>–1.0 | | 0.5<br>0.5 | dB<br>dB | 100% modulation, 75 µs deemphasis |
| $XTALK_{EIAJ}$ | Main → SUB<br>Sub → MAIN | | 66<br>80 | | | dB<br>dB | 1 kHz L or R, 100% modulation, 75 µs deemphasis, Bandpass 1 kHz |
| $SEP_{EIAJ}$ | Stereo Separation<br>50 Hz...5 kHz<br>50 Hz...10 kHz | | <br>35<br>28 | | | <br>dB<br>dB | EIA-J Stereo Signal, L or R 100% modulation |
| **FM-Radio Characteristics (MSP Standard Code = $40_{hex}$)** | | | | | | | |
| $S/N_{UKW}$ | S/N of FM-Radio Stereo Signal | DACp_s, SCn_OUT_s[1)] | 68 | | | dB | 1 kHz L or R, 100% modulation, 75 µs deemphasis, RMS unweighted 0 to 15 kHz |
| $THD_{UKW}$ | THD+N of FM-Radio Stereo Signal | | | | 0.1 | % | |
| $fR_{UKW}$ | Frequency Response of FM-Radio Stereo 50 Hz...15 kHz | | <br>–1.0 | | <br>+0.5 | <br>dB | L or R, 1%...100% modulation, 75 µs deemphasis |
| $SEP_{UKW}$ | Stereo Separation 50 Hz...15 kHz | | 45 | | | dB | |
| $f_{Pilot}$ | Pilot Frequency Range | ANA_IN1+ ANA_IN2+ | 18.844 | | 19.125 | kHz | standard FM radio stereo signal |

[1)] “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R”; “p” means “M” or “A”

## 5. Appendix A: Overview of TV-Sound Standards

### 5.1. NICAM 728

**Table 5–1:** Summary of NICAM 728 sound modulation parameters

| Specification | I | B/G | L | | D/K | |
|---|---|---|---|---|---|---|
| Carrier frequency of digital sound | 6.552 MHz | 5.85 MHz | 5.85 MHz | | 5.85 MHz | |
| Transmission rate | 728 kbit/s | | | | | |
| Type of modulation | Differentially encoded quadrature phase shift keying (DQPSK) | | | | | |
| Spectrum shaping Roll-off factor | by means of Roll-off filters | | | | | |
| | 1.0 | 0.4 | 0.4 | | 0.4 | |
| Carrier frequency of analog sound component | 6.0 MHz FM mono | 5.5 MHz FM mono | 6.5 MHz AM mono | | 6.5 MHz FM mono | |
| | | | terrestrial | cable | | |
| Power ratio between vision carrier and analog sound carrier | 10 dB | 13 dB | 10 dB | 16 dB | 13 dB | |
| Power ratio between analog and modulated digital sound carrier | 10 dB | 7 dB | 17 dB | 11 dB | China/Hungary | Poland |
| | | | | | 12 dB | 7 dB |

**Table 5–2:** Summary of NICAM 728 sound coding characteristics

| Characteristics | Values |
|---|---|
| Audio sampling frequency | 32 kHz |
| Number of channels | 2 |
| Initial resolution | 14 bit/sample |
| Companding characteristics | near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks |
| Coding for compressed samples | 2’s complement |
| Preemphasis | CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz) |
| Audio overload level | +12 dBm measured at the unity gain frequency of the preemphasis network (2 kHz) |

### 5.2. A2-Systems

**Table 5–3:** Key parameters for A2 Systems of Standards B/G, D/K, and M

| **Characteristics** | **Sound Carrier FM1** | | | **Sound Carrier FM2** | | |
|---|---|---|---|---|---|---|
| TV-Sound Standard | **B/G** | **D/K** | **M** | **B/G** | **D/K** | **M** |
| Carrier frequency in MHz | 5.5 | 6.5 | 4.5 | 5.7421875 | 6.2578125<br>6.7421875<br>5.7421875 | 4.724212 |
| Vision/sound power difference | 13 dB | | | 20 dB | | |
| Sound bandwidth | 40 Hz to 15 kHz | | | | | |
| Preemphasis | 50 µs | | 75 µs | 50 µs | | 75 µs |
| Frequency deviation (nom/max) | ±27/±50 kHz | | ±17/±25 kHz | ±27/±50 kHz | | ±15/±25 kHz |
| **Transmission Modes** | | | | | | |
| Mono transmission | mono | | | mono | | |
| Stereo transmission | (L+R)/2 | | (L+R)/2 | R | | (L–R)/2 |
| Dual sound transmission | language A | | | language B | | |
| **Identification of Transmission Mode** | | | | | | |
| Pilot carrier frequency | | | | 54.6875 kHz | | 55.0699 kHz |
| Max. deviation portion | | | | ±2.5 kHz | | |
| Type of modulation / modulation depth | | | | AM / 50% | | |
| Modulation frequency | | | | mono: unmodulated<br>stereo: 117.5 Hz<br>dual: 274.1 Hz | | <br>149.9 Hz<br>276.0 Hz |

### 5.3. BTSC-Sound System

**Table 5–4:** Key parameters for BTSC-Sound Systems

| | Aural Carrier | BTSC-MPX-Components | | | | |
|---|---|---|---|---|---|---|
| | | (L+R) | Pilot | (L–R) | SAP | Prof. Ch. |
| Carrier frequency ($f_{hNTSC}$ = 15.734 kHz) ($f_{hPAL}$ = 15.625 kHz) | 4.5 MHz | Baseband | $f_h$ | 2 $f_h$ | 5 $f_h$ | 6.5 $f_h$ |
| Sound bandwidth in kHz | | 0.05 - 15 | | 0.05 - 15 | 0.05 - 12 | 0.05 - 3.4 |
| Preemphasis | | 75 µs | | DBX | DBX | 150 µs |
| Max. deviation to Aural Carrier | 73 kHz (total) | 25 kHz[1)] | 5 kHz | 50 kHz[1)] | 15 kHz | 3 kHz |
| Max. Freq. Deviation of Subcarrier Modulation Type | | | | AM | 10 kHz FM | 3 kHz FM |
| [1)] Sum does not exceed 50 kHz due to interleaving effects | | | | | | |

### 5.4. Japanese FM Stereo System (EIA-J)

**Table 5–5:** Key parameters for Japanese FM-Stereo Sound System EIA-J

| | Aural Carrier FM | EIA-J-MPX-Components | | |
|---|---|---|---|---|
| | | (L+R) | (L–R) | Identification |
| Carrier frequency ($f_h$ = 15.734 kHz) | 4.5 MHz | Baseband | 2 $f_h$ | 3.5 $f_h$ |
| Sound bandwidth | | 0.05 - 15 kHz | 0.05 - 15 kHz | – |
| Preemphasis | | 75 µs | 75 µs | none |
| Max. deviation portion to Aural Carrier | 47 kHz | 25 kHz | 20 kHz | 2 kHz |
| Max. Freq. Deviation of Subcarrier Modulation Type | | | 10 kHz FM | 60% AM |
| Transmitter-sided delay | | 20 µs | 0 µs | 0 µs |
| Mono transmission | | L+R | – | unmodulated |
| Stereo transmission | | L+R | L–R | 982.5 Hz |
| Bilingual transmission | | Language A | Language B | 922.5 Hz |

### 5.5. FM Satellite Sound

**Table 5–6:** Key parameters for FM Satellite Sound

| Carrier Frequency | Maximum FM Deviation | Sound Mode | Bandwidth | Deemphasis |
|---|---|---|---|---|
| 6.5 MHz | 85 kHz | Mono | 15 kHz | 50 µs |
| 7.02/7.20 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |
| 7.38/7.56 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |
| 7.74/7.92 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |

### 5.6. FM-Stereo Radio

**Table 5–7:** Key parameters for FM-Stereo Radio Systems

| | Aural Carrier | FM-Radio-MPX-Components | | | |
|---|---|---|---|---|---|
| | | (L+R) | Pilot | (L–R) | RDS/ARI |
| Carrier frequency ($f_p$ = 19 kHz) | 10.7 MHz | Baseband | $f_p$ | 2 $f_p$ | 3 $f_h$ |
| Sound bandwidth in kHz | | 0.05 - 15 | | 0.05 - 15 | |
| Preemphasis:<br>– USA<br>– Europe | | <br>75 µs<br>50 µs | | <br>75 µs<br>50 µs | |
| Max. deviation to Aural Carrier | 75 kHz (100%) | 90% | 10% | 90% | 5% |

## 6. Appendix B: Manual/Compatibility Mode

To adapt the modes of the STANDARD SELECT register to individual requirements and for reasons of **compatibility to the MSP 34x0D,** the MSP 34x1G offers an Manual/Compatibility Mode, which provides sophisticated programming of the MSP 34x1G.

Using the STANDARD SELECT register generally provides a more economic way to program the MSP 34x1G and will result in optimal behavior. **Therefore, it is not recommended to use the Manual/Compatibility mode.** Only in those cases, where compatibility with MSP 34x0D is strictly required, should the Manual/Compatibility mode be used.

**Note:** In case of Automatic Sound Select (MODUS[0]=1), any modifications of the demodulator write registers listed below, except AUTO_FM/AM, are ignored.

### 6.1. Demodulator Write and Read Registers for Manual/Compatibility Mode

**Table 6–1:** Demodulator Write Registers; Subaddress: $10_{hex}$; these registers are not readable!

| Demodulator Write Registers | Address (hex) | MSP-Version | Description | Reset Mode | Page |
|---|---|---|---|---|---|
| AUTO_FM/AM | 00 21 | 3411, 3451[1)] | **1. MODUS[0]=1 (Automatic Sound Select):** Switching Level threshold of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception<br>**2. MODUS[0]=0 (Manual Mode):** Activation and configuration of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception | 00 00 | 86 |
| A2_Threshold | 00 22 | all | A2 Stereo Identification Threshold | 00 $19_{hex}$ | 87 |
| CM_Threshold | 00 24 | all | Carrier-Mute Threshold | 00 $2A_{hex}$ | 87 |
| AD_CV | 00 BB | all | SIF-input selection, configuration of AGC, and Carrier-Mute Function | 00 00 | 88 |
| MODE_REG | 00 83 | 3411, 3451[1)] | Controlling of MSP-Demodulator and Interface options. As soon as this register is applied, the MSP 34x1G works in the **MSP 34x0D Compatibility Mode.**<br>**Warning: In this mode, BTSC, EIA-J, and FM-Radio are disabled.** Only MSP 34x0D features are available; the use of MODUS and STATUS register is not allowed.<br>The MSP 34x1G is reset to the normal mode by first programming the MODUS register followed by transmitting a valid standard code to the STANDARD SELECTION register. | 00 00 | 89 |
| FIR1<br>FIR2 | 00 01<br>00 05 | | FIR1-filter coefficients channel 1 (6 · 8 bit)<br>FIR2-filter coefficients channel 2 (6 · 8 bit), + 3 · 8 bit offset (total 72 bit) | 00 00 | 91 |
| DCO1_LO<br>DCO1_HI<br>DCO2_LO<br>DCO2_HI | 00 93<br>00 9B<br>00 A3<br>00 AB | | Increment channel 1 Low Part<br>Increment channel 1 High Part<br>Increment channel 2 Low Part<br>Increment channel 2 High Part | 00 00 | 91 |
| PLL_CAPS | 00 1F | | Not of interest for the customer<br>Switchable PLL capacitors to tune open-loop frequency | 00 56 | 94 |

[1)] not in BTSC, EIA-J, and FM-Radio mode

**Table 6–2:** Demodulator Read Registers; Subaddress: $11_{hex}$; these registers are not writable!

| Demodulator Read Registers | Address (hex) | MSP-Version | Description | Page |
|---|---|---|---|---|
| C_AD_BITS | 00 23 | 3411, 3451 | NICAM-Sync bit, NICAM-C-Bits, and three LSBs of additional data bits | 93 |
| ADD_BITS | 00 38 | | NICAM: bit [10:3] of additional data bits | 93 |
| CIB_BITS | 00 3E | | NICAM: CIB1 and CIB2 control bits | 93 |
| ERROR_RATE | 00 57 | | NICAM error rate, updated with 182 ms | 94 |
| PLL_CAPS | 02 1F | | Not for customer use | 94 |
| AGC_GAIN | 02 1E | | Not for customer use | 94 |

### 6.2. DSP Write and Read Registers for Manual/Compatibility Mode

**Table 6–3:** DSP-Write Registers; Subaddress: $12_{hex}$, all registers are readable as well

| Write Register | Address (hex) | Bits | Operational Modes and Adjustable Range | Reset Mode | Page |
|---|---|---|---|---|---|
| Volume SCART1 channel: Ctrl. mode | 00 07 | [7..0] | [Linear mode / logarithmic mode] | $00_{hex}$ | 95 |
| FM Fixed Deemphasis | 00 0F | [15..8] | [50 µs, 75 µs, OFF] | 50 µs | 95 |
| FM Adaptive Deemphasis | | [7..0] | [OFF, WP1] | OFF | 95 |
| Identification Mode | 00 15 | [7..0] | [B/G, M] | B/G | 96 |
| FM DC Notch | 00 17 | [7..0] | [ON, OFF] | ON | 96 |
| Volume SCART2 channel: Ctrl. mode | 00 40 | [7..0] | [Linear mode / logarithmic mode] | $00_{hex}$ | 95 |

**Table 6–4:** DSP Read Registers; Subaddress: $13_{hex}$, all registers are not writable

| Additional Read Registers | Address (hex) | Bits | Output Range | | Page |
|---|---|---|---|---|---|
| Stereo detection register for A2 Stereo Systems | 00 18 | [15..8] | [$80_{hex}$ ... $7F_{hex}$] | 8 bit two's complement | 96 |
| DC level readout FM1/Ch2-L | 00 1B | [15..0] | [$8000_{hex}$ ... $7FFF_{hex}$] | 16 bit two's complement | 96 |
| DC level readout FM2/Ch1-R | 00 1C | [15..0] | [$8000_{hex}$ ... $7FFF_{hex}$] | 16 bit two's complement | 96 |

### 6.3. Manual/Compatibility Mode: Description of Demodulator Write Registers

#### 6.3.1. Automatic Switching between NICAM and Analog Sound

In case of bad NICAM reception or loss of the NICAM-carrier, the MSP 34x1G offers an Automatic Switching (fall back) to the analog sound (FM/AM-Mono), without the necessity of the controller reading and evaluating any parameters. If a proper NICAM signal returns, switching back to this source is performed automatically as well. The feature evaluates the NICAM ERROR_RATE and switches, if necessary, all output channels which are assigned to the NICAM source, to the analog source, and vice versa.

An appropriate hysteresis algorithm avoids oscillating effects (see Fig. 6–1). STATUS[9] and C_AD_BITS[11] (Addr: 0023 hex) provide information about the actual NICAM-FM/AM-status.

##### 6.3.1.1. Function in Automatic Sound Select Mode

The Automatic Sound Select feature (MODUS[0]=1) includes the procedure mentioned above. By default, the internal ERROR_RATE threshold is set to $700_{dec}$. i.e. :

– NICAM → analog Sound if ERROR_RATE > 700

– analog Sound → NICAM if ERROR_RATE < 700/2

The ERROR_RATE value of 700 corresponds to a BER of approximately $5.46*10^{-3}$/s.

Individual configuration of the threshold can be done using Table 6–5, whereby the bits 0 and 11 of AUTO_FM are ignored. It is recommended to use the internal setting used by the standard selection.

The optimum NICAM sound can be assigned to the MSP output channels by selecting one of the “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels.

##### 6.3.1.2. Function in Manual Mode

If the manual mode (MODUS[0]=0) is required, the activation and configuration of the Automatic Switching feature has to be done as described in Table 6–5. Note, that the channel matrix of the corresponding output channels must be set according to the NICAM mode and need not to be changed in the FM/AM-fallback case.

**Example:**
Required threshold = 500: bits [10:1]=00 1111 1010

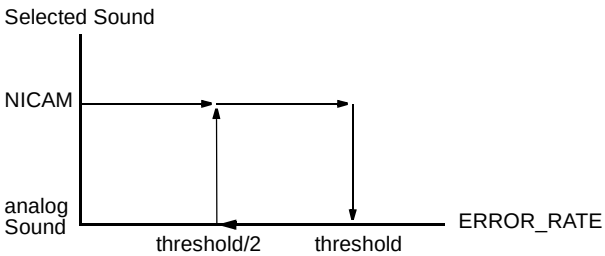



**Fig. 6–1:** Hysteresis for Automatic Switching

**Table 6–5:** Coding of Automatic NICAM/Analog Sound Switching; Reset Status: Mode 0

| Mode | Description | AUTO_FM [11:0] Addr. = 00 $21_{hex}$ | ERROR_RATE-Threshold/dec | Source Select: Input at NICAM Path[1)] |
|---|---|---|---|---|
| 0 | Compatible to MSP 3410B, i.e. automatic switching is disabled | Bit [0] = 0<br>Bits [10:1] = 0<br>Bit [11] = 0 | none | always NICAM; Mute in case of no NICAM available |
| 1 | Automatic Switching with **internal** threshold (Default, if Automatic Sound Select is on) | Bit [0] = 1<br>Bit [10:1] = 0<br>Bit [11] = 0 | 700 | NICAM or FM/AM, depending on ERROR_RATE |
| 2 | Automatic Switching with **external** threshold (Customizing of Automatic Sound Select) | Bit [0] = 1<br>Bit [10:1] = 25..1000 = threshold/2<br>Bit [11] = 0 | set by customer; recommended range: 50...2000 | |
| 3 | Forced analog mono mode, i.e. Automatic Switching is disabled (Customizing of Automatic Sound Select) | Bit [0] = 1<br>Bit [10:1] = 0<br>Bit [11] = 1 | none | always FM/AM |
| 1) In case of Automatic Sound Select (MODUS[0] = 1), the NICAM path may be assigned to “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels (see Table 2–2 on page 12). | | | | |
| In case of Automatic Sound Select (MODUS[0] = 1), bit [0] of AUTO_FM is ignored | | | | |

### 6.3.2. A2 Threshold

The threshold between Stereo/Bilingual and Mono Identification for the A2 Standard has been made programmable according to the user's preferences. An internal hysteresis ensures robustness and stability.

**Table 6–6:** Write Register on $I^2C$ Subaddress $10_{hex}$ : A2 Threshold

| Register Address | Function | Name |
|---|---|---|
| **THRESHOLDS** | | |
| 00 $22_{hex}$ (write) | **A2 THRESHOLD Register**<br>Defines threshold of all A2 and EIA_J standards for Stereo and Bilingual detection<br>bit [11..0] $7F0_{hex}$ force Mono Identification<br>...<br>$190_{hex}$ default setting after reset<br>...<br>$0A0_{hex}$ minimum Threshold for stable detection<br>bit [15..12] must be set to 0<br>recommended range : $0A0_{hex}$...$3C0_{hex}$ | A2_THRESH |

### 6.3.3. Carrier-Mute Threshold

The Carrier-Mute threshold has been made programmable according to the user's preferences. An internal hysteresis ensures stable behavior.

**Table 6–7:** Write Register on $I^2C$ Subaddress $10_{hex}$ : Carrier-Mute Threshold

| Register Address | Function | Name |
|---|---|---|
| **THRESHOLDS** | | |
| 00 $24_{hex}$ (write) | **Carrier-Mute THRESHOLD Register**<br>Defines threshold for the carrier mute feature<br>bit [6..0] $00_{hex}$ Carrier-Mute always ON (both channels muted)<br>...<br>$2A_{hex}$ default setting after reset<br>...<br>$7F_{hex}$ Carrier-Mute always OFF (both channels forced on)<br>bit [15..7] must be set to 0<br>recommended range : $14_{hex}$...$50_{hex}$ | CM_THRESH |

### 6.3.4. Register AD_CV

The use of this register is no longer recommended. Use it only in cases where compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x1G.

**Table 6–8:** AD_CV Register; reset status: all bits are “0”

| **AD_CV** (00 $BB_{hex}$) | | | **Automatic setting by STANDARD SELECT Register** | |
|---|---|---|---|---|
| **Bit** | **Function** | **Settings** | **2-8, 0A-60$_{hex}$** | **9** |
| [0] | not used | must be set to 0 | 0 | 0 |
| [1–6] | Reference level in case of Automatic Gain Control = on (see Table 6–9). Constant gain factor when Automatic Gain Control = off (see Table 6–10). | | 101000 | 100011 |
| [7] | Determination of Automatic Gain or Constant Gain | 0 = constant gain<br>1 = automatic gain | 1 | 1 |
| [8] | Selection of Sound IF source (identical to MODUS[8]) | 0 = ANA_IN1+<br>1 = ANA_IN2+ | X | X |
| [9] | MSP-Carrier-Mute Feature | 0 = off: no mute<br>1 = on: mute as described in section 2.2.2. | 1 | 0 |
| [10–15] | not used | must be set to 0 | 0 | 0 |
| X : not affected while choosing the TV sound standard by means of the STANDARD SELECT Register | | | | |

**Table 6–9:** Reference Values for Active AGC (AD_CV[7] = 1)

| **Application** | **Input Signal Contains** | **AD_CV [6:1] Ref. Value** | **AD_CV [6:1] in integer** | **Range of Input Signal at pin ANA_IN1+ and ANA_IN2+** |
|---|---|---|---|---|
| Terrestrial TV | | | | |
| – FM Standards | 1 or 2 FM Carriers | 101000 | 40 | 0.10 – 3 $V_{pp}$[1)] |
| – NICAM/FM | 1 FM and 1 NICAM Carrier | 101000 | 40 | 0.10 – 3 $V_{pp}$[1)] |
| – NICAM/AM | 1 AM and 1 NICAM Carrier | 100011 | 35 | 0.10 – 1.4 $V_{pp}$ (recommended: 0.10 – 0.8 $V_{pp}$) |
| – NICAM only | 1 NICAM Carrier only | 010100 | 20 | 0.05 – 1.0 $V_{pp}$ |
| SAT | 1 or more FM Carriers | 100011 | 35 | 0.10 – 3 $V_{pp}$[1)] |
| ADR | FM and ADR carriers | see DRP 3510A data sheet | | |

1) For signals above 1.4 $V_{pp}$, the minimum gain of 3 dB is switched, and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 $V_{pp}$, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N ratio of about 10 dB may appear.

**Table 6–10:** AD_CV parameters for Constant Input Gain (AD_CV[7]=0)

| Step | AD_CV [6:1] Constant Gain | Gain | Input Level at pin ANA_IN1+ and ANA_IN2+ |
|---|---|---|---|
| 0 | 000000 | 3.00 dB | maximum input level: 3 $V_{pp}$ (FM) or 1 $V_{pp}$ (NICAM)[1)] |
| 1 | 000001 | 3.85 dB | |
| 2 | 000010 | 4.70 dB | |
| 3 | 000011 | 5.55 dB | |
| 4 | 000100 | 6.40 dB | |
| 5 | 000101 | 7.25 dB | |
| 6 | 000110 | 8.10 dB | |
| 7 | 000111 | 8.95 dB | |
| 8 | 001000 | 9.80 dB | |
| 9 | 001001 | 10.65 dB | |
| 10 | 001010 | 11.50 dB | |
| 11 | 001011 | 12.35 dB | |
| 12 | 001100 | 13.20 dB | |
| 13 | 001101 | 14.05 dB | |
| 14 | 001110 | 14.90 dB | |
| 15 | 001111 | 15.75 dB | |
| 16 | 010000 | 16.60 dB | |
| 17 | 010001 | 17.45 dB | |
| 18 | 010010 | 18.30 dB | |
| 19 | 010011 | 19.15 dB | |
| 20 | 010100 | 20.00 dB | maximum input level: 0.14 $V_{pp}$ |

[1)] For signals above 1.4 $V_{pp}$, the minimum gain of 3 dB is switched and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 $V_{pp}$, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N ratio of about 10 dB may appear.

### 6.3.5. Register MODE_REG

**Note:** The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x1G.

As soon as this register is applied, the MSP 34x1G works in the **MSP 34x0D Compatibility Mode**. In this mode: **BTSC, EIA-J, and FM-Radio are disabled**. Only MSP 34x0D features are available; the use of MODUS and STATUS register is not allowed. The MSP 34x1G is reset to the normal mode by first programming the MODUS register, followed by transmitting a valid standard code to the STANDARD SELECTION register.

The register ‘MODE_REG’ contains the control bits determining the operation mode of the MSP 34x1G in the MSP 34x0D Compatibility Mode; Table 6–11 explains all bit positions.

**Table 6–11:** Control word ‘MODE_REG’; reset status: all bits are “0”

| **MODE_REG 00 $83_{hex}$** | | | | **Automatic setting by STANDARD SELECT Register** | | |
|---|---|---|---|---|---|---|
| **Bit** | **Function** | **Comment** | **Definition** | **2 - 5** | **8, A, B** | **9** |
| [0] | not used | | 0 : must be used | 0 | 0 | 0 |
| [1] | DCTR_TRI | Digital control out 0/1 tri-state | 0 : active<br>1 : tri-state | X | X | X |
| [2] | I2S_TRI | $I^2S$ outputs tri-state (I2S_CL, I2S_WS, I2S_DA_OUT) | 0 : active<br>1 : tri-state | X | X | X |
| [3] | $I^2S$ Mode[1)] | Master/Slave mode of the $I^2S$ bus | 0 : Master<br>1 : Slave | X | X | X |
| [4] | I2S_WS Mode | WS due to the Sony or Philips-Format | 0 : Sony<br>1 : Philips | X | X | X |
| [5] | Audio_CL_OUT | Switch Audio_Clock_Output to tri-state | 0 : on<br>1 : tri-state | X | X | X |
| [6] | NICAM[1)] | Mode of MSP-Ch1 | 0 : FM<br>1 : Nicam | 0 | 1 | 1 |
| [7] | not used | | 0 : must be used | 0 | 0 | 0 |
| [8] | FM AM | Mode of MSP-Ch2 | 0 : FM<br>1 : AM | 0 | 0 | 1 |
| [9] | HDEV | High Deviation Mode (channel matrix must be sound A) | 0 : normal<br>1 : high deviation mode | 0 | 0 | 0 |
| [11:10] | not used | | 0 : must be used | 0 | 0 | 0 |
| [12] | MSP-Ch1 Gain | see also Table 6–13 | 0 : Gain = 6 dB<br>1 : Gain = 0 dB | 0 | 0 | 0 |
| [13] | FIR1-Filter Coeff. Set | see also Table 6–13 | 0 : use FIR1<br>1 : use FIR2 | 1 | 0 | 0 |
| [14] | ADR | Mode of MSP-Ch1/ ADR-Interface | 0 : normal mode/tri-state<br>1 : ADR-mode/active | 0 | 0 | 0 |
| [15] | AM-Gain | Gain for AM Demodulation | 0 : 0 dB (default. of MSPB)<br>1 :12 dB (recommended) | 1 | 1 | 1 |
| | | | | X: not affected by short-programming | | |

**Table 6–12:** Loading sequence for FIR-coefficients

| **FIR1 00 $01_{hex}$ (MSP-Ch1: NICAM/FM2)** | | | |
|---|---|---|---|
| **No.** | **Symbol Name** | **Bits** | **Value** |
| 1 | NICAM/FM2_Coeff. (5) | 8 | see Table 6–13 |
| 2 | NICAM/FM2_Coeff. (4) | 8 | |
| 3 | NICAM/FM2_Coeff. (3) | 8 | |
| 4 | NICAM/FM2_Coeff. (2) | 8 | |
| 5 | NICAM/FM2_Coeff. (1) | 8 | |
| 6 | NICAM/FM2_Coeff. (0) | 8 | |
| **FIR2 00 $05_{hex}$ (MSP-Ch2: FM1/AM)** | | | |
| **No.** | **Symbol Name** | **Bits** | **Value** |
| 1 | IMREG1 | 8 | $04_{hex}$ |
| 2 | IMREG1 / IMREG2 | 8 | $40_{hex}$ |
| 3 | IMREG2 | 8 | $00_{hex}$ |
| 4 | FM/AM_Coef (5) | 8 | see Table 6–13 |
| 5 | FM/AM_Coef (4) | 8 | |
| 6 | FM/AM_Coef (3) | 8 | |
| 7 | FM/AM_Coef (2) | 8 | |
| 8 | FM/AM_Coef (1) | 8 | |
| 9 | FM/AM_Coef (0) | 8 | |

### 6.3.6. FIR-Parameter, Registers FIR1 and FIR2

**Note:** The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x1G.

Data-shaping and/or FM/AM bandwidth limitation is performed by a pair of linear phase Finite Impulse Response filters (FIR-filter). The filter coefficients are programmable and are either configured automatically by the STANDARD SELECT register or written manually by the control processor via the control bus. Two not necessarily different sets of coefficients are required: one for MSP-Ch1 (NICAM or FM2) and one for MSP-Ch2 (FM1 = FM-mono). In Table 6–13 several coefficient sets are proposed.

To load the FIR-filters, the following data values are to be transferred **8 bits at a time embedded LSB-bound in a 16-bit word**.

The loading sequences must be obeyed. To change a coefficient set, the complete block FIR1 or FIR2 must be transmitted.

**Note:** For compatibility with MSP 3410B, IMREG1 and IMREG2 have to be transmitted. The value for IMREG1 and IMREG2 is 004. Due to the partitioning to 8-bit units, the values $04_{hex}$, $40_{hex}$, and $00_{hex}$ arise.

### 6.3.7. DCO-Registers

**Note:** The use of this register is no longer recommended. It should be used only in cases where software-compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x1G.

When selecting a TV-sound standard by means of the STANDARD SELECT register, all frequency tuning is performed automatically.

If manual setting of the tuning frequency is required, a set of 24-bit registers determining the mixing frequencies of the quadrature mixers can be written manually into the IC. In Table 6–14, some examples of DCO registers are listed. It is necessary to divide them up into low part and high part. The formula for the calculation of the registers for any chosen IF frequency is as follows:

$$INCR_{dec} = int(f/fs \cdot 2^{24})$$

with: int = integer function
f = IF frequency in MHz
$f_S$ = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required register values (DCO1_HI or _LO for MSP-Ch1, DCO2_HI or LO for MSP-Ch2).

**Table 6–13:** 8-bit FIR-coefficients (decimal integer); reset status: all coefficients are “0”

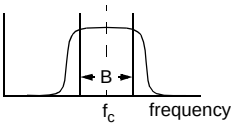
| **Coefficients for FIR1 00 $01_{hex}$ and FIR2 00 $05_{hex}$** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Terrestrial TV Standards** | | | | | | | **FM - Satellite** FIR filter corresponds to a band-pass with a band-width of B = 130 to 500 kHz   | | | | | | |
| | **B/G-, D/K-NICAM-FM** | | **I-NICAM-FM** | | **L-NICAM-AM** | | **B/G-, D/K-, M-Dual FM** | **130 kHz** | **180 kHz** | **200 kHz** | **280 kHz** | **380 kHz** | **500 kHz** | **Auto-search** |
| **Coef(i)** | **FIR1** | **FIR2** | **FIR1** | **FIR2** | **FIR1** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** | **FIR2** |
| **0** | –2 | 3 | 2 | 3 | –2 | –4 | 3 | 73 | 9 | 3 | –8 | –1 | –1 | –1 |
| **1** | –8 | 18 | 4 | 18 | –8 | –12 | 18 | 53 | 18 | 18 | –8 | –9 | –1 | –1 |
| **2** | –10 | 27 | –6 | 27 | –10 | –9 | 27 | 64 | 28 | 27 | 4 | –16 | –8 | –8 |
| **3** | 10 | 48 | –4 | 48 | 10 | 23 | 48 | 119 | 47 | 48 | 36 | 5 | 2 | 2 |
| **4** | 50 | 66 | 40 | 66 | 50 | 79 | 66 | 101 | 55 | 66 | 78 | 65 | 59 | 59 |
| **5** | 86 | 72 | 94 | 72 | 86 | 126 | 72 | 127 | 64 | 72 | 107 | 123 | 126 | 126 |
| **Mode-REG[12]** | 0 | | 0 | | 0 | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| **Mode-REG[13]** | 0 | | 0 | | 0 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| For compatibility, except for the FIR2-AM and the Autosearch-sets, the FIR-filter programming as used for the MSP 3410B is also possible. | | | | | | | | | | | | | | |
| ADR coefficients are listed in the DRP data sheet. | | | | | | | | | | | | | | |

**Table 6–14:** DCO registers for the MSP 34x1G; reset status: DCO_HI/LO = “0000”

| **DCO1_LO 00 $93_{hex}$, DCO1_HI 00 $9B_{hex}$; DCO2_LO 00 $A3_{hex}$, DCO2_HI 00 $AB_{hex}$** | | | | | |
|---|---|---|---|---|---|
| **Freq. MHz** | **DCO_HI/hex** | **DCO_LO/hex** | **Freq. MHz** | **DCO_HI/hex** | **DCO_LO/hex** |
| 4.5 | 03E8 | 000 | | | |
| 5.04<br>5.5<br>5.58<br>5.7421875 | 0460<br>04C6<br>04D8<br>04FC | 0000<br>038E<br>0000<br>00AA | 5.76<br>5.85<br>5.94 | 0500<br>0514<br>0528 | 0000<br>0000<br>0000 |
| 6.0<br>6.2<br>6.5<br>6.552 | 0535<br>0561<br>05A4<br>05B0 | 0555<br>0C71<br>071C<br>0000 | 6.6<br>6.65<br>6.8 | 05BA<br>05C5<br>05E7 | 0AAA<br>0C71<br>01C7 |
| 7.02 | 0618 | 0000 | 7.2 | 0640 | 0000 |
| 7.38 | 0668 | 0000 | 7.56 | 0690 | 0000 |

### 6.4. Manual/Compatibility Mode: Description of Demodulator Read Registers

**Note:** The use of these register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the STATUS register provides a more economic way to program the MSP 34x1G and to retrieve information from the IC.

All registers except C_AD_BITs are 8 bits wide. They can be read out of the RAM of the MSP 34x1G if the MSP 34x0D Compatibility Mode is required.

All transmissions take place in 16-bit words. The valid 8-bit data are the 8 LSBs of the received data word.

If the Automatic Sound Select feature is not used, the NICAM or FM-identification parameters must be read and evaluated by the controller in order to enable appropriate switching of the channel select matrix of the baseband processing part. The FM-identification registers are described in section 6.6.1. To handle the NICAM-sound and to observe the NICAM-quality, at least the registers C_AD_BITS and ERROR_RATE must be read and evaluated by the controller. Additional data bits and CIB bits, if supplied by the NICAM transmitter, can be obtained by reading the registers ADD_BITS and CIB_BITS.

#### 6.4.1. NICAM Mode Control/Additional Data Bits Register

NICAM operation mode control bits and A[2:0] of the additional data bits.

Format:

| MSB | | C_AD_BITS 00 $23_{hex}$ | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 11 | ... | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Auto _FM | ... | A[2] | A[1] | A[0] | C4 | C3 | C2 | C1 | S |

**Important:** “S” = Bit[0] indicates correct NICAM-synchronization (S = 1). If S = 0, the MSP 3411/3451G has not yet synchronized correctly to frame and sequence, or has lost synchronization. The remaining read registers are therefore not valid. The MSP mutes the NICAM output automatically and tries to synchronize again as long as MODE_REG[6] is set.

The operation mode is coded by C4-C1 as shown in Table 6–15.

**Table 6–15:** NICAM operation modes as defined by the EBU NICAM 728 specification

| C4 | C3 | C2 | C1 | Operation Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Stereo sound (NICAMA/B), independent mono sound (FM1) |
| 0 | 0 | 0 | 1 | Two independent mono signals (NICAMA, FM1) |
| 0 | 0 | 1 | 0 | Three independent mono channels (NICAMA, NICAMB, FM1) |
| 0 | 0 | 1 | 1 | Data transmission only; no audio |
| 1 | 0 | 0 | 0 | Stereo sound (NICAMA/B), FM1 carries same channel |
| 1 | 0 | 0 | 1 | One mono signal (NICAMA). FM1 carries same channel as NICAMA |
| 1 | 0 | 1 | 0 | Two independent mono channels (NICAMA, NICAMB). FM1 carries same channel as NICAMA |
| 1 | 0 | 1 | 1 | Data transmission only; no audio |
| x | 1 | x | x | Unimplemented sound coding option (not yet defined by EBU NICAM 728 specification) |
| AUTO_FM: monitor bit for the AUTO_FM Status:<br>0: NICAM source is NICAM<br>1: NICAM source is FM | | | | |

**Note:** It is no longer necessary to read out and evaluate the C_AD_BITS. All evaluation is performed in the MSP and indicated in the STATUS register.

#### 6.4.2. Additional Data Bits Register

Contains the remaining 8 of the 11 additional data bits. The additional data bits are not yet defined by the NICAM 728 system.

Format:

| MSB | | ADD_BITS 00 $38_{hex}$ | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| A[10] | A[9] | A[8] | A[7] | A[6] | A[5] | A[4] | A[3] |

#### 6.4.3. CIB Bits Register

CIB bits 1 and 2 (see NICAM 728 specifications).

Format:

| MSB | | CIB_BITS 00 $3E_{hex}$ | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| x | x | x | x | x | x | CIB1 | CIB2 |

### 6.4.4. NICAM Error Rate Register

| ERROR_RATE | 00 $57_{hex}$ |
|---|---|
| Error free | $0000_{hex}$ |
| maximum error rate | $07FF_{hex}$ |

Average error rate of the NICAM reception in a time interval of 182 ms, which should be close to 0. The initial and maximum value of ERROR_RATE is 2047. This value is also active if the NICAM bit of MODE_REG is not set. Since the value is achieved by filtering, a certain transition time (approx. 0.5 sec) is unavoidable. Acceptable audio may have error rates up to a value of 700 int. Individual evaluation of this value by the controller and an appropriate threshold may define the fallback mode from NICAM to FM/AM-Mono in case of poor NICAM reception.

The bit error rate per second (BER) can be calculated by means of the following formula:

BER = ERROR_RATE * $12.3*10^{-6}$ /s

### 6.4.5. PLL_CAPS Readback Register

It is possible to read out the actual setting of the PLL_CAPS. In standard applications, this register is not of interest for the customer.

| PLL_CAPS | 02 $1F_{hex}$ L | |
|---|---|---|
| minimum frequency | 1111 1111 | $FF_{hex}$ |
| nominal frequency | 0101 0110 RESET | $56_{hex}$ |
| maximum frequency | 0000 0000 | $00_{hex}$ |
| **PLL_CAPS** | **02 $1F_{hex}$ H** | |
| PLL open | xxxx xxx0 | |
| PLL closed | xxxx xxx1 | |

### 6.4.6. AGC_GAIN Readback Register

It is possible to read out the actual setting of AGC_GAIN in Automatic Gain Mode. In standard applications, this register is not of interest for the customer.

| AGC_GAIN | 02 $1E_{hex}$ | |
|---|---|---|
| max. amplification (20 dB) | 0001 0100 | $14_{hex}$ |
| min. amplification (3 dB) | 0000 0000 | $00_{hex}$ |

### 6.4.7. Automatic Search Function for FM-Carrier Detection in Satellite Mode

The AM demodulation ability of the MSP 34x1G offers the possibility to calculate the “field strength” of the momentarily selected FM carrier, which can be read out by the controller. In SAT receivers, this feature can be used to make automatic FM carrier search possible.

For this, the MSP has to be switched to AM-mode (MODE_REG[8]), FM-Prescale must be set to $7F_{hex} = +127_{dec}$, and the FM DC notch (see section 6.5.7.) must be switched off. The sound-IF frequency range must now be “scanned” in the MSP-channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz). After each incrementation, a field strength value is available at the quasi-peak detector output (quasi-peak detector source must be set to FM), which must be examined for relative maxima by the controller. This results in either continuing search or switching the MSP back to FM demodulation mode.

During the search process, the FIR2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth, resulting in appropriate field strength characteristics. The absolute field strength value (can be read out of “quasi-peak detector output FM1”) also gives information on whether a main FM carrier or a subcarrier was detected; and as a practical consequence, the FM bandwidth (FIR1/2) and the deemphasis (50 µs or adaptive) can be switched accordingly.

Due to the fact that a constant demodulation frequency offset of a few kHz leads to a DC level in the demodulated signal, further fine tuning of the found carrier can be achieved by evaluating the “DC Level Readout FM1”. Therefore, the FM DC Notch must be switched on, and the demodulator part must be switched back to FM-demodulation mode.

For a detailed description of the automatic search function, please refer to the corresponding MSP Windows software.

## 6.5. Manual/Compatibility Mode: Description of DSP Write Registers

### 6.5.1. Additional Channel Matrix Modes

| **Loudspeaker Matrix** | **00 $08_{hex}$** | **L** |
|---|---|---|
| **Headphone Matrix** | **00 $09_{hex}$** | **L** |
| **SCART1 Matrix** | **00 $0A_{hex}$** | **L** |
| **SCART2 Matrix** | **00 $41_{hex}$** | **L** |
| **$I^2S$ Matrix** | **00 $0B_{hex}$** | **L** |
| **Quasi-Peak Detector Matrix** | **00 $0C_{hex}$** | **L** |
| SUM/DIFF | 0100 0000 | $40_{hex}$ |
| AB_XCHANGE | 0101 0000 | $50_{hex}$ |
| PHASE_CHANGE_B | 0110 0000 | $60_{hex}$ |
| PHASE_CHANGE_A | 0111 0000 | $70_{hex}$ |
| A_ONLY | 1000 0000 | $80_{hex}$ |
| B_ONLY | 1001 0000 | $90_{hex}$ |

This table shows additional modes for the channel matrix registers.

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

### 6.5.2. Volume Modes of SCART1/2 Outputs

| **Volume Mode SCART1** | **00 $07_{hex}$** | **[3:0]** |
|---|---|---|
| **Volume Mode SCART2** | **00 $40_{hex}$** | **[3:0]** |
| linear | 0000 RESET | $0_{hex}$ |
| logarithmic | 0001 | $1_{hex}$ |

| **Linear Mode** | | |
|---|---|---|
| **Volume SCART1** | **00 $07_{hex}$** | **H** |
| **Volume SCART2** | **00 $40_{hex}$** | **H** |
| OFF | 0000 0000 RESET | $00_{hex}$ |
| 0 dB gain (digital full scale (FS) to 2 $V_{RMS}$ output) | 0100 0000 | $40_{hex}$ |
| +6 dB gain (–6 dBFS to 2 $V_{RMS}$ output) | 0111 1111 | $7F_{hex}$ |

**Note:** SCART Volume linear mode will not be supported in the future (documented for compatibility reasons only).

### 6.5.3. FM Fixed Deemphasis

| **FM Deemphasis** | **00 $0F_{hex}$** | **H** |
|---|---|---|
| 50 µs | 0000 0000 RESET | $00_{hex}$ |
| 75 µs | 0000 0001 | $01_{hex}$ |
| OFF | 0011 1111 | $3F_{hex}$ |

### 6.5.4. FM Adaptive Deemphasis

| **FM Adaptive Deemphasis WP1** | **00 $0F_{hex}$** | **L** |
|---|---|---|
| OFF | 0000 0000 RESET | $00_{hex}$ |
| WP1 | 0011 1111 | $3F_{hex}$ |

### 6.5.5. NICAM Deemphasis

A J17 Deemphasis is always applied to the NICAM signal. It is not switchable.

### 6.5.6. Identification Mode for A2 Stereo Systems

| Identification Mode | 00 $15_{hex}$ | L |
|---|---|---|
| Standard B/G (German Stereo) | 0000 0000 RESET | $00_{hex}$ |
| Standard M (Korean Stereo) | 0000 0001 | $01_{hex}$ |
| Reset of Ident-Filter | 0011 1111 | $3F_{hex}$ |

To shorten the response time of the identification algorithm after a program change between two FM-Stereo capable programs, the reset of the ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Set identification mode back to standard B/G or M
4. Read stereo detection register

### 6.5.7. FM DC Notch

The DC compensation filter (FM DC Notch) for FM input can be switched off. This is used to speed up the automatic search function (see Section 6.4.7.). In normal FM-mode, the FM DC Notch should be switched on.

| FM DC Notch | 00 $17_{hex}$ | L |
|---|---|---|
| ON | 0000 0000 Reset | $00_{hex}$ |
| OFF | 0011 1111 | $3F_{hex}$ |

## 6.6. Manual/Compatibility Mode: Description of DSP Read Registers

All readable registers are 16-bit wide. Transmissions via $I^2C$ bus have to take place in 16-bit words. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writable.

### 6.6.1. Stereo Detection Register for A2 Stereo Systems

| Stereo Detection Register | 00 $18_{hex}$ | H |
|---|---|---|
| Stereo Mode | Reading (two's complement) | |
| MONO | near zero | |
| STEREO | positive value (ideal reception: $7F_{hex}$) | |
| BILINGUAL | negative value (ideal reception: $80_{hex}$) | |

**Note:** It is no longer necessary to read out and evaluate the A2 identification level. All evaluation is performed in the MSP and indicated in the STATUS register.

### 6.6.2. DC Level Register

| DC Level Readout FM1 (MSP-Ch2) | 00 $1B_{hex}$ | H+L |
|---|---|---|
| DC Level Readout FM2 (MSP-Ch1) | 00 $1C_{hex}$ | H+L |
| DC Level | [$8000_{hex}$ ... $7FFF_{hex}$] values are 16 bit two's complement | |

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. A too low demodulation frequency (DCO) results in a positive DC-level and vice versa. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant $\tau$, defining the transition time of the DC Level Register, is approximately 28 ms.

## 6.7. Demodulator Source Channels in Manual Mode

### 6.7.1. Terrestric Sound Standards

Table 6–16 shows the source channel assignment of the demodulated signals in case of manual mode for all terrestric sound standards. See Table 2–2 for the assignment in the Automatic Sound Select mode. In manual mode for terrestric sound standards, only two demodulator sources are defined.

### 6.7.2. SAT Sound Standards

Table 6–17 shows the source channel assignment of the demodulated signals for SAT sound standards.

**Table 6–16:** Manual Sound Select Mode for Terrestric Sound Standards

| | | | | Source Channels of Sound Select Block | |
|---|---|---|---|---|---|
| **Broadcasted Sound Standard** | **Selected MSP Standard Code** | **Broadcasted Sound Mode** | **FM Matrix** | **FM/AM** (use 0 for channel select) | **Stereo or A/B** (use 1 for channel select) |
| B/G-FM<br>D/K-FM<br>M-Korea<br>M-Japan | 03<br>04, 05<br>02<br>30 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | German Stereo<br>Korean Stereo | Stereo | Stereo |
| | | BILINGUAL, Languages A and B | No Matrix | Left = A<br>Right = B | Left = A<br>Right = B |
| B/G-NICAM<br>L-NICAM<br>I-NICAM<br>D/K-NICAM<br>D/K-NICAM (with high deviation FM) | 08<br>09<br>0A<br>0B<br>0C | NICAM not available or NICAM error rate too high | Sound A Mono | analog Mono | no sound<br>with AUTO_FM: analog Mono |
| | | MONO | Sound A Mono | analog Mono | NICAM Mono |
| | | STEREO | Sound A Mono | analog Mono | NICAM Stereo |
| | | BILINGUAL, Languages A and B | Sound A Mono | analog Mono | Left = NICAM A<br>Right = NICAM B |
| BTSC | 20 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | Korean Stereo | Stereo | Stereo |
| | | MONO + SAP | Sound A Mono | Mono | Mono |
| | | STEREO + SAP | Korean Stereo | Stereo | Stereo |
| | 21 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | | | |
| | | MONO + SAP | No Matrix | Left = Mono<br>Right = SAP | Left = Mono<br>Right = SAP |
| | | STEREO + SAP | | | |
| FM-Radio | 40 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | Korean Stereo | Stereo | Stereo |

**Table 6–17:** Manual Sound Select Modes for SAT-Modes (FM Matrix is set automatically)

| | | | Source Channels of Sound Select Block for SAT-Modes | | | |
|---|---|---|---|---|---|---|
| **Broadcasted Sound Standard** | **Selected MSP Standard Code** | **Broadcasted Sound Mode** | **FM/AM** (source select: 0) | **Stereo or A/B** (source select: 1) | **Stereo or A** (source select: 3) | **Stereo or B** (source select: 4) |
| FM SAT | $6, 50_{hex}$ | MONO | Mono | Mono | Mono | Mono |
| | $51_{hex}$ | STEREO | Stereo | Stereo | Stereo | Stereo |
| | | BILINGUAL | Left = A (FM1)<br>Right = B (FM2) | Left = A (FM1)<br>Right = B (FM2) | A (FM1) | B (FM2) |

### 6.8. Exclusions of Audio Baseband Features

In general, all functions can be switched independently. Two exceptions exist:

1. NICAM cannot be processed simultaneously with the FM2 channel.
2. FM adaptive deemphasis cannot be processed simultaneously with FM-identification.

### 6.9. Phase Relationship of Analog Outputs

The analog output signals: Loudspeaker, headphone, and SCART2 all have the same phases. The user does not need to correct output phases when using these analog outputs directly. The SCART1 output has opposite phase.

Using the $I^2S$-outputs for other DSPs or D/A converters, care must be taken to adjust for the correct phase. If the attached coprocessor is one of the MSP family, the following schematics help to determine the phase relationship.

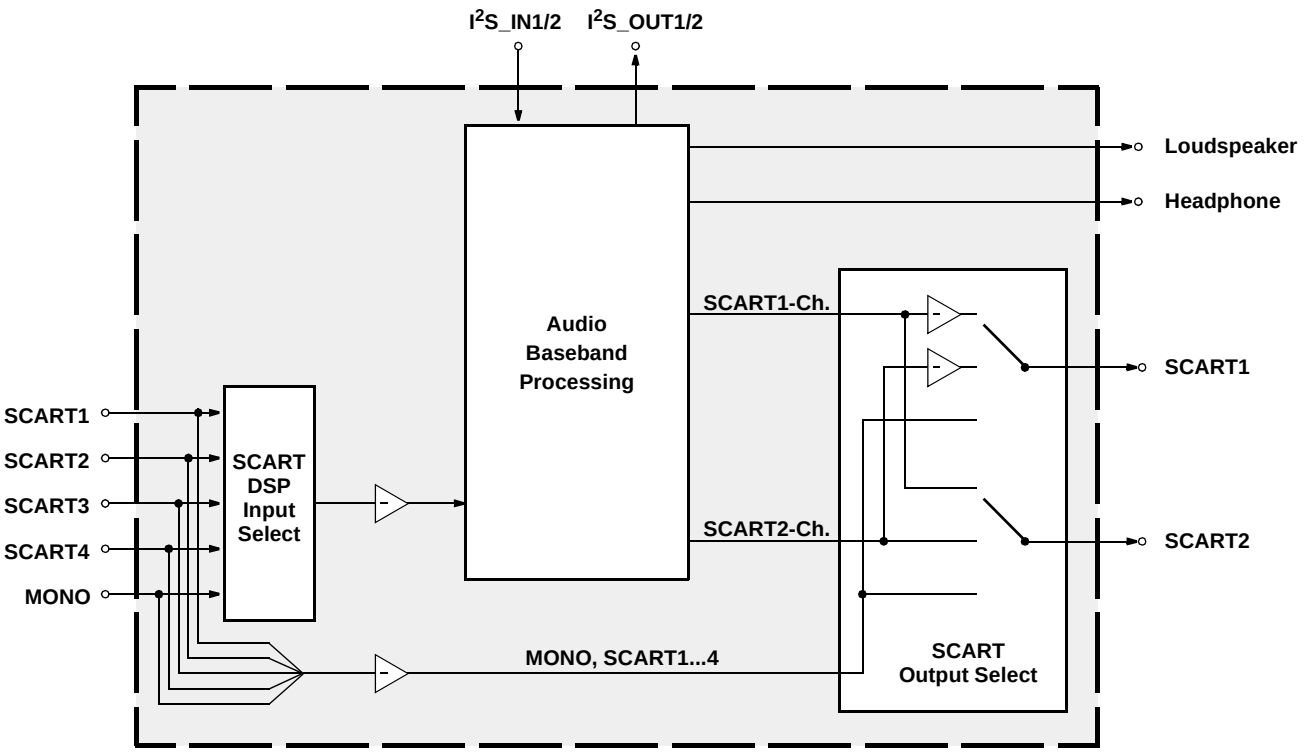



**Fig. 6–2:** Phase diagram of the MSP 34x1G

## 7. Appendix D: MSP 34x1G Version History

### MSP 3451G-A1

First release

### MSP 3451G-A2

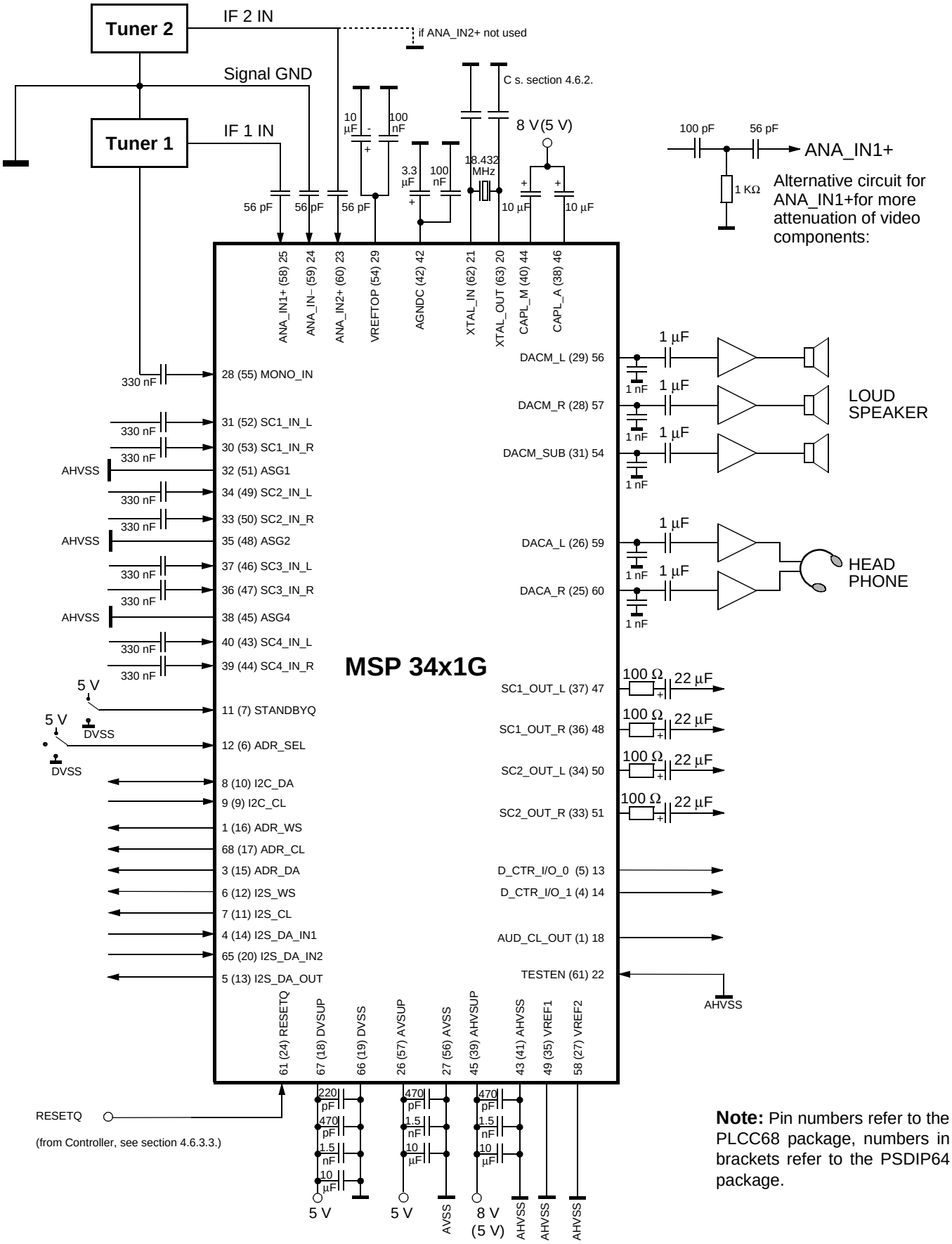
– CONTROL register now readable for more status information

– new D/K standard for Poland

– improved $I^2C$ hardware problem handling

– improved AM-performance

## 8. Appendix E: Application Circuit




**Note:** Pin numbers refer to the PLCC68 package, numbers in brackets refer to the PSDIP64 package.

## 9. Data Sheet History

1. Preliminary data sheet: “MSP 34x1G Multistandard Sound Processor Family with Virtual Dolby Surround”, Edition Oct. 15, 1999, 6251-511-1PD. First release of the preliminary data sheet.

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