Datasheet No. PD60292

International
IOR Rectifier

# IRS2166D(S)PbF

## PFC + BALLAST CONTROL IC

### Features

- PFC, ballast control and 600 V half-bridge driver in one IC
- Critical-conduction mode boost-type PFC
- Programmable half-bridge over-current protection
- Programmable preheat frequency
- Programmable deadtime
- Programmable preheat time
- Programmable run frequency
- RoHS compliant
- End-of-life window comparator pin
- Internal up/down current-sense fault counter
- DC bus undervoltage reset
- Lamp removal/auto-restart shutdown pin
- Internal bootstrap MOSFET
- Internal 15.6 V zener clamp diode on $V_{CC}$
- Micropower startup (250 µA)
- Latch immunity and ESD protection

### Description

The IRS2166D is a fully integrated, fully protected 600 V ballast control IC designed to drive all types of fluorescent lamps. The IRS2166D is based on the popular IR2166 control IC with additional improvements to increase ballast performance. PFC circuitry operates in critical conduction mode and provides high PF, low THD, and DC bus regulation. The IRS2166D features include programmable preheat and run frequencies, programmable preheat time, and programmable end-of-life protection. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, end-of-life protection, DC bus undervoltage reset as well as an automatic restart function, have been included in the design.

### System Features

- Improved $V_{BUS}$ regulation voltage tolerance
- Increased SD pin shutdown voltage threshold hysteresis
- Changed EOL pin internal 2.0 V bias to a +/-10 µA OTA
- Internal bootstrap MOSFET

### Packages

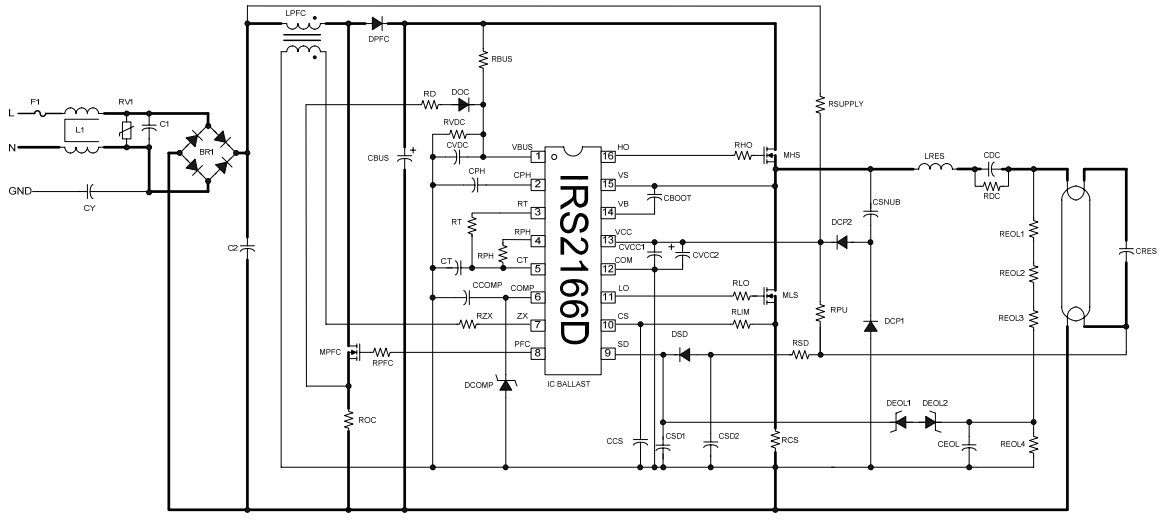


**16-Lead PDIP**
**IRS2166DPbF**



**16-Lead SOIC**
**IRS2166DSPbF**

### Application Diagram (Typical Only)




**Note:** Thick traces represent high-frequency, high-current paths.
Lead lengths should be minimized and power and IC grounds should be separated to avoid high-frequency noise problems.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_B$ | High-side floating supply voltage | | -0.3 | 625 | V |
| $V_S$ | High-side floating supply offset voltage | | $V_B$ – 25 | $V_B$ + 0.3 | |
| $V_{HO}$ | High-side floating output voltage | | $V_S$ - 0.3 | $V_B$ + 0.3 | |
| $V_{LO}$ | Low-side output voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{PFC}$ | PFC gate driver output voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $I_{O,MAX}$ | Maximum allowable output current (HO, LO, PFC) due to external power transistor miller effect | | -500 | 500 | mA |
| $V_{BUS}$ | VBUS pin voltage | | -0.3 | $V_{CC}$ + 0.3 | V |
| $V_{CPH}$ | CPH pin voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{RT}$ | RT pin voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $V_{RPH}$ | RPH pin voltage | | -0.3 | $V_{CC}$ + 0.3 | |
| $I_{RT}$ | RT pin current | | -5 | 5 | mA |
| $I_{RPH}$ | RPH pin current | | -5 | 5 | |
| $V_{CT}$ | CT pin voltage | | -0.3 | $V_{CC}$ + 0.3 | V |
| $I_{COMP}$ | COMP pin current | | -5 | 5 | mA |
| $I_{ZX}$ | ZX pin current | | -5 | 5 | |
| $I_{CC}$ | VCC pin current (see Note 1) | | -25 | 25 | |
| $V_{SD/EOL}$ | SD/EOL pin voltage | | -0.3 | $V_{CC}$ + 0.3 | V |
| $I_{SD/EOL}$ | SD/EOL pin current | | -5 | 5 | mA |
| $V_{CS}$ | CS pin voltage | | -0.3 | $V_{CC}$ + 0.3 | V |
| $I_{CS}$ | CS pin current | | -5 | 5 | mA |
| dV/dt | Allowable $V_S$ offset voltage slew rate | | -50 | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \le +25$ ºC<br>$PD = (T_{JMAX}-T_A)/R_{\theta JA}$ | (16-Pin DIP) | --- | 1.8 | W |
| | | (16-Pin SOIC) | --- | 1.4 | |
| $R_{\Theta JA}$ | Thermal resistance, junction to ambient | (16-Pin DIP) | --- | 70 | ºC/W |
| | | (16-Pin SOIC) | --- | 82 | |
| $T_J$ | Junction temperature | | -55 | 150 | ºC |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | --- | 300 | |

Note 1: This IC contains a zener clamp structure between the chip $V_{CC}$ and COM which has a nominal breakdown voltage of 15.6 V. This supply pin should not be driven by a DC, low impedance power source greater than the $V_{CLAMP}$ specified in the electrical characteristics section.

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$-$V_S$ | High side floating supply voltage | $V_{BSUV+}$ | $V_{CLAMP}$ | V |
| $V_S$ | Steady state high-side floating supply offset voltage | -1 | 600 | |
| $V_{CC}$ | Supply voltage | $V_{CCUV+}$ | $V_{CLAMP}$ | |
| $I_{CC}$ | $V_{CC}$ supply current (see Note 2) | Note 2 | 20 | mA |
| $C_T$ | CT pin capacitance | 220 | --- | pF |
| $I_{SD/EOL}$ | SD/EOL pin current | -1 | 1 | mA |
| $I_{CS}$ | CS pin current | | | |
| $I_{ZX}$ | ZX pin current | | | |
| $T_J$ | Junction temperature | -25 | 125 | ºC |

Note 2: Enough current should be supplied into the $V_{CC}$ pin to keep the internal 15.6 V zener clamp diode on this pin regulating its voltage, $V_{CLAMP}$.

## Electrical Characteristics

$V_{CC}$ = $V_{BS}$ = $V_{BIAS}$=14 V +/- 0.25 V, $V_{CPH}$=$V_{SD/EOL}$=$V_{COMP}$=$V_{CS}$=$V_{BUS}$=$V_{ZX}$=0.0 V, $R_T$ = $R_{PH}$ = 39.2 kΩ, $C_{LO}$ = $C_{HO}$ = $C_{PFC}$ = 1000 pF, $C_T$ = 470 pF, $T_A$ =25 °C unless otherwise specified. See state diagram for MODE.

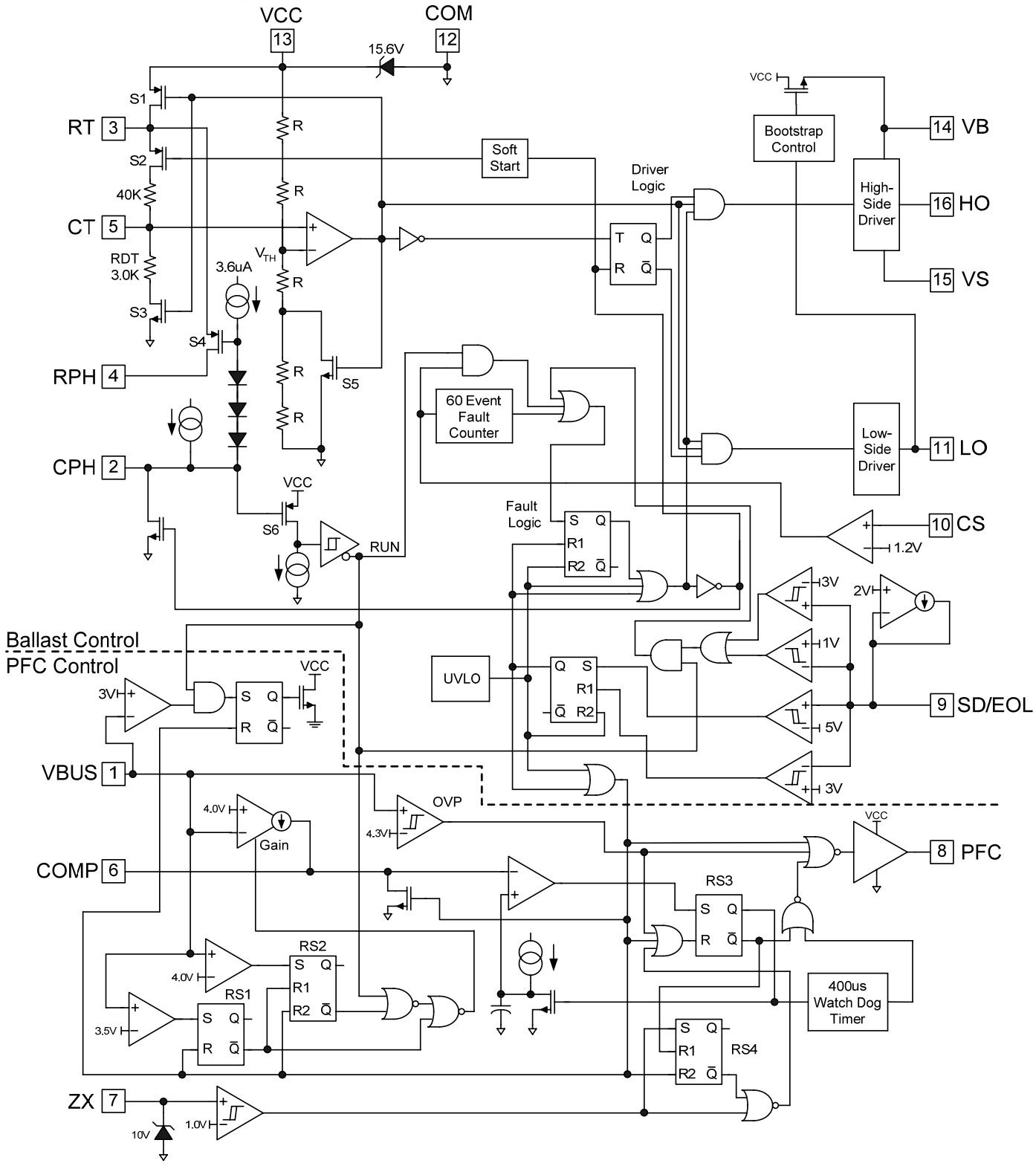
| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **Supply Characteristics** | | | | | | |
| $V_{CCUV+}$ | $V_{CC}$ supply undervoltage positive going threshold | 11.5 | 12.5 | 13.5 | V | $V_{CC}$ rising from 0 V, CT = COM |
| $V_{CCUV-}$ | $V_{CC}$ supply undervoltage negative going threshold | 9.5 | 10.5 | 11.5 | | $V_{CC}$ falling from 14 V, CT = COM |
| $V_{UVHYS}$ | $V_{CC}$ supply undervoltage lockout hysteresis | 1.5 | 2.0 | 3.0 | | CT = COM |
| $I_{QCCUV}$ | UVLO mode $V_{CC}$ quiescent current | --- | 250 | 500 | µA | $V_{CC}$ = 8 V, CT = COM |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | --- | 4.3 | 5.1 | mA | CT = COM |
| $I_{QCCFLT}$ | Fault quiescent $V_{CC}$ supply current | --- | 600 | 900 | µA | MODE = FAULT |
| $I_{CC,RUN}$ | $V_{CC}$ current at RUN frequency | --- | 5.0 | --- | mA | MODE=RUN COMP=2 V, $t_{off,PFC}$=2 µs |
| $V_{CLAMP}$ | $V_{CC}$ zener clamp voltage | 14.6 | 15.6 | 16.6 | V | $I_{CC}$ = 10 mA |
| **Floating Supply Characteristics** | | | | | | |
| $I_{QBS0}$ | Quiescent $V_{BS}$ supply current | --- | 30 | 70 | µA | $V_{HO}$ = $V_S$ |
| $I_{QBS1}$ | Quiescent $V_{BS}$ supply current | --- | 50 | 90 | | $V_{HO}$ = $V_B$ |
| $V_{BSUV+}$ | $V_{BS}$ supply undervoltage positive going threshold | 8.0 | 9.0 | 10.0 | V | $V_{BS}$ rising from 0 V |
| $V_{BSUV-}$ | $V_{BS}$ supply undervoltage negative going threshold | 7.0 | 8.0 | 9.0 | | $V_{BS}$ falling from 14 V |
| $I_{LKVS}$ | $V_S$ offset supply leakage current | --- | --- | 50 | µA | $V_B$ = $V_S$ = HO = 600 V |
| **PFC Error Amplifier Characteristics** | | | | | | |
| $I_{COMP,SOURCE}$ | OTA error amplifier output current sourcing | 20 | 30 | 40 | µA | MODE = RUN $V_{VBUS}$ = 3.5 V |
| $I_{COMP,SINK}$ | OTA error amplifier output current sinking | -45 | -35 | -25 | | MODE = RUN $V_{VBUS}$ = 4.5 V |
| $V_{COMPOH}$ | OTA error amplifier output voltage swing (high state) | 12.0 | 12.5 | 13.0 | V | |
| $V_{COMPOL}$ | OTA error amplifier output voltage swing (low state) | 200 | 300 | 400 | mV | |
| **PFC Control Characteristics** | | | | | | |
| $V_{VBUSREG}$ | $V_{BUS}$ internal reference voltage (guaranteed by design) | 3.9 | 4.0 | 4.1 | V | $V_{COMP}$=4.0 V |
| $V_{VBUSOV+}$ | $V_{BUS}$ over-voltage comparator positive going threshold | 4.1 | 4.3 | 4.5 | | |
| $V_{VBUSOV-}$ | $V_{BUS}$ over-voltage comparator negative going hysteresis | 4.0 | 4.15 | 4.3 | | |
| $V_{ZX}$ | ZX pin positve edge triggered threshold voltage | 1.5 | 2.0 | 2.5 | | CT=COM |
| $V_{ZXHYS}$ | ZX pin comparator hysterisis | 100 | 300 | 500 | mV | |
| $V_{ZXclamp}$ | ZX pin clamp voltage (high state) | 5.7 | 6.7 | 7.7 | V | $I_{ZX}$ = 5 mA, CT=COM |
| $t_{WD}$ | PFC watch-dog pulse interval | 150 | 400 | 500 | µs | $V_{ZX}$ = 0 V, $V_{COMP}$ = 2.0 V CT=COM |

## Electrical Characteristics (cont'd)

$V_{CC}$ = $V_{BS}$ = $V_{BIAS}$=14 V +/- 0.25 V, $V_{CPH}$=$V_{SD/EOL}$ = $V_{COMP}$= $V_{CS}$= $V_{BUS}$ = $V_{ZX}$ =0.0 V, $R_T$ = $R_{PH}$ = 39.2 kΩ, $C_{LO}$ = $C_{HO}$ = $C_{PFC}$ = 1000 pF, $C_T$ = 470 pF, $T_A$=25 °C unless otherwise specified. See state diagram for MODE.

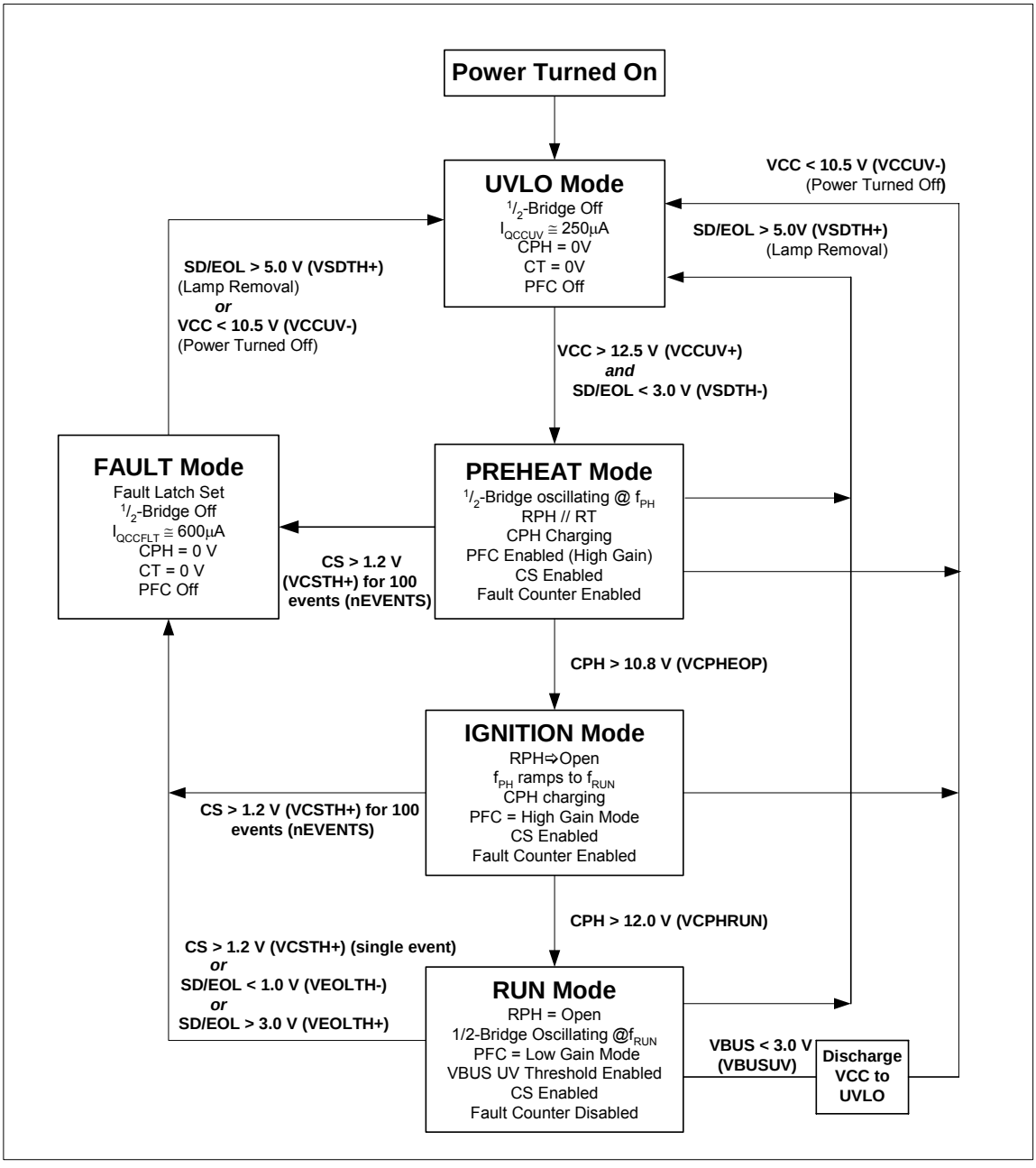
| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **PFC Protection Circuitry Characteristics** | | | | | | |
| $V_{VBUSUV-}$ | $V_{BUS}$ pin undervoltage reset threshold | 2.7 | 3.0 | 3.3 | V | CT=COM |
| **Gate Driver Output Characteristics (HO, LO and PFC pins)** | | | | | | |
| $V_{OL}$ | Low-level output voltage, LO, HO, PFC | --- | COM | --- | V | |
| $V_{OH}$ | High-level output voltage, LO, HO, PFC | --- | $V_{CC}$ | --- | | |
| $t_r$ | Turn-on rise time | --- | 120 | 220 | ns | |
| $t_f$ | Turn-off fall time | --- | 50 | 100 | | |
| $I_{0+}$ | Source current | --- | 180 | --- | mA | |
| $I_{0-}$ | Sink current | --- | 260 | --- | | |
| **Bootstrap FET Characteristics** | | | | | | |
| $V_{B,ON}$ | $V_B$ when the bootstrap FET is on | 13.2 | 13.7 | --- | V | |
| $I_{B,CAP}$ | $V_B$ source current when FET is on | 40 | 55 | --- | mA | $C_{BS}$=0.1 µF |
| $I_{B,10V}$ | $V_B$ source current when FET is on | 9 | 12 | --- | | $V_B$=10 V |
| **Ballast Control Oscillator Characteristics** | | | | | | |
| $f_{PH}$ | Preheat half-bridge oscillator frequency | 73 | 76 | 81 | kHz | MODE=PREHEAT |
| $f_{RUN}$ | Run half-bridge oscillator frequency | 40 | 43 | 46 | | MODE=RUN, CPH=13 V |
| D | Oscillator duty cycle | --- | 50 | --- | % | |
| $t_{d,LO}$ | LO output deadtime | 0.7 | 1.0 | 1.5 | µs | |
| $t_{d,HO}$ | HO output deadtime | 0.7 | 1.0 | 1.5 | | |
| $V_{CT+}$ | CT pin rising threshold voltage | 7.8 | 8.4 | 9.0 | V | |
| $V_{CT-}$ | CT pin falling threshold voltage | 4.1 | 4.6 | 5.1 | | |
| **Ballast Control Preheat Characteristics** | | | | | | |
| $V_{CPHEOP}$ | CPH pin end of preheat threshold voltage | --- | 10.8 | --- | V | CT=COM, $I_{RPH}$<2 µA |
| $V_{CPHRUN}$ | CPH pin run mode threshold voltage | --- | 12.0 | --- | | $V_{BUS}$=$V_{CC}$, CT=COM, $V_{SDEOL}$=3.5 V, |
| $I_{RPHLK}$ | RPH pin leakage current | --- | 0.1 | --- | µA | MODE=RUN |
| $I_{CPH}$ | CPH pin charging current | 2.6 | 3.6 | 4.6 | | CPH=5 V |
| $V_{CPHFLT}$ | CPH pin voltage in fault mode | --- | 0 | --- | V | MODE = FAULT |
| **Ballast Control Protection Circuitry Characteristics** | | | | | | |
| $V_{CSTH+}$ | CS pin over-current sense threshold | 1.075 | 1.20 | 1.325 | V | |
| $n_{EVENTS}$ | CS pin fault counter number of events | 70 | 100 | 140 | | MODE=PREHEAT, $V_{BUS}$=0 V |
| $V_{SDTH+}$ | SD pin rising non-latched shutdown threshold | 4.5 | 5.0 | 5.5 | V | CT=COM |
| $V_{SDTH-}$ | SD pin falling reset threshold voltage | 2.7 | 3.0 | 3.3 | | |
| $V_{SD,delay}$ | Delay from $V_{SDTH+}$ until LO goes low | --- | 450 | --- | ns | |
| $V_{EOLBIAS}$ | EOL pin bias voltage | 1.8 | 2.0 | 2.2 | V | |
| $I_{EOL,SRC}$ | EOL pin internal OTA source current | --- | 10 | --- | µA | SD = $V_{EOLBIAS}$ + 0.5 V |
| $I_{EOL,SNK}$ | EOL pin internal OTA sink current | --- | 10 | --- | | |
| $V_{EOLTH+}$ | EOL pin rising latched shutdown threshold (active during RUN MODE) | 2.7 | 3.0 | 3.3 | V | MODE=RUN, CT=COM $V_{BUS}$=4.0 V, CPH=13 V |
| $V_{EOLTH-}$ | EOL pin falling latched shutdown threshold (active during RUN MODE) | 0.9 | 1.0 | 1.1 | | |
| $V_{EOL,delay}$ | Delay from $V_{EOLTH+}$ until LO goes low | --- | 1 | --- | µs | MODE=RUN, CT=COM, CPH=13 V |
| $V_{CTFLT}$ | CT pin fault mode voltage | --- | 0 | --- | V | MODE=FAULT |
| $V_{CPHFLT}$ | CPH pin fault mode voltage | --- | 0 | --- | | |

## Schematic Block Diagram



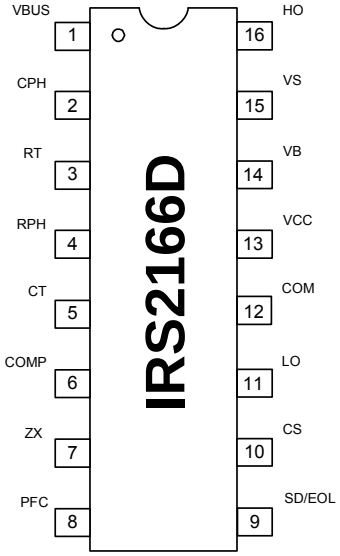

**Please Note: All values shown in block diagram are typical values only**

## State Diagram



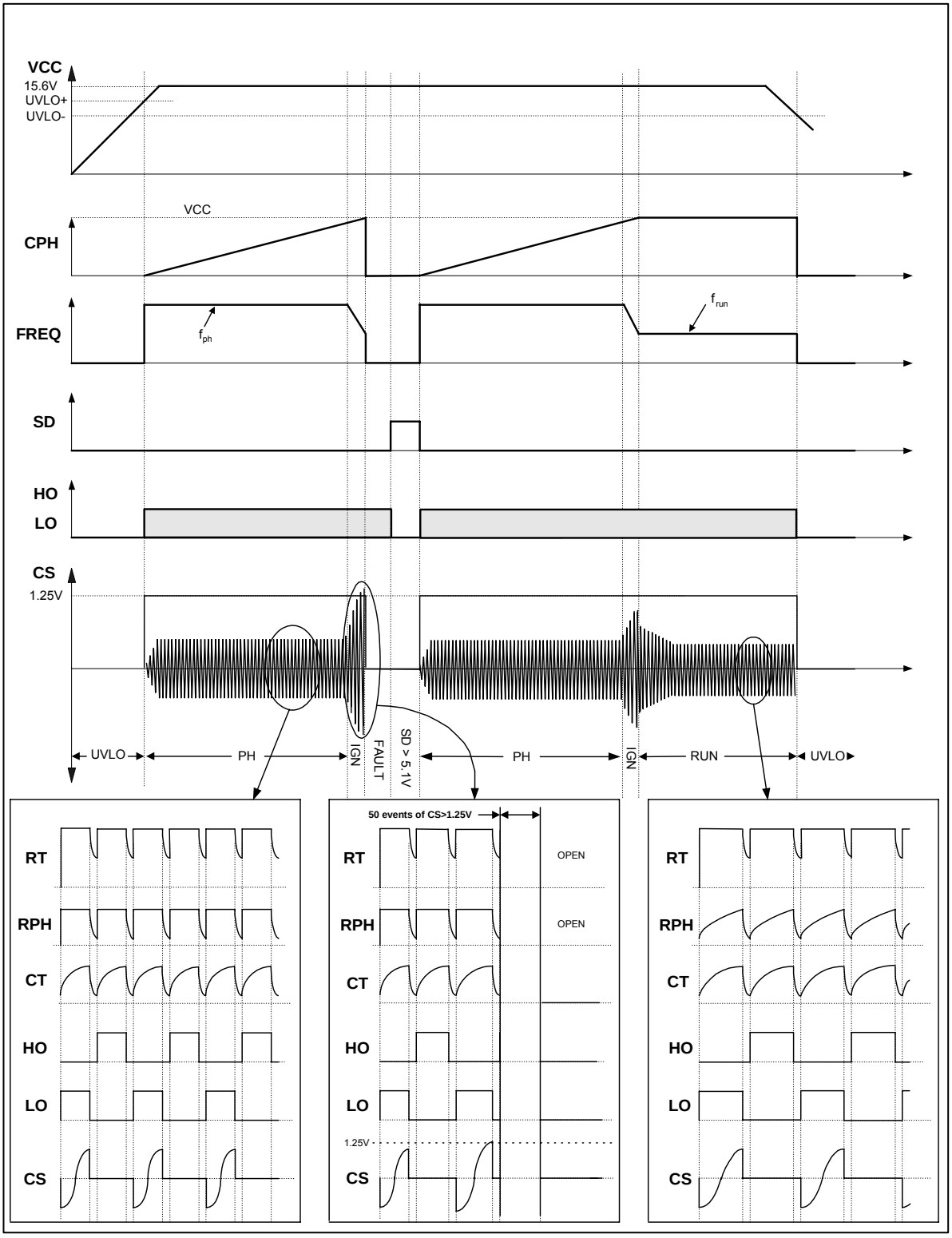

All values are typical. Applies to application diagram on page 1.

## Lead Assignments & Definitions




| Pin # | Symbol | Description |
|---|---|---|
| 1 | VBUS | DC bus sensing input |
| 2 | CPH | Preheat timing capacitor |
| 3 | RT | Oscillator timing resistor |
| 4 | RPH | Preheat frequency timing resistor |
| 5 | CT | Oscillator timing capacitor |
| 6 | COMP | PFC error amplifier compensation |
| 7 | ZX | PFC zero-crossing detection |
| 8 | PFC | PFC gate driver output |
| 9 | SD/EOL | Shutdown/end of life densing circuit |
| 10 | CS | Half-bridge current sensing input |
| 11 | LO | Low-side gate driver output |
| 12 | COM | IC power & signal ground |
| 13 | VCC | Logic & low-side gate driver supply |
| 14 | VB | High-side gate driver floating supply |
| 15 | VS | High voltage floating return |
| 16 | HO | High-side gate driver output |

## Timing Diagrams Ballast Section



## I. Ballast Section Functional Description

### Undervoltage Lock-Out Mode (UVLO)

The undervoltage lock-out mode (UVLO) is defined as the state the IC is in when $V_{CC}$ is below the turn-on threshold of the IC. To identify the different modes of the IC, refer to the State Diagram shown on page 7 of this document. The IRS2166D undervoltage lock-out is designed to maintain an ultra low supply current of 250 µA ($I_{QCCUV}$), and to guarantee the IC is fully functional before the high and low side output drivers are activated. Fig. 1 shows an efficient supply voltage using the start-up current of the IRS2166D together with a charge pump from the ballast output stage ($R_{SUPPLY}$, $C_{VCC}$, $D_{CP1}$, and $D_{CP2}$).

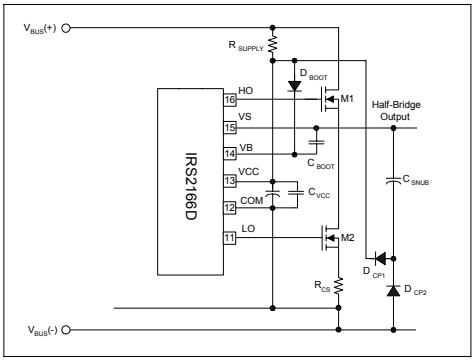



**Fig. 1:** Start-up and supply circuitry

The start-up capacitor ($C_{VCC}$) is charged by current through supply resistor ($R_{SUPPLY}$) minus the start-up current drawn by the IC. This resistor is chosen to set the line input voltage turn-on threshold for the ballast. Once the capacitor voltage on $V_{CC}$ reaches the start-up threshold $V_{CCUV}$+, and the SD pin is below 3.0 V ($V_{SDTH}$-), the IC turns on and HO and LO begin to oscillate. The capacitor begins to discharge due to the increase in IC operating current (Fig. 2).

During the discharge cycle, the rectified current from the charge pump charges the capacitor above the IC turn-off threshold. The charge pump and the internal 15.6 V ($V_{CLAMP}$) zener clamp of the IC take over as the supply voltage. The start-up capacitor and snubber capacitor must be selected such that enough supply current is available over all ballast operating conditions. A supply capacitor ($C_{BOOT}$) comprises the supply voltage for the high side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. During undervoltage lock-out mode, the high- and low-side driver outputs HO and LO are both low, pin CT is connected internally to COM to disable the oscillator, and pin CPH is connected internally to COM for resetting the preheat time.

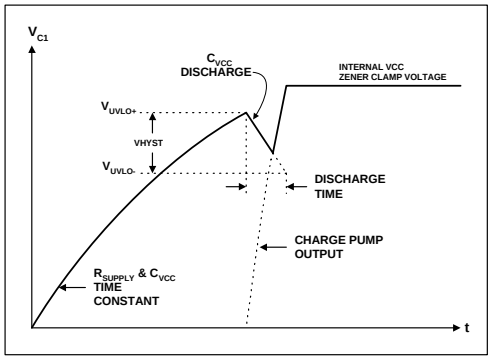



**Fig. 2:** Supply capacitor ($C_{VCC}$) voltage

### Preheat Mode (PH)

The preheat mode is defined as the state the IC is in when the lamp filaments are being heated to their correct emission temperature. This is necessary for maximizing lamp life and reducing the required ignition voltage. The IRS2166D enters preheat mode when $V_{CC}$ exceeds the UVLO positive-going threshold $V_{CCUV+}$. HO and LO begin to oscillate at the preheat frequency with 50% duty cycle and with a deadtime which is set by the value of the external timing capacitor, $C_T$, and internal deadtime resistor, $R_{DT}$. Pin CPH is disconnected from COM and an internal 3.6 µA ($I_{CPH}$) current source (Fig. 3) charges the external preheat timing capacitor on CPH linearly. The over-current protection on pin CS is enabled during preheat. The preheat frequency is determined by the parallel combination of resistors $R_T$ and $R_{PH}$, together with timing capacitor $C_T$. $C_T$ charges and discharges between 1/3 ($V_{CT-}$) and 3/5 ($V_{CT+}$) of $V_{CC}$ (see Timing Diagram, page 9). $C_T$ is charged exponentially through the parallel combination of $R_T$ and $R_{PH}$ connected internally to $V_{CC}$ through MOSFET S1. The charge time of CT from 1/3 to 3/5 $V_{CC}$ is the on-time of the respective output gate driver, HO or LO. Once $C_T$ exceeds 3/5 $V_{CC}$, MOSFET S1 is turned off, disconnecting $R_T$ and $R_{PH}$ from $V_{CC}$. $C_T$ is then discharged exponentially through an internal resistor, $R_{DT}$, through MOSFET S3 to COM. The discharge time of $C_T$ from 3/5 to 1/3 $V_{CC}$ is the deadtime (both off) of the output gate drivers, HO and LO. The selected value of $C_T$ and $R_{DT}$ program the desired deadtime (see Design Equations, page 15, Equations 1 and 2). Once $C_T$ discharges below 1/3 $V_{CC}$, MOSFET S3 is turned off, disconnecting $R_{DT}$ from COM, and MOSFET S1 is turned on, connecting $R_T$ and $R_{PH}$ again to $V_{CC}$. The frequency remains at the preheat frequency until the voltage on pin $C_{PH}$ exceeds 10 V and the IC enters ignition mode. During the preheat mode, both the over-current protection and the DC bus undervoltage reset are enabled when pin $C_{PH}$ exceeds 12 V ($V_{CPHRUN}$).

### Ignition Mode (IGN)

The ignition mode is defined as the state the IC is in when a high voltage is being established across the lamp necessary for igniting the lamp. The IRS2166D enters ignition mode when the voltage on pin CPH exceeds 10.8 V ($V_{CPHEOP}$). Pin CPH is connected internally to the

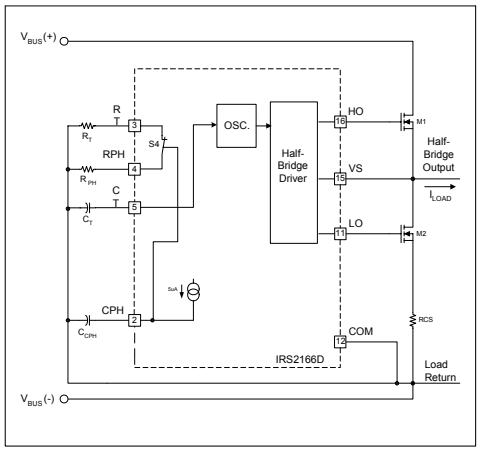



**Fig. 3:** Preheat circuitry

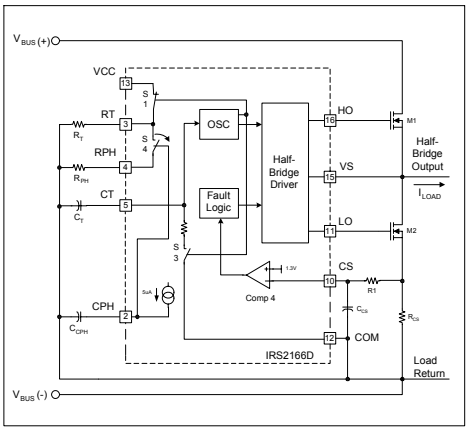



**Fig.4:** Ignition circuitry

gate of a p-channel MOSFET (S4) (see Fig. 4) that connects pin RPH with pin RT. As pin CPH exceeds 10.8 V ($V_{CPHEOP}$), the gate-to-source voltage of MOSFET S4 begins to fall below the turn-on threshold of S4. As pin CPH continues to ramp towards $V_{cc}$, switch S4 turns off slowly. This results in resistor $R_{PH}$ being disconnected smoothly from resistor $R_T$, which causes the operating frequency to ramp smoothly from the preheat frequency, through the ignition frequency, to the final run frequency. The over-current threshold on pin CS will protect the ballast against a non-strike or open-filament lamp fault condition. The voltage on pin CS is defined by the lower half-bridge MOSFET current flowing through the external current sensing resistor $R_{CS}$. The resistor $R_{CS}$ therefore programs the maximum allowable peak ignition current (and therefore peak ignition voltage) of the ballast output stage. The peak ignition current must not exceed the maximum allowable current ratings of the output stage MOSFETs. Should this voltage exceed the internal threshold of 1.20 V ($V_{CSTH+}$), the internal fault counter begins counting the number of of sequential over-current faults (see timing diagram). If the number of over-current faults exceeds 50 ($n_{EVENTS}$), the IC will enter FAULT mode and gate driver outputs HO, LO and PFC will be latched low.

## Run Mode (RUN)

Once the lamp has successfully ignited, the ballast enters run mode. The run mode is defined as the state the IC is in when the lamp arc is established and the lamp is being driven to a given power level. The run mode oscillating frequency is determined by the timing resistor $R_T$ and timing capacitor $C_T$ (see Design Equations, page 15). Should hard-switching occur at the half-bridge at any time due to an open-filament or lamp removal, the voltage across the current sensing resistor, $R_{CS}$, will exceed the internal threshold of 1.20 V ($V_{CSTH+}$) and the fault counter will begin counting (see timing diagram). Should the number of consecutive over-current faults exceed 50 ($n_{EVENTS}$), the IC will enter fault mode and gate driver outputs HO, LO and PFC will be latched low.

## DC Bus Undervoltage Reset

Should the DC bus decrease too low during a brown-out line condition or over-load condition, the resonant output stage to the lamp can shift near or below resonance. This can produce hard-switching at the half-bridge which can damage the half-bridge switches or, the DC bus can decrease too far and the lamp can extinguish. To protect against this, the VBUS pin includes a 3.0 V undervoltage threshold ($V_{BUSUV}$). Should the voltage at the VBUS pin decrease below 3.0 V, $V_{CC}$ will be discharged below the $V_{CCUV}$- threshold and all gate driver outputs will be latched low.

For proper ballast design, the designer should design the PFC section such that the DC bus does not drop until the AC line input voltage falls below the rated input voltage of the ballast (see PFC section). When correctly designed, the voltage measured at the VBUS pin will decrease below the internal 3.0 V threshold (VBUSUV) and the ballast will turn off cleanly. The pull-up resistor to $V_{CC}$ ($R_{SUPPLY}$) will then turn the ballast on again when the AC input line voltage increases to the minimum specified value causing $V_{CC}$ to exceed $V_{CCUV}$+.

$R_{SUPPLY}$ should be set to turn the ballast on at the minimum specified ballast input voltage. The PFC should then be designed such that the DC bus decreases at an input line voltage that is lower than the minimum specified ballast input voltage. This hysteresis will result in clean turn-on and turn-off of the ballast.

## SD/EOL and CS Fault Mode (FAULT)

Should the voltage at the SD/EOL pin exceed 3.0 V ($V_{EOLTH+}$) or decrease below 1.0 V ($V_{EOLTH-}$) during run mode, an end-of-life (EOL) fault condition has occurred and the IC enters fault mode. LO, HO, and PFC gate driver outputs are all latched off in the 'low' state. $C_{PH}$ is discharged to COM for resetting the preheat time. To exit fault mode, $V_{CC}$ can be decreased below $V_{CCUV}$- (ballast power off) or the SD pin can be increased above 5.0 V ($V_{SDTH+}$) (lamp removal). Either of these will force the IC to enter UVLO mode (see State Diagram, page 7). Once

$V_{CC}$ is above $V_{CCUV}$+ (ballast power on) and SD is pulled above 5.0 V ($V_{SDTH+}$) and back below 3.0 V ($V_{SDTH-}$) (lamp re-insertion), the IC will enter preheat mode and begin oscillating again.

The current sense function will force the IC to enter fault mode only after the voltage at the CS pin has been greater than 1.20 V ($V_{CSTH+}$) for 100 ($n_{EVENTS}$) consecutive cycles of LO. The over-current function at the CS pin (see Fig. 5) will only consecutive cycles of LO. The over-current function at the CS pin (see Fig. 5) will only work with over-current events that occur during the LO on-time. If the over-current faults are not consecutive, then the internal fault counter will count back down each cycle when there is no fault present. Should an over-current fault occur only for a few cycles and then not occur again, the counter will eventually count back down to zero. The over-current fault counter is enabled during preheat and ignition modes and disabled during run mode. During run mode, the IC will enter fault mode after a single over-current event at the CS pin.

## II. PFC Section Functional Description

In most electronic ballasts it is necessary to have the circuit act as a pure resistive load to the AC input line voltage. The degree to which the circuit matches a pure resistor is measured by the phase shift between the input voltage and input current and how well the shape of the input current waveform matches the shape of the sinusoidal input voltage. The cosine of the phase angle between the input voltage and input current is defined as the power factor (PF), and how well the shape of the input current waveform matches the shape of the input voltage is determined by the total harmonic distortion (THD). A power factor of 1.0 (maximum) corresponds to zero phase shift and a THD of 0% represents a pure sinewave (no distortion). For this reason it is desirable to have a high PF and a low THD. To achieve this, the IRS2166D includes an active power factor correction (PFC) circuit which, for an AC line input voltage, produces an AC line input current.

The control method implemented in the IRS2166D is for a boost-type converter (Fig. 6) running in critical-conduction mode (CCM). This means that during each switching cycle of the PFC MOSFET, the circuit waits until the inductor current discharges to zero before turning the PFC MOSFET on again. The PFC MOSFET is turned on and off at a much higher frequency (>10 kHz) than the line input frequency (50 Hz to 60 Hz).

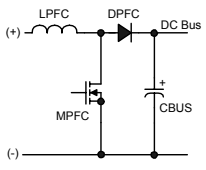



**Fig. 6:** Boost-type PFC circuit

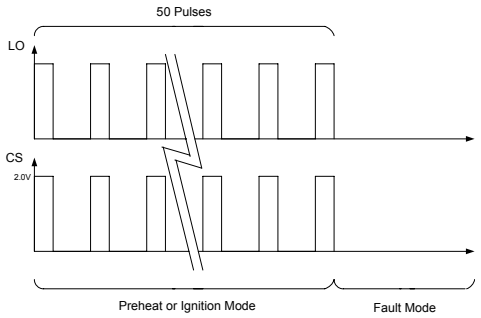



**Fig. 5:** CS & LO Waveforms

When the switch $M_{PFC}$ is turned on, the inductor $L_{PFC}$ is connected between the rectified line input (+) and (-) causing the current in $L_{PFC}$ to charge up linearly. When $M_{PFC}$ is turned off, $L_{PFC}$ is connected between the rectified line input (+) and the DC bus capacitor $C_{BUS}$ (through diode $D_{PFC}$) and the stored current in $L_{PFC}$ flows into $C_{BUS}$. As $M_{PFC}$ is turned on and off at a high-frequency, the voltage on $C_{BUS}$ charges up to a specified voltage. The feedback loop of the IRS2166D regulates this voltage to a fixed value by continuously monitoring the DC voltage and adjusting the on-time of $M_{PFC}$ accordingly. For an increasing DC bus the on-time is decreased, and for a decreasing DC bus the on-time is increased. This negative feedback control is performed with a slow loop speed and a low loop gain such that the average inductor current smoothly follows the low-frequency line input voltage for high power factor and low THD. The on-time of $M_{PFC}$ therefore appears to be fixed (with an additional modulation to be discussed later) over several cycles of the line voltage. With a fixed on-time, and an off-time determined by the inductor current discharging to zero, the result is a system where the switching frequency is free-running and constantly changing from a high frequency near the zero crossing of the AC input line voltage, to a lower frequency at the peaks (Fig. 7).

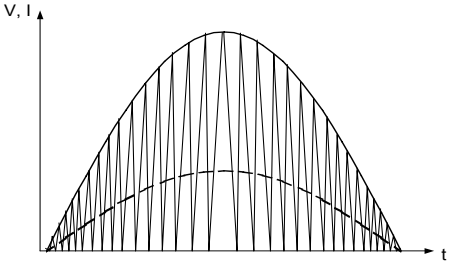



**Fig. 7:** Sinusoidal line input voltage (solid line), triangular PFC inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the line input voltage

When the line input voltage is low (near the zero crossing), the inductor current will charge up to a small amount and the discharge time will be fast resulting in a high switching frequency. When the input line voltage is high (near the peak), the inductor current will charge up to a higher amount and the discharge time will be longer giving a lower switching frequency. The triangular PFC inductor current is then smoothed by the EMI filter to produce a sinusoidal line input current.

The PFC control circuit of the IRS2166D (Fig. 8) only requires four control pins: VBUS, COMP, ZX and PFC. The VBUS pin is for sensing the DC bus voltage (via an external resistor voltage divider), the COMP pin programs the on-time of $M_{PFC}$ and the speed of the feedback loop, the ZX pin detects when the inductor current discharges to zero (via a secondary winding from the PFC inductor), and the PFC pin is the low-side gate driver output for $M_{PFC}$.

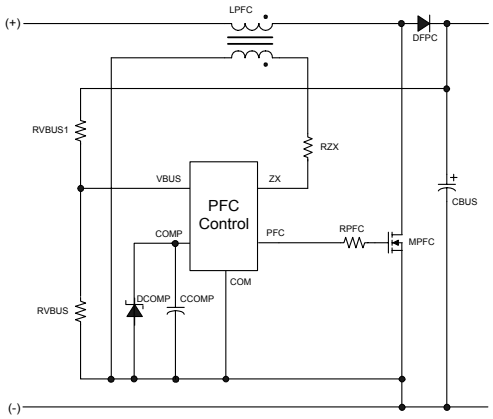



**Fig. 8:** IRS2166D simplified PFC control circuit

The VBUS pin is regulated against a fixed internal 4.0 V reference voltage ($V_{BUSREG}$) for regulating the DC bus voltage (Fig. 9). The feedback loop is performed by an operational transconductance amplifier (OTA) that sinks or sources a current to the external capacitor at the COMP pin. The resulting voltage on the COMP pin sets the threshold for the charging of the internal timing capacitor (C1) and therefore programs the on-time of $M_{PFC}$. During preheat and ignition modes of the ballast section, the gain of the OTA is set to a high level to raise the DC bus level quickly and to minimize the transient on the DC bus which can occur during ignition. During run mode, the gain is then decreased to a lower level necessary for achieving high power factor and low THD.

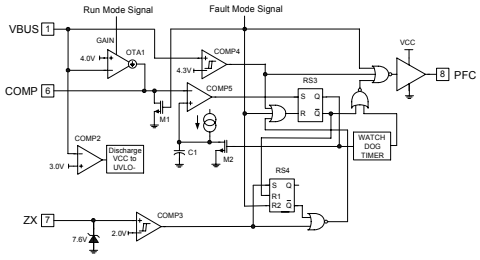



**Fig. 9:** IRS2166D detailed PFC control circuit

The off-time of $M_{PFC}$ is determined by the time it takes the $L_{PFC}$ current to discharge to zero. This zero current level is detected by a secondary winding on $L_{PFC}$ which is connected to the ZX pin. A positive-going edge exceeding the internal 2 V threshold ($V_{ZXTH+}$) signals the beginning of the off-time. A negative-going edge on the ZX pin falling below ($V_{ZXTH+}$ - $V_{ZXHYS}$) will occur when the $L_{PFC}$ current discharges to zero which signals the end of the off-time and $M_{PFC}$ is turned on again (Fig. 10). The cycle repeats itself indefinitely until the PFC section is disabled due to a fault detected by the ballast section (fault mode), an over-voltage or undervoltage condition on the DC bus, or, the negative transition of ZX pin voltage does not occur. Should the negative edge on the ZX pin not occur, $M_{PFC}$ will remain off until the watch-dog timer forces a turn-on of $M_{PFC}$ for an on-time duration programmed by the voltage on the COMP pin. The watch-dog pulses occur every 400 µs ($t_{WD}$) indefinitely until a correct positive- and negative-going signal is detected on the ZX pin and normal PFC operation is resumed.

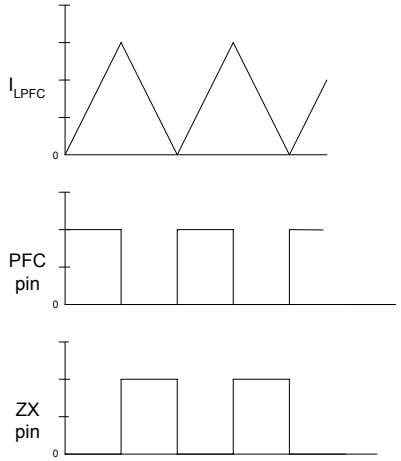



**Fig. 10:** LPFC current, PFC pin and ZX pin timing diagram

A fixed on-time of $M_{PFC}$ over an entire cycle of the line input voltage produces a peak inductor current which naturally follows the sinusoidal shape of the line input voltage. The smoothed averaged line input current is in phase with the line input voltage for high power factor but the total harmonic distortion (THD), as well as the individual higher harmonics, of the current can still be too high. This is mostly due to cross-over distortion of the line current near the zero-crossings of the line input voltage. To achieve low harmonics which are acceptable to international standard organizations and general market requirements, an additional on-time modulation circuit has been added to the PFC control. This circuit dynamically increases the on-time of $M_{PFC}$ as the line input voltage nears the zero-crossings (Fig. 11). This causes the peak $L_{PFC}$ current, and therefore the smoothed line input current, to increase slightly higher near the zero-crossings of the line input voltage. This reduces the amount of cross-over distortion in the line input current which reduces the THD and higher harmonics to low levels.

## Over-Voltage Protection (OVP)

Should over-voltage occur on the DC bus causing the VBUS pin to exceed the internal 4.3 V threshold ($V_{BUSOV+}$), the PFC output is disabled (set to a logic 'low'). When the DC bus decreases again causing the VBUS pin to

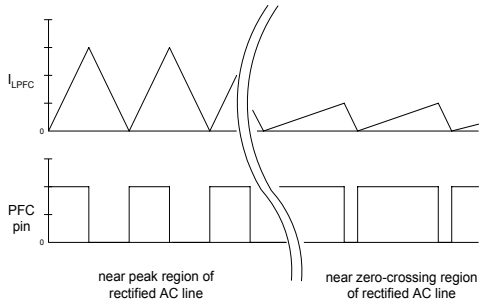



**Fig. 12:** On-time modulation near the zero-crossings

decrease below the internal 4.0 V threshold ($V_{BUSREG}$), a watch-dog pulse is forced on the PFC pin and normal PFC operation is resumed.

## Undervoltage Reset (UVR)

When the line input voltage is decreased, interrupted or a brown-out condition occurs, the PFC feedback loop causes the on-time of $M_{PFC}$ to increase in order to keep the DC bus constant. Should the on-time increase too far, the resulting peak currents in $L_{PFC}$ can exceed the saturation current limit of $L_{PFC}$. $L_{PFC}$ will then saturate and very high peak currents and di/dt levels will occur. To prevent this, the maximum on-time is limited by limiting the maximum voltage on the COMP pin with an external zener diode $D_{COMP}$ (Fig. 8). As the line input voltage decreases, the COMP pin voltage and therefore the on-time will eventually limit. The PFC can no longer supply enough current to keep the DC bus fixed for the given load power and the DC bus will begin to drop. Decreasing the line input voltage further will cause the VBUS pin to eventually decrease below the internal 3 V threshold ($V_{BUSUV}$) (Fig. 9). When this occurs, $V_{cc}$ is discharged internally below $V_{CCUV-}$, the IRS2166D enters UVLO mode and both the PFC and ballast sections are disabled (see State Diagram). The start-up supply resistor to $V_{cc}$, together with the micro-power start-up current of the IRS2166D, determines the line input turn-on voltage. This should be set such that the ballast turns on at a line voltage level above the undervoltage turn-off level, $V_{CCUV+}$. It is the correct selection of the value of the supply resistor to $V_{cc}$ and the zener diode on the COMP pin that correctly program the on and off line input voltage thresholds for the ballast. With these thresholds correctly set, the ballast will turn off due to the 3.0 V undervoltage threshold ($V_{BUSUV}$) on the VBUS pin, and on again at a higher liine input voltage (hysterisis) due to the supply resistor to $V_{cc}$. This hysterisis will result in a proper reset of the ballast without flickering of the lamp, bouncing of the DC bus or re-ignition of the lamp when the DC bus is too low.

## Over-Current Protection (OCP)

In case of fast on/off interruptions of the mains input voltage, or, during normal lamp ignition, the DC bus voltage level can decrease below the instantaneous rectified line voltage. Should this occur, the PFC inductor current and PFC MOSFET current can increase to high levels causing the PFC inductor to saturate and/or the PFC MOSFET to become damaged. During fast on/off interruptions of the mains input voltage, the DC bus can drop during the time when the mains input voltage is interrupted (off). Since VCC is still above UVLO-, the IC will continue to operate and will increase the COMP pin voltage to increase the PFC MOSFET on-time due to the dropping of the DC bus. When the mains voltage returns again quickly (before VCC reaches UVLO-), the on-time of the PFC MOSFET is too long for the given mains input voltage level resulting in high PFC inductor and MOSFET currents that can saturate the inductor and/or damage the PFC MOSFET (Fig. 13).

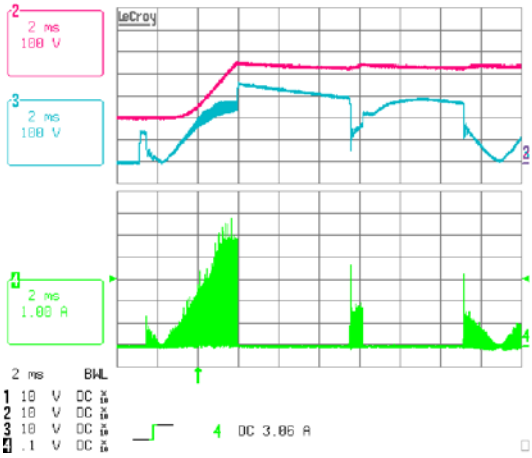



**Fig. 13:** High PFC inductor current during fast mains on/off (upper trace: DC Bus, 100V/div; middle trace: AC line input voltage, 100V/div; lower trace: PFC inductor current 1A/div).

During lamp ignition, the DC bus can drop below the rectified AC line voltage causing current to conduct directly from the output of the rectifier, through the PFC inductor and diode, to the DC bus capacitor. This results in a low-frequency offset of current in the PFC inductor. Since the zero-crossing detection circuit only detects the high-frequency zero-crossing of the inductor current, the PFC MOSFET will turn on again each cycle before the inductor current has reached zero. This causes the PFC to work in a continuous conduction mode and the sum of the low-frequency and high-frequency components of current can saturate the PFC inductor and/or damage the PFC MOSFET. To protect against these conditions, a current sense resistor (ROC) must be inserted between the source of the PFC MOSFET and ground, and a series diode (DOC) and limiting resistor (RD) connected from the top of the current sensing resistor to the VBUS pin (Fig. 14).

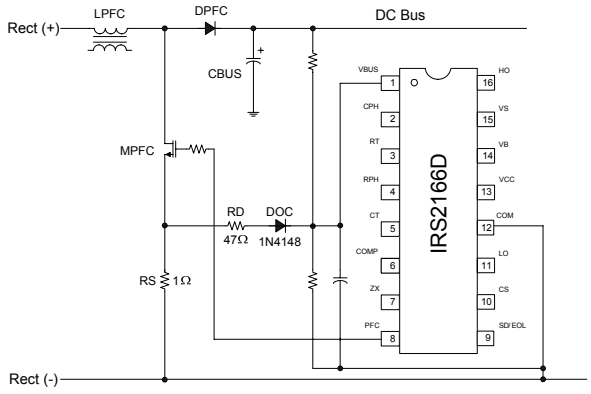



**Fig. 14:** External over-current protection circuit

Should high currents occur, the voltage across the current-sensing resistor will exceed 4.3V over-voltage protection threshold at the VBUS pin and the PFC MOSFET will turn off safely limiting the current. The watch-dog timer will then restart the PFC as normal (Fig. 15). The current sensing resistor value should be selected such that the over-current protection does not false trip during normal operation over the entire line voltage and load range. A current-sensing resistor value of 1.0 ohm, for example, will set the over-current threshold to about 5 A peak.

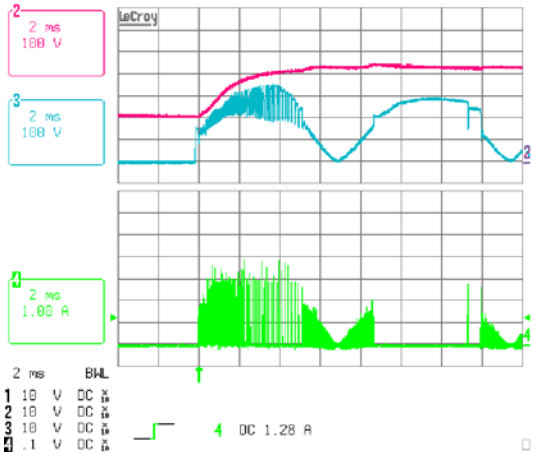



**Fig. 15:** PFC inductor current limited using over-current protection circuit (upper trace: DC Bus, 100V/div; middle trace: AC line input voltage, 100V/div; lower trace: PFC inductor current 1A/div).

The effect that these line and load conditions have on the performance of the ballast depends on the saturation level of the PFC inductor, the selection of the PFC MOSFET, the DC bus capacitor value, the maximum on-time limit set by the DZCOMP, and, how fast VCC decreases below UVLO-.

For these reasons, the ballast designer should perform these mains interrupt and ignition tests carefully to determine the correct current-sensing resistor value and determine the robustness of their final design.

## Ballast Design Equations

Note: The results from the following design equations can differ slightly from experimental measurements due to IC tolerances, component tolerances, and oscillator over- and under-shoot due to internal comparator response time.

Step 1: Program Deadtime

The deadtime between the gate driver outputs HO and LO is programmed with timing capacitor $C_T$ and an internal deadtime resistor $R_{DT}$. The deadtime is the discharge time of capacitor $C_T$ from 3/5 $V_{cc}$ to 1/3 $V_{cc}$ and is given as:

$$t_{DT} = C_T \cdot 1475 \qquad [s] \quad (1)$$

or

$$C_T = \frac{t_{DT}}{1475} \qquad [F] \quad (2)$$

Step 2: Program Run Frequency

The final run frequency is programmed with timing resistor $R_T$ and timing capacitor $C_T$. The charge time of capacitor $C_T$ from 1/3 $V_{cc}$ to 3/5 $V_{cc}$ determines the on-time of HO and LO gate driver outputs. The run frequency is therefore given as:

$$f_{RUN} = \frac{1}{2 \cdot C_T (0.51 \cdot R_T + 1475)} \qquad [Hz] \quad (3)$$

or

$$R_T = \frac{1}{1.02 \cdot C_T \cdot f_{RUN}} - 2892 \qquad [\Omega] \quad (4)$$

Step 3: Program Preheat Frequency

The preheat frequency is programmed with timing resistors $R_T$ and $R_{PH}$, and timing capacitor $C_T$. The timing resistors are connected in parallel internally for the duration of the preheat time. The preheat frequency is therefore given as:

$$f_{PH} = \frac{1}{2 \cdot C_T \cdot \left( \frac{0.51 \cdot R_T \cdot R_{PH}}{R_T + R_{PH}} + 1475 \right)} \quad [\text{Hz}] \quad (5)$$

or

$$R_{PH} = \frac{\left( \frac{1}{1.02 \cdot C_T \cdot f_{PH}} - 2892 \right) \cdot R_T}{R_T - \left( \frac{1}{1.02 \cdot C_T \cdot f_{PH}} - 2892 \right)} \quad [\Omega] \quad (6)$$

Step 4: Program Preheat Time

The preheat time is defined by the time it takes for the capacitor on pin CPH to charge up to 12 V. An internal current source of 3.6 µA ($I_{CPH}$) flows out of pin CPH. The preheat time is therefore given as:

$$t_{PH} = C_{PH} \cdot 2.6e6 \quad [\text{s}] \quad (7)$$

or

$$C_{PH} = t_{PH} \cdot 0.385e-6 \quad [\text{F}] \quad (8)$$

Step 5: Program Maximum Ignition Current

The maximum ignition current is programmed with the external resistor $R_{CS}$ and an internal threshold of 1.20 V. This threshold determines the over-current limit of the ballast, which can be exceeded when the frequency ramps down towards resonance during ignition and the lamp does not ignite. The maximum ignition current is given as:

$$I_{IGN} = \frac{VCSTH+}{R_{CS}} \quad [\text{A}] \quad (9)$$

or

$$R_{CS} = \frac{VCSTH+}{I_{IGN}} \quad [\Omega] \quad (10)$$

## PFC Design Equations

Step1: Calculate PFC inductor value:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^2 \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS} \quad [\text{H}] \quad (1)$$

where,

$VBUS$ = DC bus voltage
$VAC_{MIN}$ = Minimum rms AC input voltage
$\eta$ = PFC efficiency (typically 0.95)
$f_{MIN}$ = Minimum PFC switching frequency at minimum AC input voltage
$P_{OUT}$ = Ballast output power

Step 2: Calculate peak PFC inductor current:

$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta} \quad [\text{A}] \quad (2)$$

Note: The PFC inductor must not saturate at $i_{PK}$ over the specified ballast operating temperature range. Proper core sizing and air-gapping should be considered in the inductor design.

Step 3: Calculate maximum on-time:

$$t_{ON_{MAX}} = \frac{2 \cdot P_{OUT} \cdot L_{PFC}}{VAC_{MIN}^2 \cdot \eta} \quad [\text{s}] \quad (3)$$

Step 4: Calculate maximum COMP voltage:

$$V_{COMP_{MAX}} = \frac{t_{ON_{MAX}}}{0.9E-6} \quad [\text{V}] \quad (4)$$

Step 5: Select zener diode $D_{COMP}$ value:

$$D_{COMP} \text{ zener voltage} \approx V_{COMP_{MAX}} \quad [\text{V}] \quad (5)$$

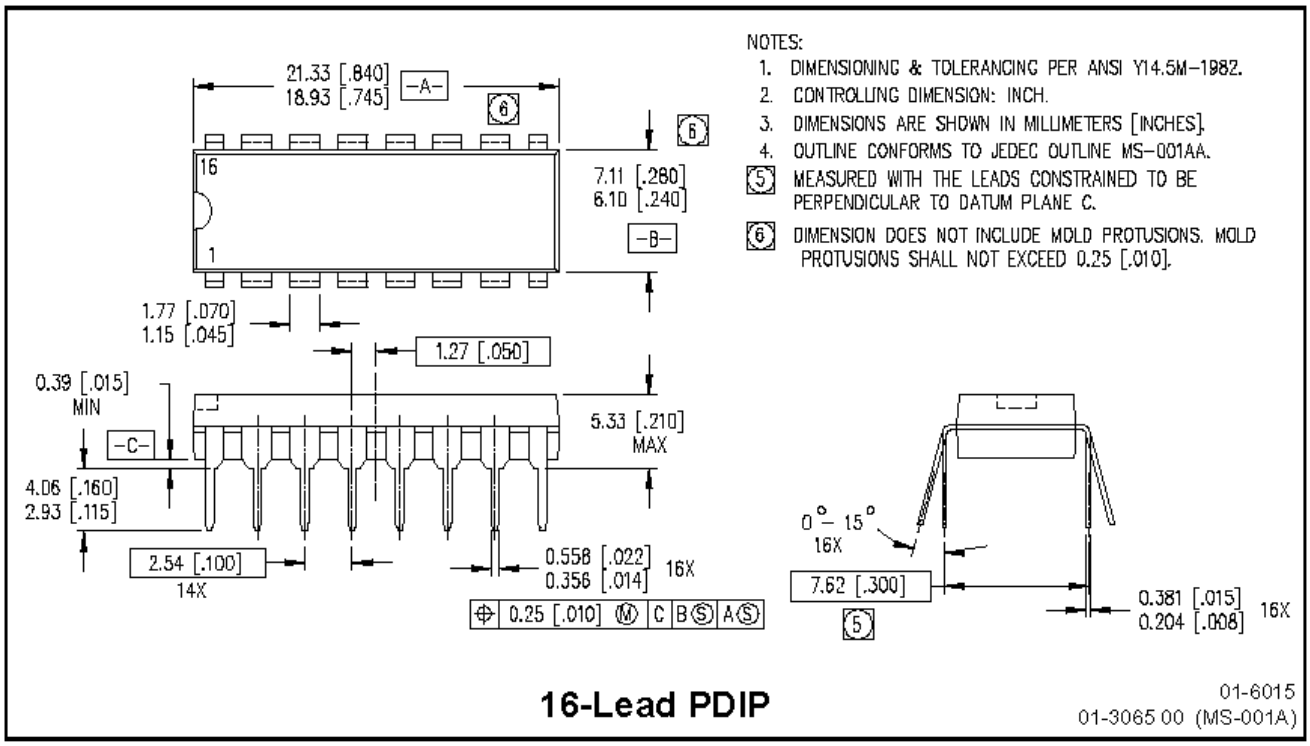
Step 6: Calculate resistor $R_{SUPPY}$ value:

$$R_{SUPPLY} = \frac{VAC_{MIN_PK} + 10}{IQCCUV} \quad [\Omega] \quad (6)$$

Step 7: Calculate resistor ROC value:

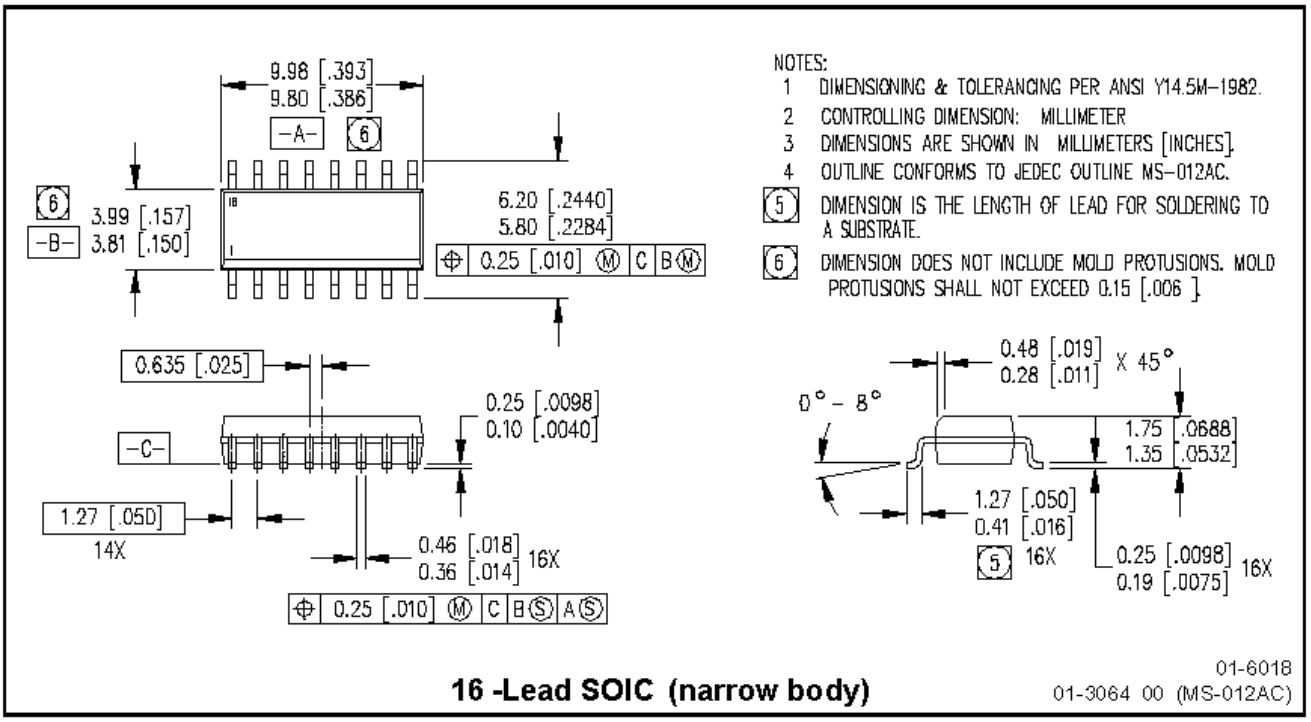
$$R_{OC} = \frac{5}{I_{PFCMAX_PK}} \quad [\Omega] \quad (7)$$

**CaseOutlines**




**16-Lead PDIP**

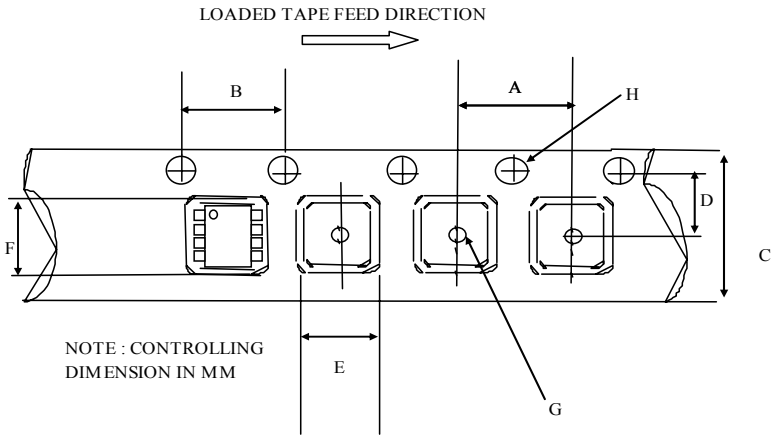
01-6015
01-3065 00 (MS-001A)




**16 -Lead SOIC (narrow body)**

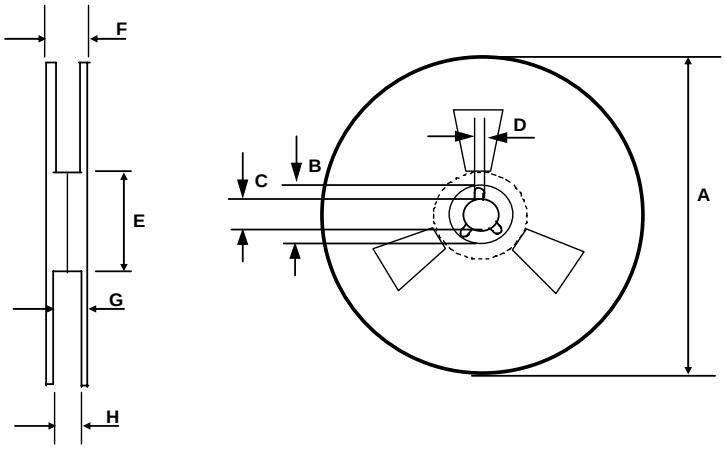
01-6018
01-3064 00 (MS-012AC)

**16-Lead Tape & Reel**




CARRIER TAPE DIMENSION FOR 16SOICN

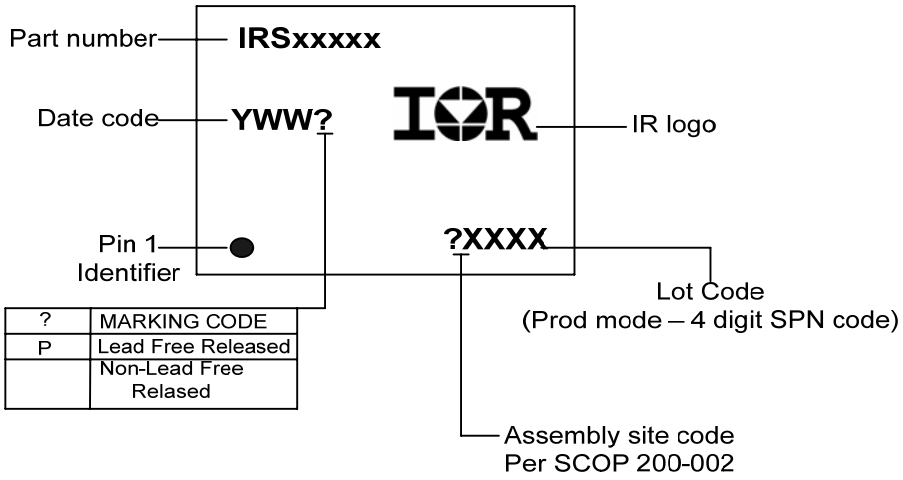
| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 7.90 | 8.10 | 0.311 | 0.318 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 15.70 | 16.30 | 0.618 | 0.641 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 6.40 | 6.60 | 0.252 | 0.260 |
| F | 10.20 | 10.40 | 0.402 | 0.409 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |




REEL DIMENSIONS FOR 16SOICN

| | Metric | | Imperial | |
|---|---|---|---|---|
| Code | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 22.40 | n/a | 0.881 |
| G | 18.50 | 21.10 | 0.728 | 0.830 |
| H | 16.40 | 18.40 | 0.645 | 0.724 |

## LEAD-FREE PART MARKING INFORMATION




| | |
|---|---|
| ? | MARKING CODE |
| P | Lead Free Released |
| | Non-Lead Free Relased |

## ORDER INFORMATION

16-Lead PDIP IRS2166DPbF
16-Lead SOIC IRS2166DSPbF
16-Lead SOIC Tape & Reel IRS2166DSTRPbF

International
IOR Rectifier

The SOIC-16 is MSL2 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com <http://www.irf.com>
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 252-7105
Data and specifications subject to change without notice. 6/27/2006