

μ PA2811T1L

R07DS0191EJ0100

Rev.1.00

Jan 11, 2011

MOS FIELD EFFECT TRANSISTOR

Description

The μ PA2811T1L is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- $V_{DSS} -30\text{ V}$ ($T_A = 25^\circ\text{C}$)
- Low on-state resistance
— $R_{DS(on)} = 15\text{ m}\Omega$ MAX. ($V_{GS} = -10\text{ V}$, $I_D = -19\text{ A}$)
- 4.5 V Gate-drive available
- Built-in gate protection diode
- Small & thin type surface mount package with heat spreader (8-pin HVSON)
- Halogen free and RoHS compliant

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μ PA2811T1L-E1-AY *1	Pure Sn	Tape 3000 p/reel	8-pin HVSON (3333) typ. 0.028 g
μ PA2811T1L-E2-AY *1			

Note: *1. Pb-free (This product does not contain Pb in external electrode.)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0\text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0\text{ V}$)	V_{GSS}	± 25	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 19	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 76	A
Total Power Dissipation *2	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	3.8	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T3}	52	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current *3	I_{AS}	-19	A
Single Avalanche Energy *3	E_{AS}	36	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	2.4	$^\circ\text{C/W}$

Notes: *1. $PW \leq 10\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$

*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

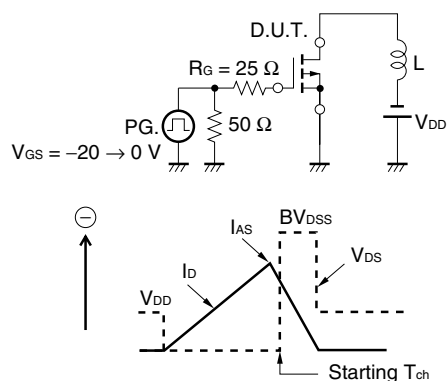
*3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -15\text{ V}$, $R_G = 25\text{ }\Omega$, $V_{GS} = -20 \rightarrow 0\text{ V}$, $L = 100\text{ }\mu\text{H}$

Electrical Characteristics (T_A = 25°C)

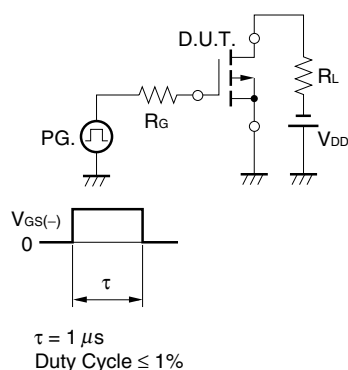
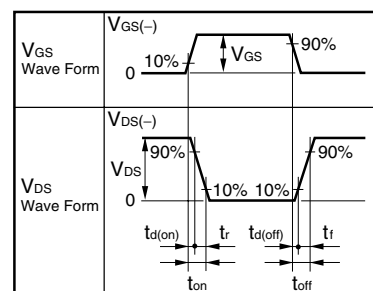
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			-1	μA	V _{DS} = -30 V, V _{GS} = 0 V
Gate Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0 V
Gate Cut-off Voltage	V _{GS(off)}	-1.0		-2.5	V	V _{DS} = -10 V, I _b = -1 mA
Forward Transfer Admittance *1	y _{fs}	7.0			S	V _{DS} = -10 V, I _D = -9.5 A
Drain to Source On-state Resistance *1	R _{DS(on)1}		12	15	mΩ	V _{GS} = -10 V, I _D = -19 A
	R _{DS(on)2}		20	28	mΩ	V _{GS} = -4.5 V, I _D = -9.5 A
Input Capacitance	C _{iss}		1360		pF	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz
Output Capacitance	C _{oss}		310		pF	
Reverse Transfer Capacitance	C _{rss}		240		pF	
Turn-on Delay Time	t _{d(on)}		10		ns	V _{DD} = -15 V, I _D = -9.5 A, V _{GS} = -10 V, R _G = 10 Ω
Rise Time	t _r		14		ns	
Turn-off Delay Time	t _{d(off)}		100		ns	
Fall Time	t _f		70		ns	
Total Gate Charge	Q _G		30		nC	V _{DD} = -24 V, V _{GS} = -10 V, I _D = -19 A
Gate to Source Charge	Q _{GS}		5		nC	
Gate to Drain Charge	Q _{GD}		10		nC	
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9		V	I _F = 19 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		31		ns	I _F = 19 A, V _{GS} = 0 V, di/dt = 100 A/μs
Reverse Recovery Charge	Q _{rr}		27		nC	

Note: *1. Pulsed

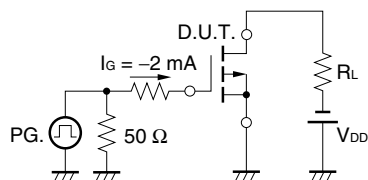
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

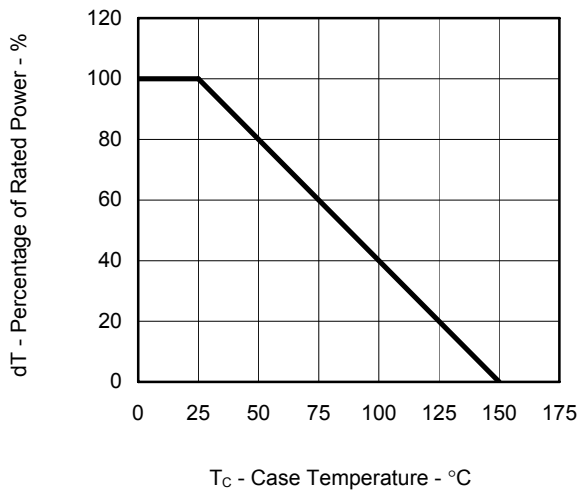


TEST CIRCUIT 3 GATE CHARGE

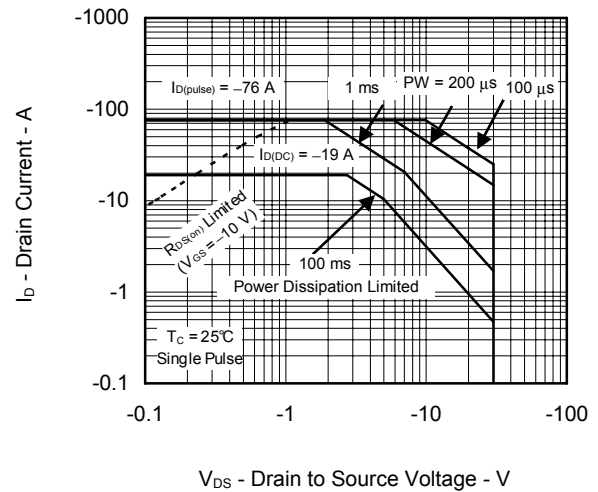


Typical Characteristics ($T_A = 25^\circ\text{C}$)

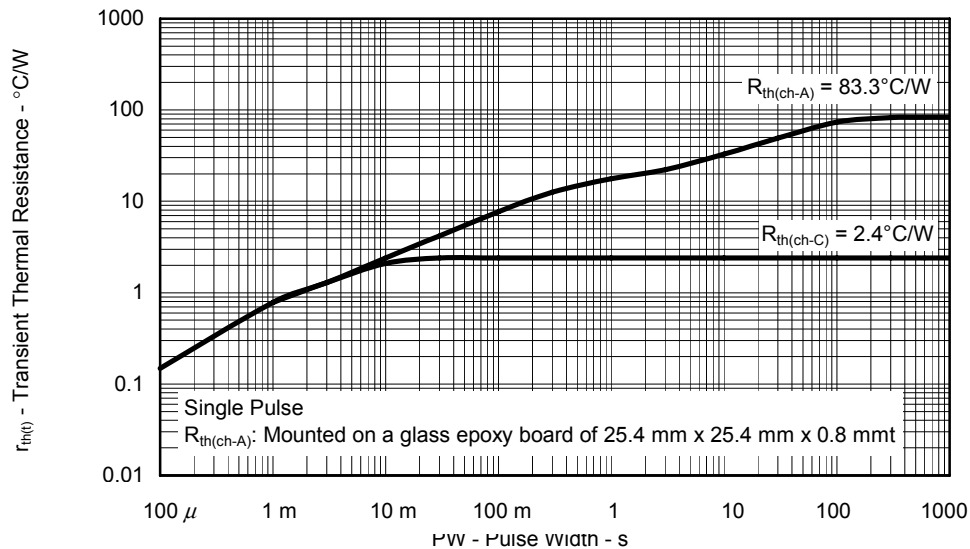
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



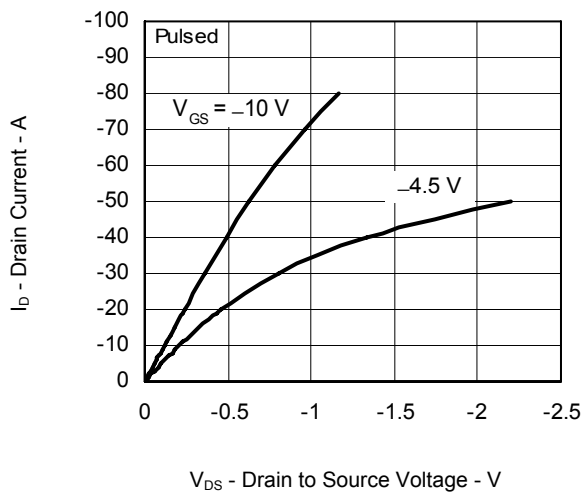
FORWARD BIAS SAFE OPERATING AREA



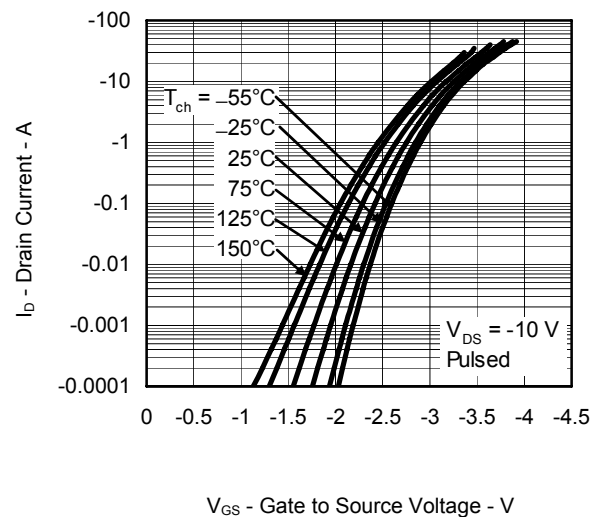
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

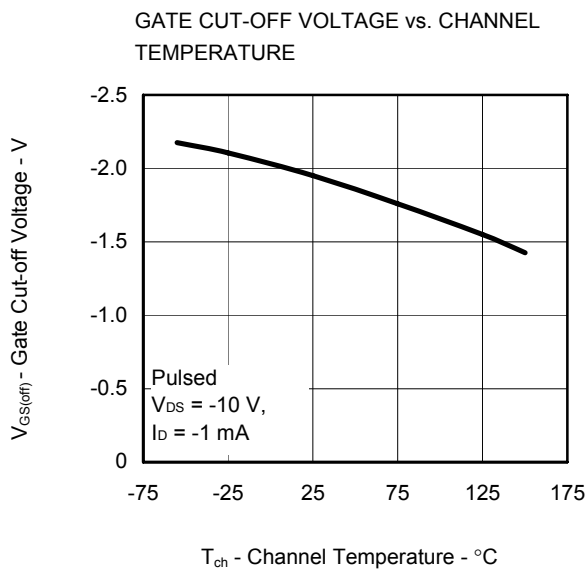
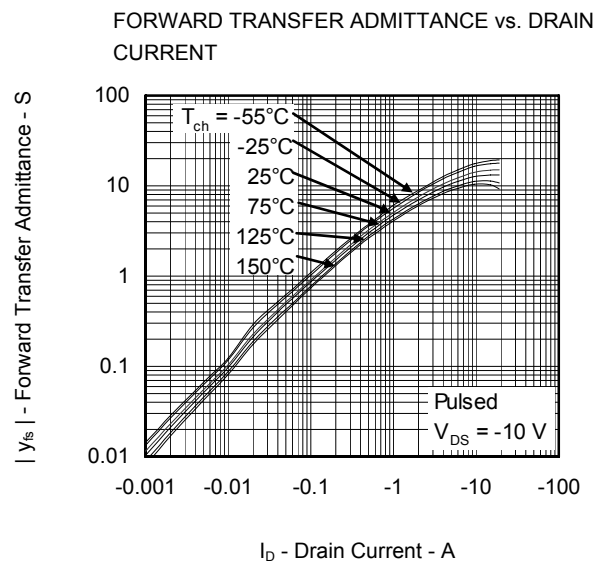
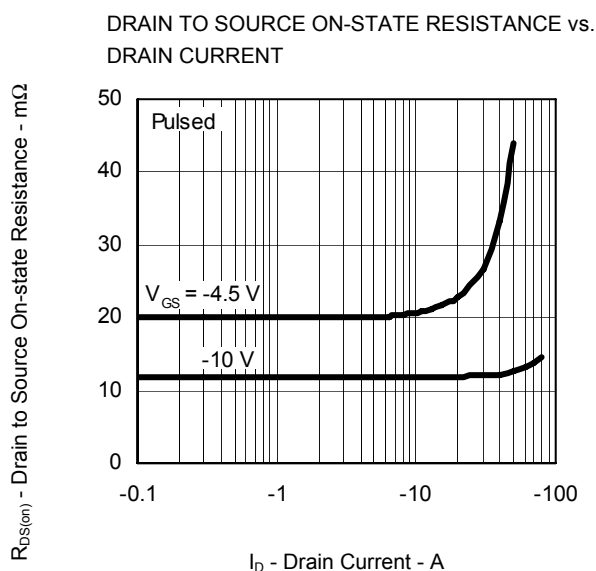
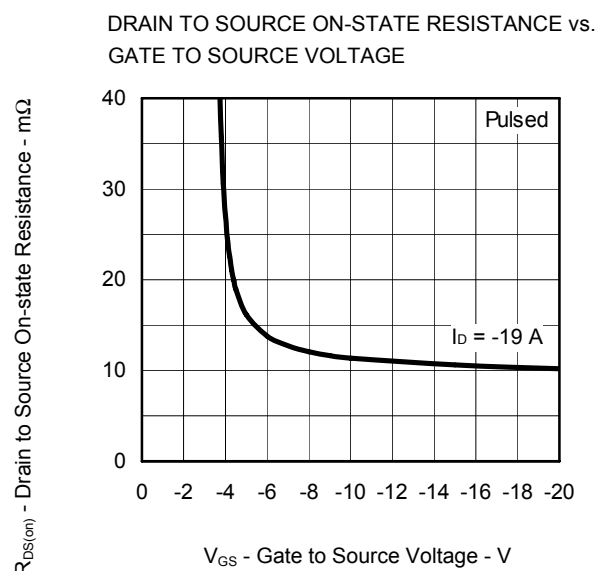
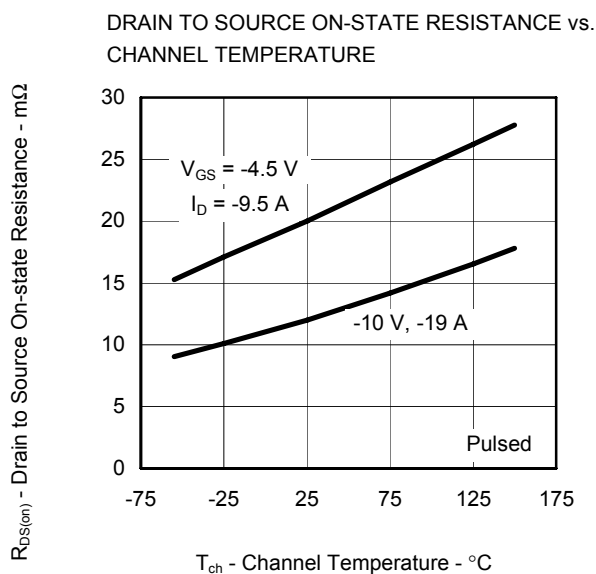
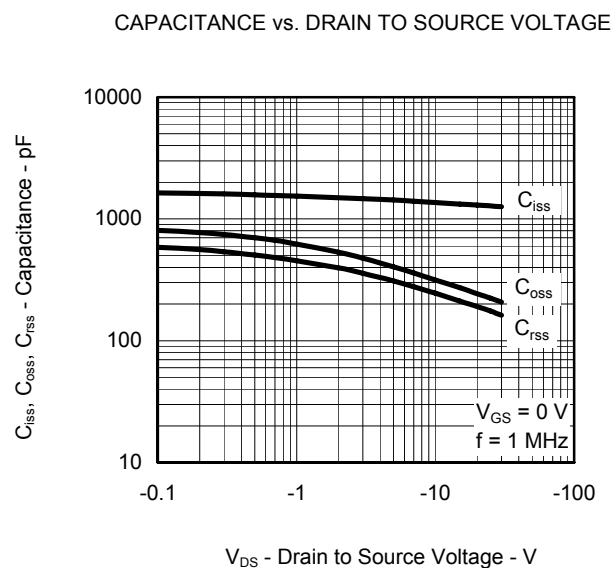


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

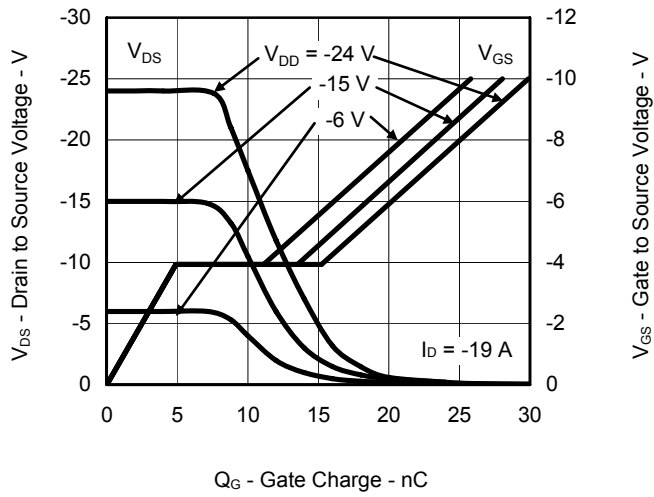


FORWARD TRANSFER CHARACTERISTICS

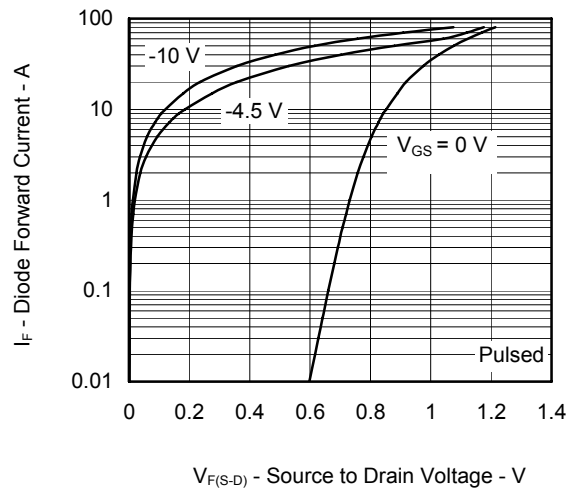




DYNAMIC INPUT/OUTPUT CHARACTERISTICS

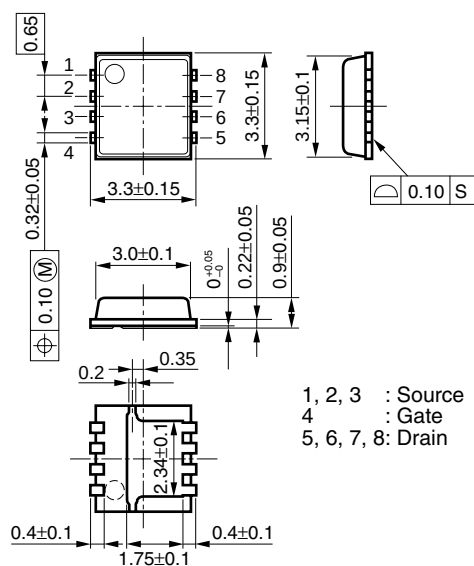


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

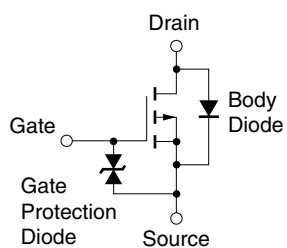


Package Drawings (Unit: mm)

8-pin HVSON (3333)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	μPA2811T1L Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jan 11, 2011	–	First Edition Issued

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