HMS40N65T
650V N-Channel Super Junction MOSFET

Features

- Very Low FOM ($R_{DS(on)}$ X Q_g)
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

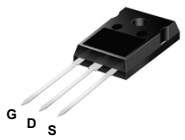
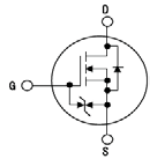
Key Parameters

Parameter	Value	Unit
BV_{DSS} @$T_{j,max}$	700	V
I_D	40	A
$R_{DS(on),\ max}$	68	mΩ
$Qg_{,\ Typ}$	75	nC

Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- AC to DC Converters
- Telecom, Solar

Package & Internal Circuit

TO-247	SYMBOL
	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	650	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current - Continuous (T_C = 25℃)	40	A
	Drain Current - Continuous (T_C = 100℃)	28	A
I_{DM}[1)]	Drain Current - Pulsed	120	A
E_{AS}[2)]	Single Pulsed Avalanche Energy	546	mJ
I_{AR}	Avalanche Current	3.4	A
dv/dt	MOSFET dv/dt ruggedness, VDS=0…400V	50	V/ns
dv/dt	Reverse diode dv/dt, V_{DS}=0…400V, I_{DS}≤I_D	15	V/ns
P_D	Power Dissipation (T_C = 25℃)	205	W
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	2000	V
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.61	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient , Max.	62.5	℃/W

Electrical Characteristics T_J=25 °C unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
On Characteristics						
V_{GS}	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1.29 mA	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 11.9 A	-	68	78	mΩ
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1mA	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0	-	-	5	μA
		V_{DS} = 650 V, T_C = 150℃	-	-	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±1	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1.0 MHz	-	3300	-	pF
C_{oss}	Output Capacitance		-	69	-	pF
C_{rss}	Reverse Transfer Capacitance		-	3.7	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	V_{DS} = 325 V, I_D = 16.7 A, R_G = 25 Ω (Note 3,4)	-	63	-	ns
t_r	Turn-On Rise Time		-	32	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	281	-	ns
t_f	Turn-Off Fall Time		-	20	-	ns
$Q_{g(}$	Total Gate Charge	V_{DS} = 520 V, I_D = 16.7 A, V_{GS} = 10 V (Note 3,4)	-	75	-	nC
Q_{gs}	Gate-Source Charge		-	14	-	nC
Q_{gd}	Gate-Drain Charge		-	22	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	40	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		-	-	120	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 16.7 A	-	-	1.3	V
trr	Reverse Recovery Time	V_R = 400 V, I_F = 16.7 A, di_F/dt = 100 A/μs	-	445	-	ns
Qrr	Reverse Recovery Charge		-	7.7	-	μC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{AS}=3.4A V_{DD}=100V, R_G=25Ω, Starting T_J=25°C
3. Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%
4. Essentially Independent of Operating Temperature

Typical Characteristics

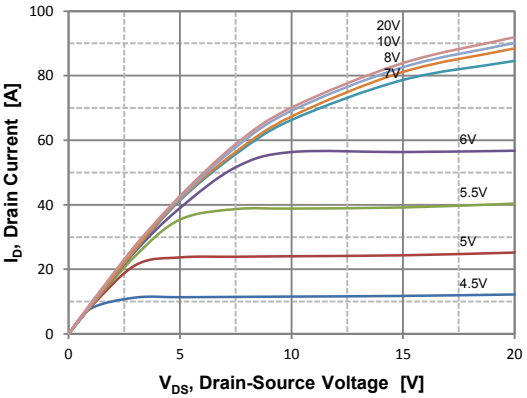


Figure 1. On Region Characteristics

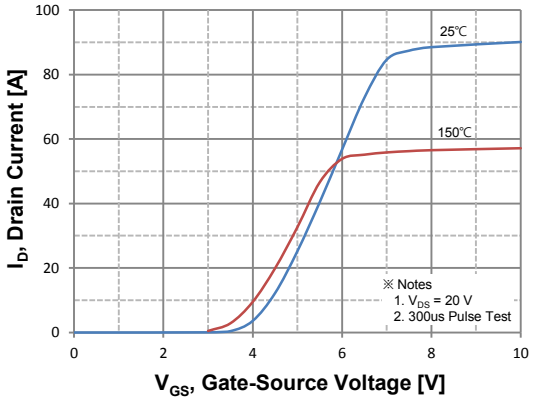


Figure 2. Transfer Characteristics

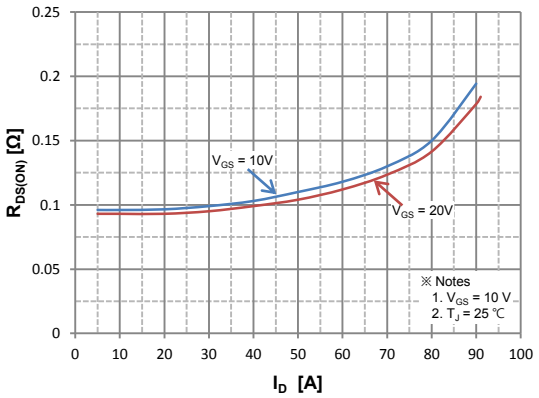


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

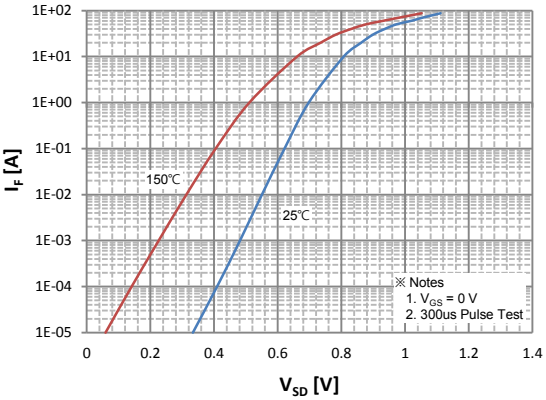


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

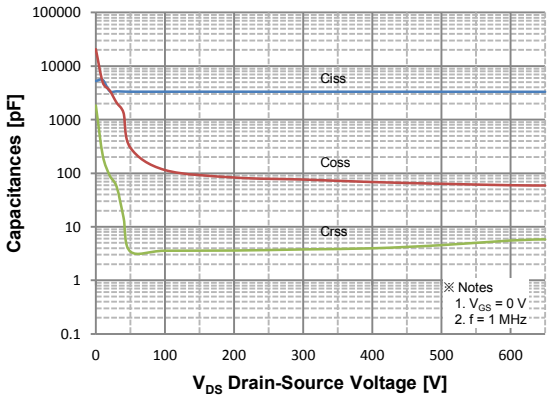


Figure 5. Capacitance Characteristics

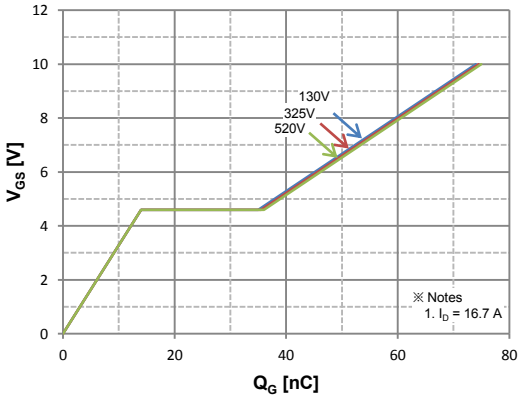


Figure 6. Gate Charge Characteristics

Typical Characteristics

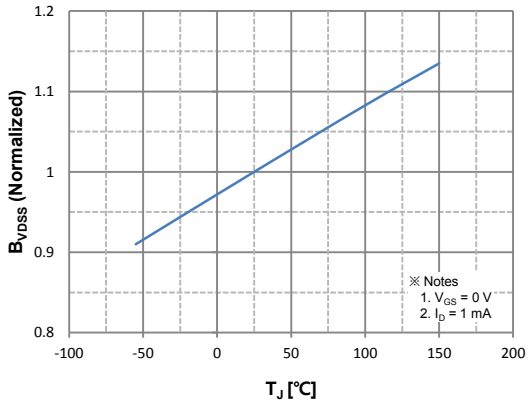


Figure 7. Breakdown Voltage Variation vs. Temperature

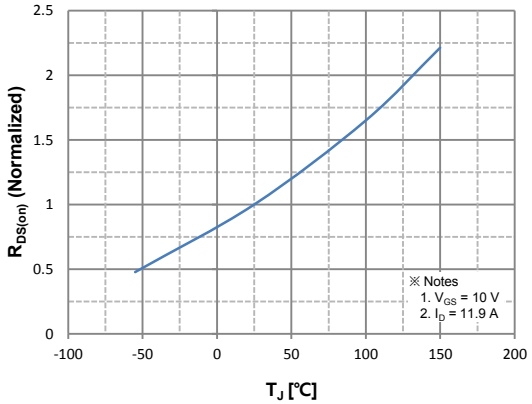


Figure 8. On-Resistance Variation vs. Temperature

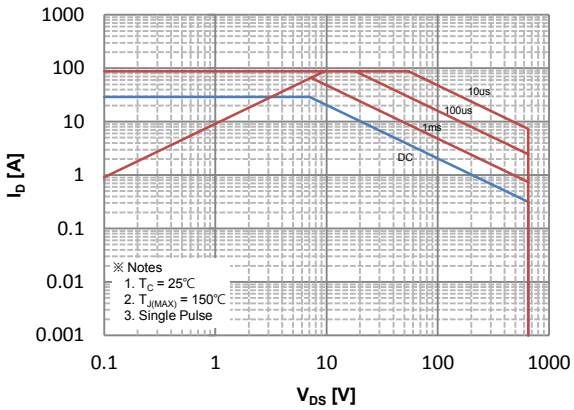


Figure 9. Maximum Safe Operating Area

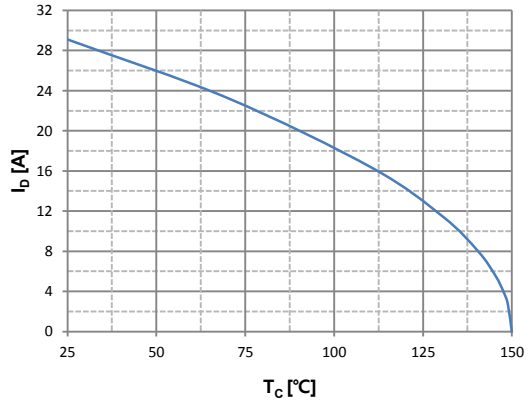


Figure 10. Maximum Drain Current vs. Case Temperature

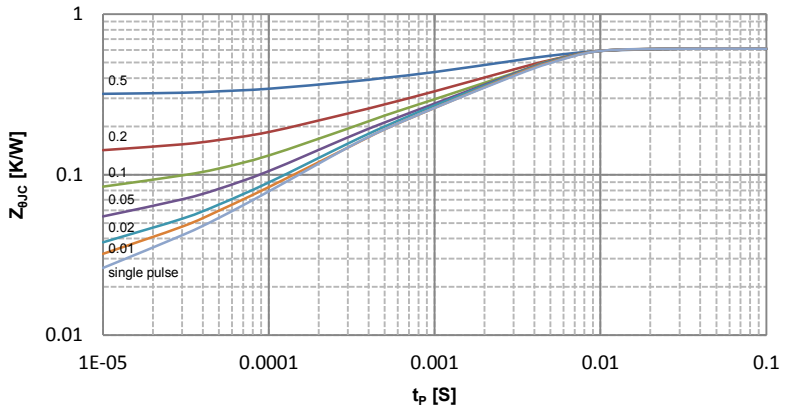


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

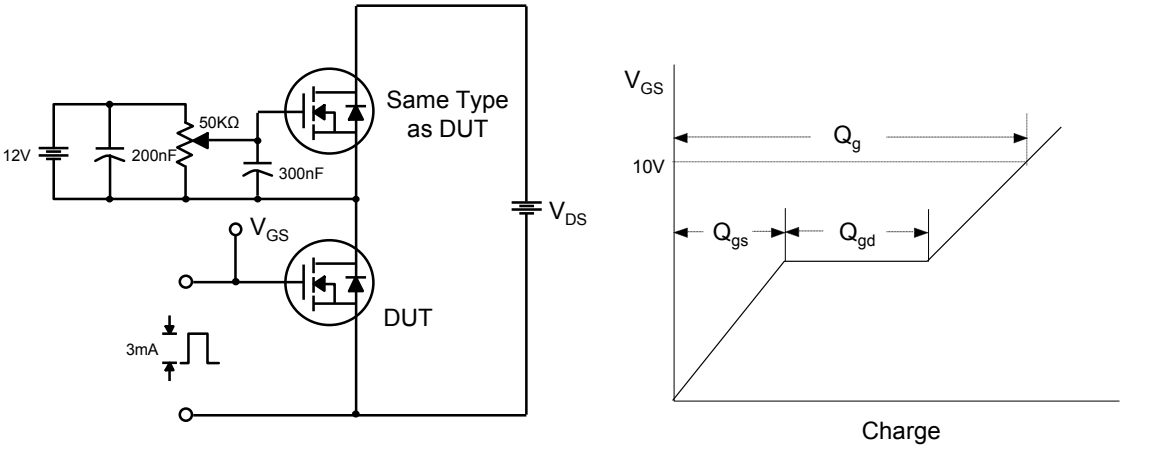


Fig 13. Resistive Switching Test Circuit & Waveforms

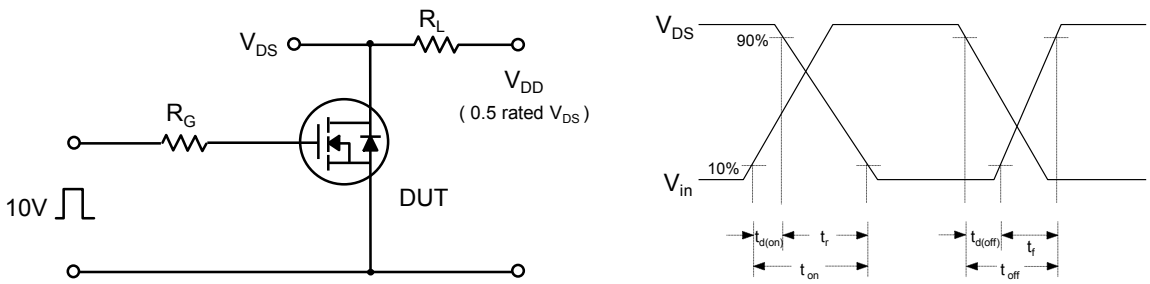


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

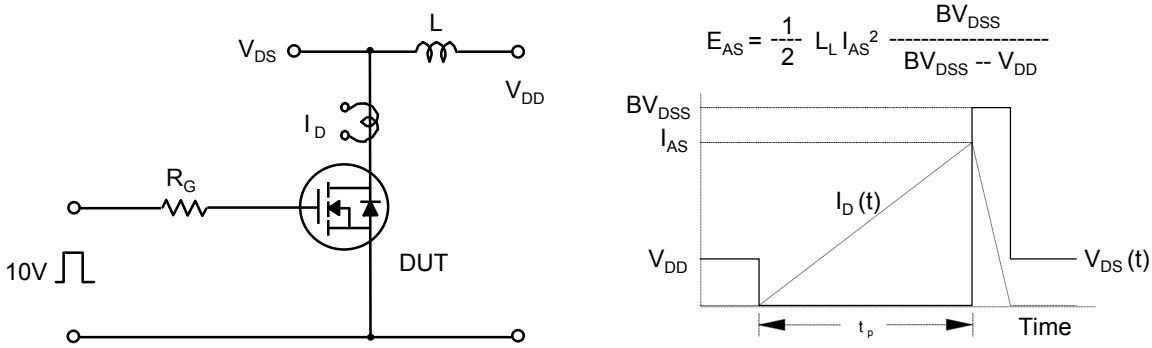
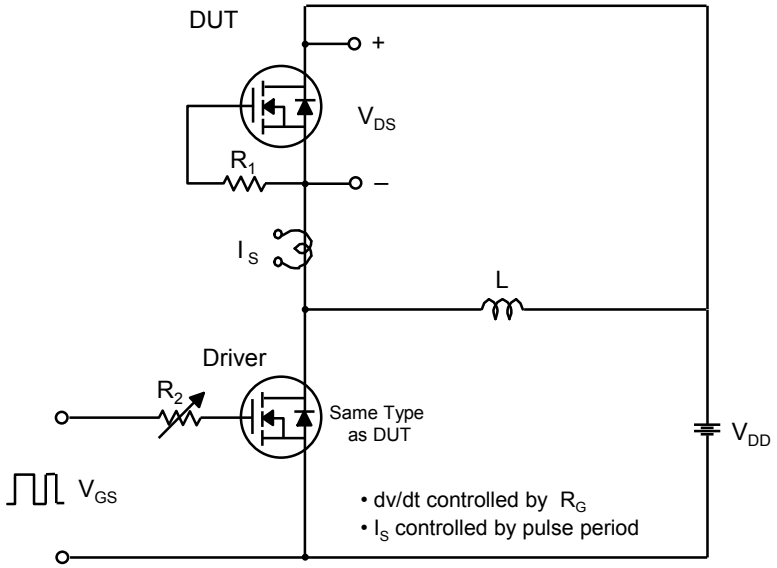
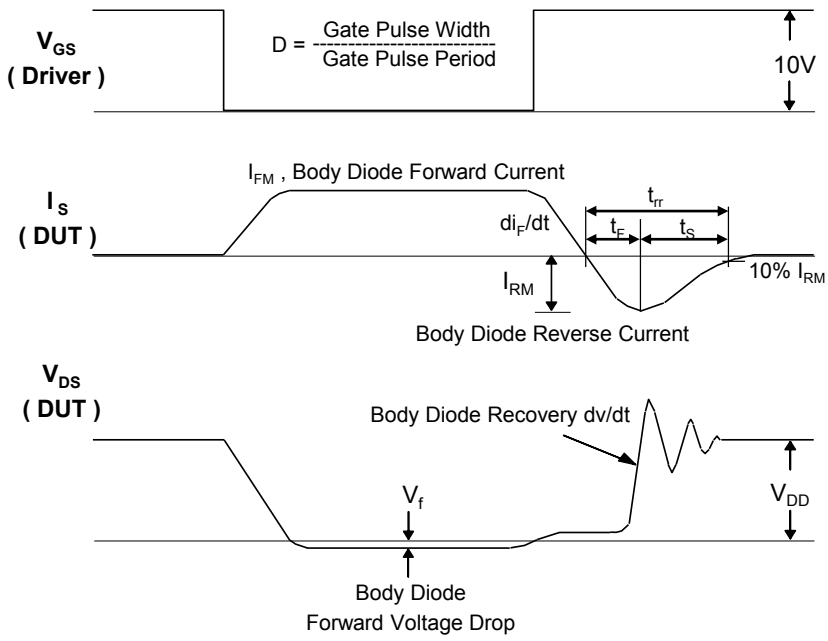


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimension

TO-247

