

Hybrid Quad Silicon Junction Field-Effect Transistor Array

- Analog Multiplier
- VHF Double-Balanced Mixer

Absolute maximum ratings at $T_A = 25^\circ\text{C}$.

Reverse Gate Source & Reverse Gate Drain Voltage

– 25 V

Gate Current

25 mA

Continuous Device Power Dissipation

400 mW

Power Derating

3.2 mW/°C

At 25°C free air temperature:

Static Electrical Characteristics

		U350			Four Matched Process NJ72L		
		Min	Typ	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	– 25			V	$I_G = -1\ \mu\text{A}$, $V_{DS} = \emptyset\text{V}$	
Gate Reverse Current	I_{GSS}			– 1	nA	$V_{GS} = -15\text{V}$, $V_{DS} = \emptyset\text{V}$	
				– 1	μA	$V_{GS} = -15\text{V}$, $V_{DS} = \emptyset\text{V}$	$T_A = 125^\circ\text{C}$
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 2		– 6	V	$V_{DS} = 10\text{V}$, $I_D = 1\ \text{nA}$	
Gate Source Forward Voltage	$V_{GS(F)}$			1	V	$V_{DS} = \emptyset\text{V}$, $I_G = 1\ \text{mA}$	
Drain Saturation Current (Pulsed)	I_{DSS}	24		60	mA	$V_{DS} = 15\text{V}$, $V_{GS} = \emptyset\text{V}$	

Dynamic Electrical Characteristics

Drain Source ON Resistance	$r_{ds(on)}$		50	90	Ω	$V_{GS} = \emptyset\text{V}$, $I_D = \text{mA}$	$f = 1\ \text{kHz}$
Common Source Forward Transconductance	g_{fs}	10		18	mS	$V_{DS} = 10\text{V}$, $I_D = 10\ \text{mA}$	$f = 1\ \text{kHz}$
Common Source Output Conductance	g_{os}			150	μS	$V_{DS} = 10\text{V}$, $I_D = 10\ \text{mA}$	$f = 1\ \text{kHz}$
Drain Gate Capacitance	C_{dgo}			2.5	pF	$V_{GD} = -10\text{V}$, $I_S = \emptyset\text{V}$	$f = 1\ \text{MHz}$
Gate Source Capacitance	C_{sgo}			5	pF	$V_{GS} = -10\text{V}$, $I_D = \emptyset\text{V}$	$f = 1\ \text{MHz}$
(Conversion Gain)	G_c		4		dB	$V_{DS} = 20\text{V}$, $V_{GS} = 1/2\ V_{GS(OFF)}$ $R_D = 1,700\ \Omega$	$f = 100\ \text{MHz}$
Noise Figure	NF		7		dB	$V_{DS} = 20\text{V}$, $V_{GS} = 1/2\ V_{GS(OFF)}$ $R_D = 1,700\ \Omega$	$f = 100\ \text{MHz}$
Saturation Drain Current Ratio	I_{DSS} / I_{DSS}	0.9		1		$V_{DS} = 15\text{V}$, $V_{DS} = \emptyset\text{V}$	
Gate Source Cutoff Voltage Ratio	$V_{GS(OFF)} / V_{GS(OFF)}$	0.9		1		$V_{DS} = 15\text{V}$, $I_D = 1\ \text{nA}$	
Common Source Forward Transconductance	g_{fs} / g_{fs}	0.9		1		$V_{DS} = 15\text{V}$, $I_D = 10\ \text{mA}$	$f = 1\ \text{kHz}$
Differential Output Conductance	Y_{os} / Y_{os}	0.9		1		$V_{DS} = 15\text{V}$, $I_D = 10\ \text{mA}$	$f = 1\ \text{kHz}$

TO-78 Package

Dimensions in Inches (mm)

Pin Configuration

1 Gate 1 & 3, 2 Drain 1 & 4,
3 Source 1 & 2, 4 Ground & Case,
5 Source 3 & 4, 6 Drain 2 & 3,
7 Gate 2 & 4, 8 Omitted



InterFET Corporation

1000 N. Shiloh Road, Garland, TX 75042

(972) 487-1287 FAX (972) 276-3375