# TS3USB221A ESD Protected, High-Speed USB 2.0 (480-Mbps) 1:2 Multiplexer and Demultiplexer Switch With Single Enable

## 1 Features

- $V_{CC}$ Operation at 2.5 V to 3.3 V
- $V_{I/O}$ Accepts Signals Up to 5.5 V
- 1.8-V Compatible Control-Pin Inputs
- Low-Power Mode When $\overline{OE}$ Is Disabled (1 µA)
- $R_{ON}$ = 6 Ω Maximum
- $\Delta R_{ON}$ = 0.2 Ω Typical
- $C_{io(on)}$ = 6 pF Typical
- Low Power Consumption (30 µA Maximum)
- High Bandwidth (900 MHz Typical)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 7000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance I/O to GND
  - 12-kV Human-Body Model

## 2 Applications

- Routes Signals for USB 1.0, 1.1, and 2.0
- Mobile Phones
- Cameras
- Notebooks
- USB I/O expansion

## 3 Description

The TS3USB221A device is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that will reduce the power consumtion to 1 µA for portible applications with a battery or limited power budget. The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

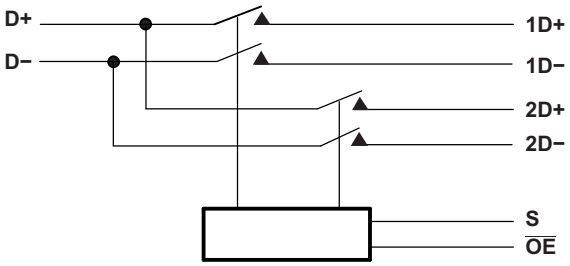
The TS3USB221A device integrates ESD protection cells on all pins, is available in a tiny µQFN package (2 mm × 1.5 mm) and is characterized over the free air temperature range from –40°C to 85°C.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TS3USB221A | UQFN | 1.50 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Schematic




EN is the internal enable signal applied to the switch.

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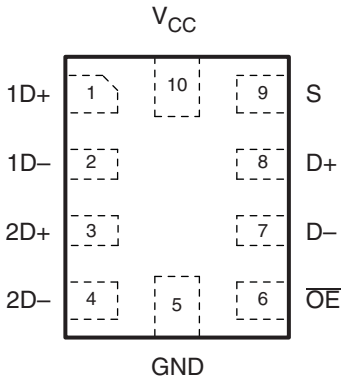
## 5 Revision History

**Changes from Original (November 2008) to Revision A** **Page**

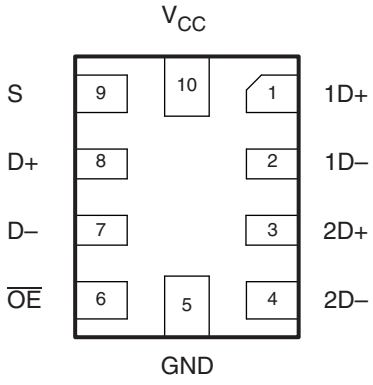
- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Deleted the *Ordering Information* table from the data sheet. See the *Mechanical, Packaging, and Orderable Information* section for the ordering information ... 1
- Update the document to the new TI data sheet standard ... 1

# 6 Pin Configuration and Functions

**10-Pin µQFN**
**RSE Package**
**(Top View)**




**10-Pin µQFN**
**RSE Package**
**(Bottom View)**




**Pin Functions**

| PIN | | | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | I/O | |
| 1D+ | 1 | I/O | USB port 1 |
| 1D– | 2 | I/O | |
| 2D+ | 3 | I/O | USB port 2 |
| 2D– | 4 | I/O | |
| GND | 5 | - | Ground |
| $\overline{OE}$ | 6 | I | Bus-switch enable |
| D+ | 8 | I/O | Common USB port |
| D— | 7 | I/O | |
| S | 9 | I | Select input |
| $V_{CC}$ | 10 | - | Supply voltage |

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | –0.5 | 4.6 | V |
| Control input voltage, $V_S$, $V_{\overline{OE}}$ (2) (3) | | –0.5 | 7 | V |
| Switch I/O voltage, $V_{I/O}$ (2) (3) (4) | | –0.5 | 7 | V |
| Control input clamp current, $I_{IK}$ | $V_{IN} < 0$ | | –50 | mA |
| I/O port clamp current, $I_{I/OK}$ | $V_{I/O} < 0$ | | –50 | mA |
| ON-state switch current, $I_{I/O}$ (5) | | | ±120 | mA |
| Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
(5) $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins except I/O to GND | ±7000 | V |
| | | | I/O to GND | ±12000 | |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | All pins | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 7.3 Recommended Operating Conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_S$, $V_{\overline{OE}}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 0.46 × $V_{CC}$ | $V_{CC}$ | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0.46 × $V_{CC}$ | $V_{CC}$ | |
| | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.25 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | 0.25 × $V_{CC}$ | |
| $V_{I/O}$ | Data input/output voltage | | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | RSE | UNIT |
|---|---|---|---|
| | | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 179.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 107.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 100.7 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.1 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 100.0 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics(1)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(2) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input-Source Clamp Voltage | $V_{CC}$ = 3.6 V, 2.7 V, $I_I$ = –18 mA | | | | –1.8 | V |
| $I_{IN}$ | Input leakage current, control inputs | $V_{CC}$ = 3.6 V, 2.7 V, 0 V, $V_{IN}$ = 0 V to 3.6 V | | | | ±1 | µA |
| $I_{OZ}$ (3) | Off-state leakage current | $V_{CC}$ = 3.6 V, 2.7 V, $V_O$ = 0 V to 5.25 V, $V_I$ = 0 V, $V_{IN}$ = $V_{CC}$ or GND, Switch OFF | | | | ±1 | µA |
| $I_{(OFF)}$ | Power-off leakage current | $V_{CC}$ = 0 V | $V_{I/O}$ = 0 V to 5.25 V | | | ±2 | µA |
| | | | $V_{I/O}$ = 0 V to 3.6 V | | | ±2 | |
| | | | $V_{I/O}$ = 0 V to 2.7 V | | | ±1 | |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 3.6 V, 2.7 V, $V_{IN}$ = $V_{CC}$ or GND, $I_{I/O}$ = 0 V, Switch ON or OFF | | | | 30 | µA |
| $I_{CC}$ | Supply Current (low power mode) | $V_{CC}$ = 3.6 V, 2.7 V, $V_{IN}$ = $V_{CC}$ or GND, Switch disabled, $\overline{OE}$ in high state | | | | 1 | µA |
| $\Delta I_{CC}$ (4) | Supply-current change, control inputs | One input at 1.8 V, Other inputs at $V_{CC}$ or GND | $V_{CC}$ = 3.6 V | | | 20 | µA |
| | | | $V_{CC}$ = 2.7 V | | | 0.5 | |
| $C_{in}$ | Input capacitance, control inputs | $V_{CC}$ = 3.3 V, 2.5 V, $V_{IN}$ = $V_{CC}$ or 0 V | | | 1.5 | 2.5 | pF |
| $C_{io(OFF)}$ | OFF capacitance | $V_{CC}$ = 3.3 V, 2.5 V, $V_{I/O}$ = $V_{CC}$ or 0 V, Switch OFF | | | 3.5 | 5 | pF |
| $C_{io(ON)}$ | ON capacitance | $V_{CC}$ = 3.3 V, 2.5 V, $V_{I/O}$ = $V_{CC}$ or 0 V, Switch ON | | | 6 | 7.5 | pF |
| $R_{ON}$ (5) | ON-state resistance | $V_{CC}$ = 3 V, 2.3 V | $V_I$ = 0 V, $I_O$ = 30 mA | | 3 | 6 | Ω |
| | | | $V_I$ = 2.4 V, $I_O$ = –15 mA | | 3.4 | 6 | |
| $\Delta R_{ON}$ | ON-state resistance match between channels | $V_{CC}$ = 3 V, 2.3 V | $V_I$ = 0 V, $I_O$ = 30 mA | | 0.2 | | Ω |
| | | | $V_I$ = 1.7, $I_O$ = –15 mA | | 0.2 | | |
| $R_{ON(flat)}$ | ON-state resistance flatness | $V_{CC}$ = 3 V, 2.3 V | $V_I$ = 0 V, $I_O$ = 30 mA | | 1 | | Ω |
| | | | $V_I$ = 1.7, $I_O$ = –15 mA | | 1 | | |

(1) $V_{IN}$ and $I_{IN}$ refer to control inputs. $V_I$, $V_O$, $I_I$, and $I_O$ refer to data pins.
(2) All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 7.6 Dynamic Electrical Characteristics, $V_{CC}$ = 3.3 V ±10%

over operating range, $T_A$ = –40°C to 85°C, $V_{CC}$ = 3.3 V ±10%, GND = 0 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 , f = 250 MHz | | –40 | | dB |
| $O_{IRR}$ | OFF isolation | $R_L$ = 50 , f = 250 MHz | | –41 | | dB |
| BW | Bandwidth (–3 dB) | $R_L$ = 50 | | 0.9 | | GHz |

## 7.7 Dynamic Electrical Characteristics, $V_{CC}$ = 2.5 V ±10%

over operating range, $T_A$ = –40°C to 85°C, $V_{CC}$ = 2.5 V ±10%, GND = 0 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 , f = 250 MHz | | –39 | | dB |
| $O_{IRR}$ | OFF isolation | $R_L$ = 50 , f = 250 MHz | | -40 | | dB |
| BW | Bandwidth (3 dB) | $R_L$ = 50 | | 0.9 | | GHz |

## 7.8 Switching Characteristics, $V_{CC}$ = 3.3 V ±10%

over operating range, $T_A$ = –40°C to 85°C, $V_{CC}$ = 3.3 V ±10%, GND = 0 V

| PARAMETER | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay(2) (3) | | | 0.25 | | ns |
| $t_{ON}$ | Line enable time | S to D, nD | | | 30 | ns |
| | | $\overline{OE}$ to D, nD | | | 17 | |
| $t_{OFF}$ | Line disable time | S to D, nD | | | 12 | ns |
| | | $\overline{OE}$ to D, nD | | | 10 | |
| $t_{SK(O)}$ | Output skew between center port to any other port(2) | | | 0.1 | 0.2 | ns |
| $t_{SK(P)}$ | Skew between opposite transitions of the same output ($t_{PHL}$ – $t_{PLH}$)(2) | | | 0.1 | 0.2 | ns |

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

## 7.9 Switching Characteristics, $V_{CC}$ = 2.5 V ±10%

over operating range, $T_A$ = –40°C to 85°C, $V_{CC}$ = 2.5 V ±10%, GND = 0 V

| PARAMETER | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay(2) (3) | | | 0.25 | | ns |
| $t_{ON}$ | Line enable time | S to D, nD | | | 50 | ns |
| | | $\overline{OE}$ to D, nD | | | 32 | |
| $t_{OFF}$ | Line disable time | S to D, nD | | | 23 | ns |
| | | $\overline{OE}$ to D, nD | | | 12 | |
| $t_{SK(O)}$ | Output skew between center port to any other port(2) | | | 0.1 | 0.2 | ns |
| $t_{SK(P)}$ | Skew between opposite transitions of the same output ($t_{PHL}$ – $t_{PLH}$)(2) | | | 0.1 | 0.2 | ns |

(1) For Max or Min conditions, use the appropriate value specified under Electrical Characteristics for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

## 7.10 Typical Characteristics

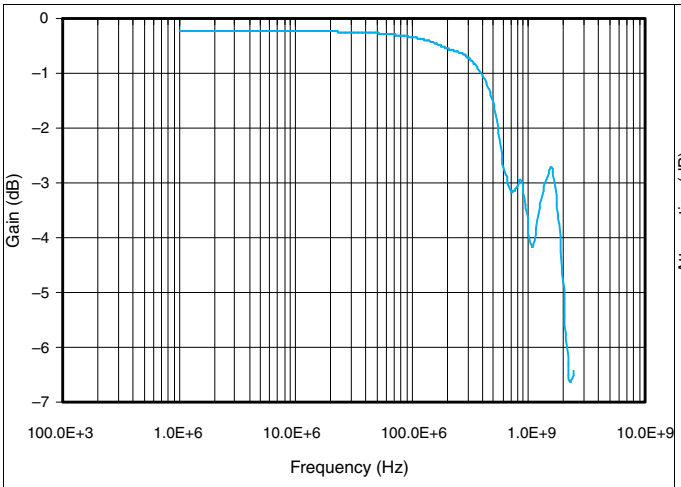



**Figure 1. Gain vs Frequency**

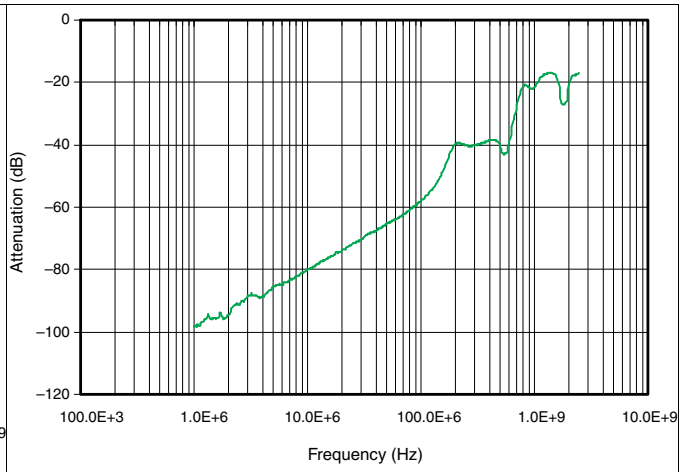



**Figure 2. OFF Isolation vs Frequency**

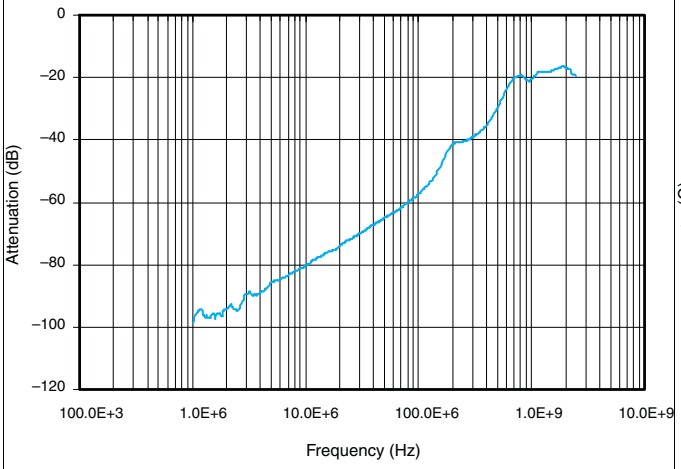



**Figure 3. Crosstalk vs Frequency**

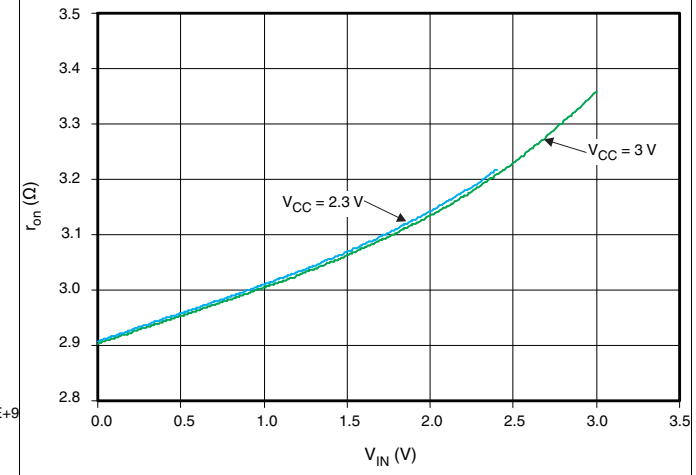



**Figure 4. $r_{on}$ vs $V_{IN}$ ($I_{OUT}$ = –15 mA)**

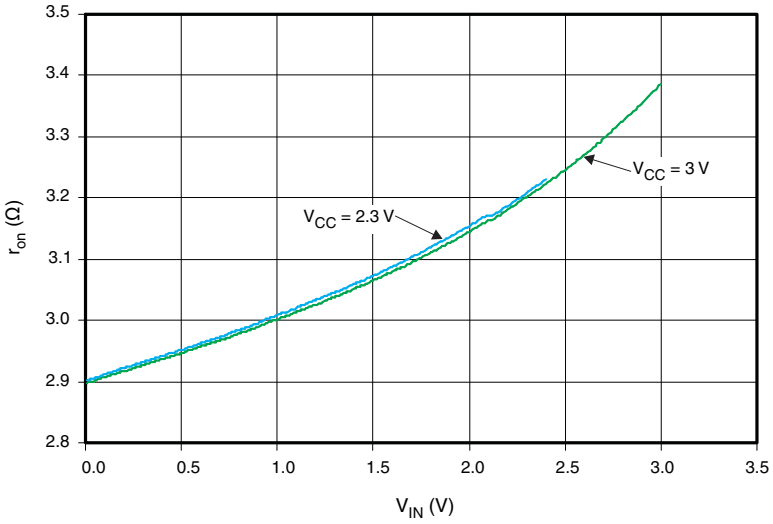
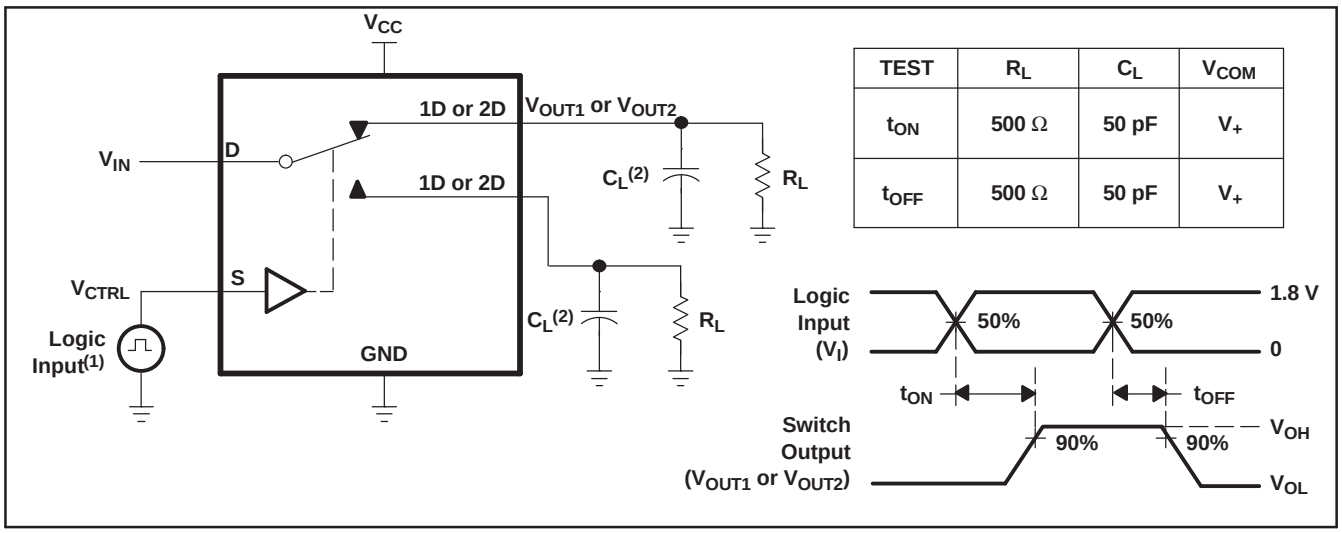



**Figure 5. $r_{ON}$ vs $V_{IN}$ ($I_{OUT}$ = 30 mA)**

# 8 Parameter Measurement Information




| TEST | $R_L$ | $C_L$ | $V_{COM}$ |
|---|---|---|---|
| $t_{ON}$ | 500 Ω | 50 pF | $V_+$ |
| $t_{OFF}$ | 500 Ω | 50 pF | $V_+$ |

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.
(2) $C_L$ includes probe and jig capacitance.

**Figure 6. Turn-On ($t_{ON}$) and Turn-Off Time ($t_{OFF}$)**

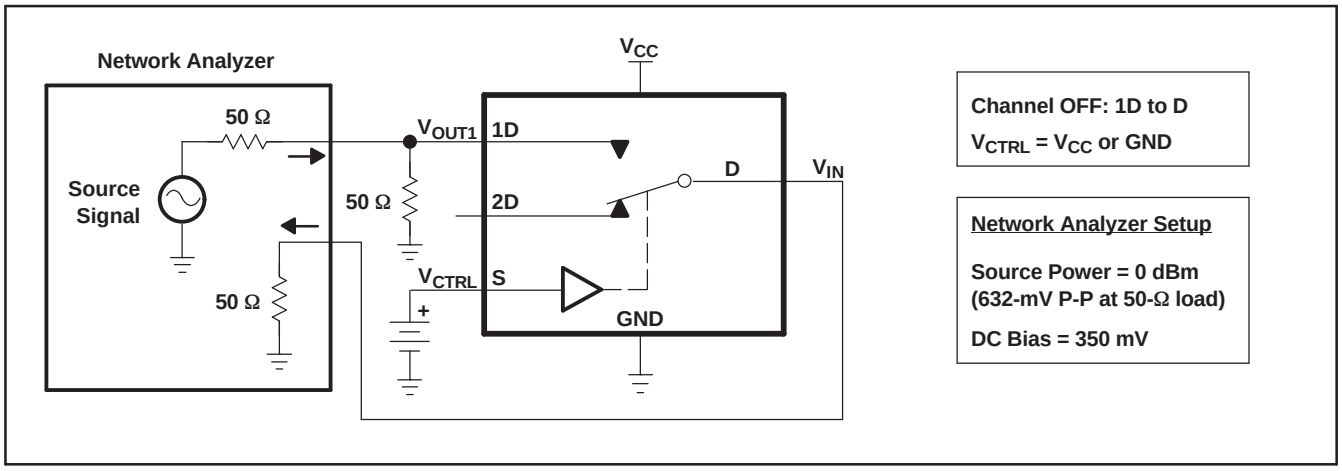



**Figure 7. OFF Isolation ($O_{ISO}$)**

## Parameter Measurement Information (continued)

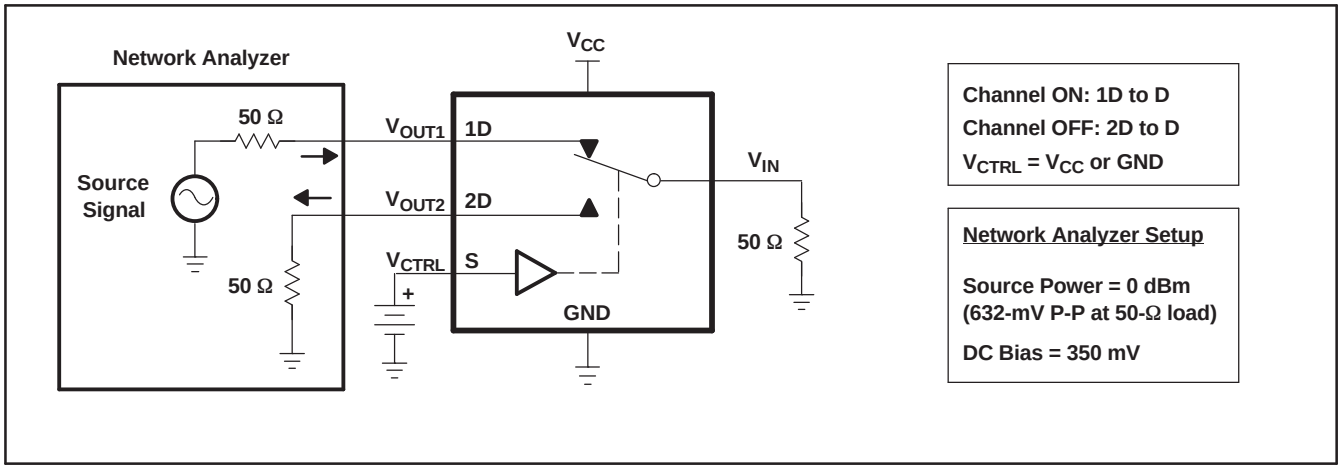



**Figure 8. Crosstalk ($X_{TALK}$)**

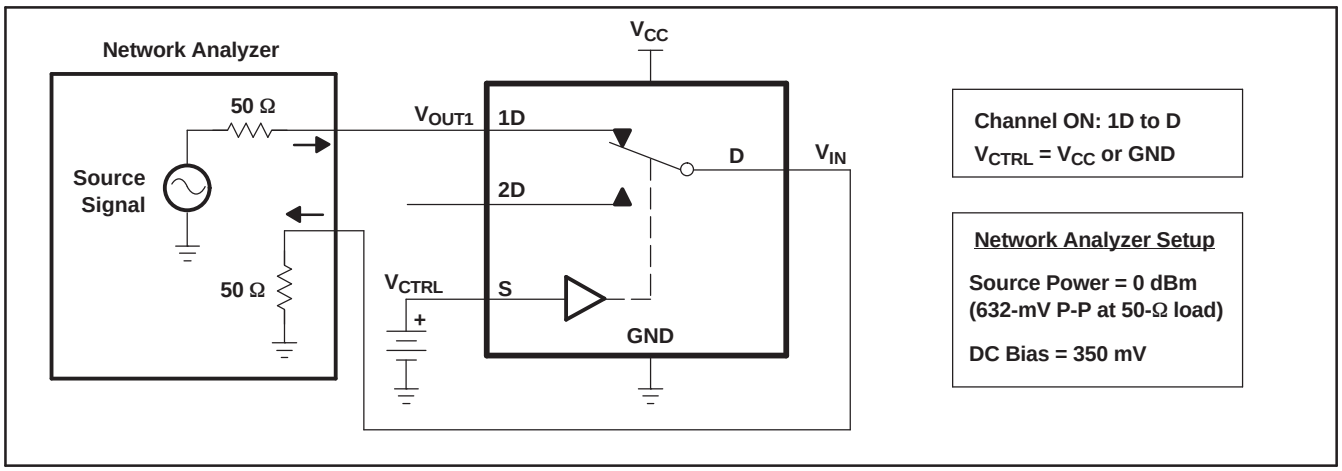



**Figure 9. Bandwidth (BW)**

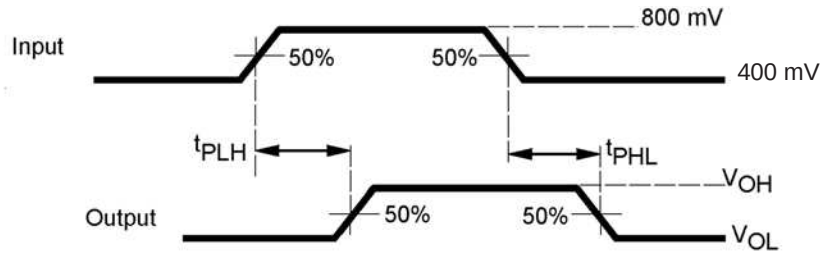



**Figure 10. Propagation Delay**

## Parameter Measurement Information (continued)

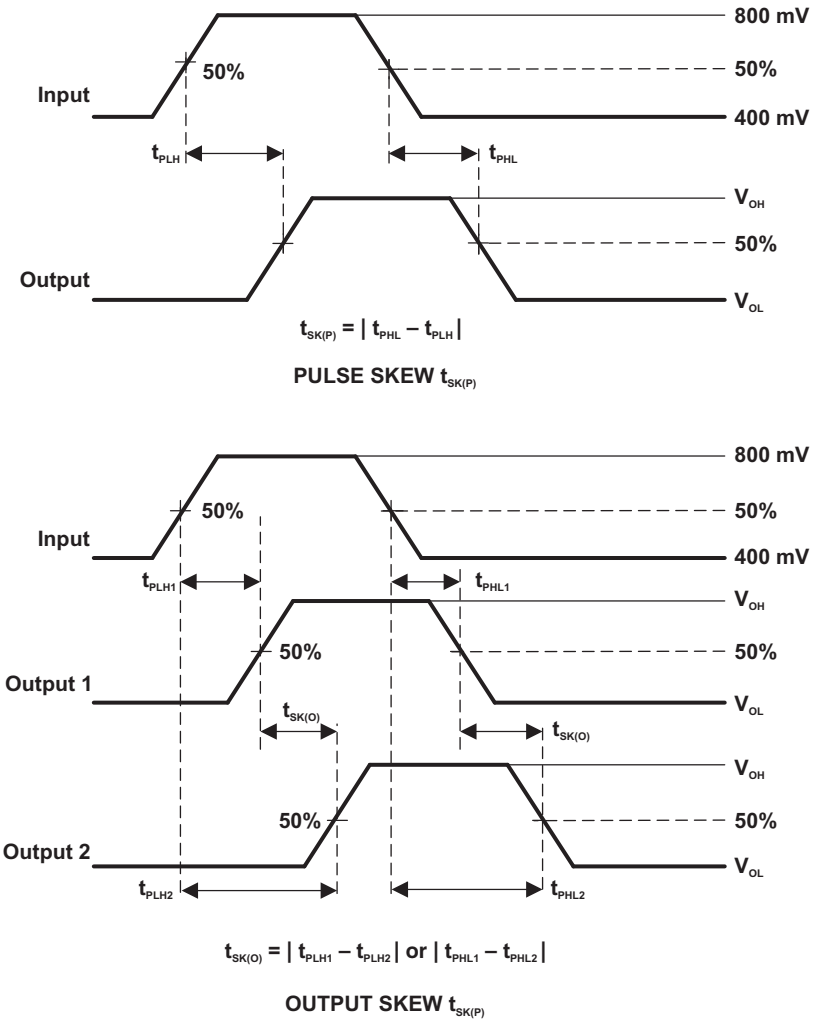



**Figure 11. Skew Test**

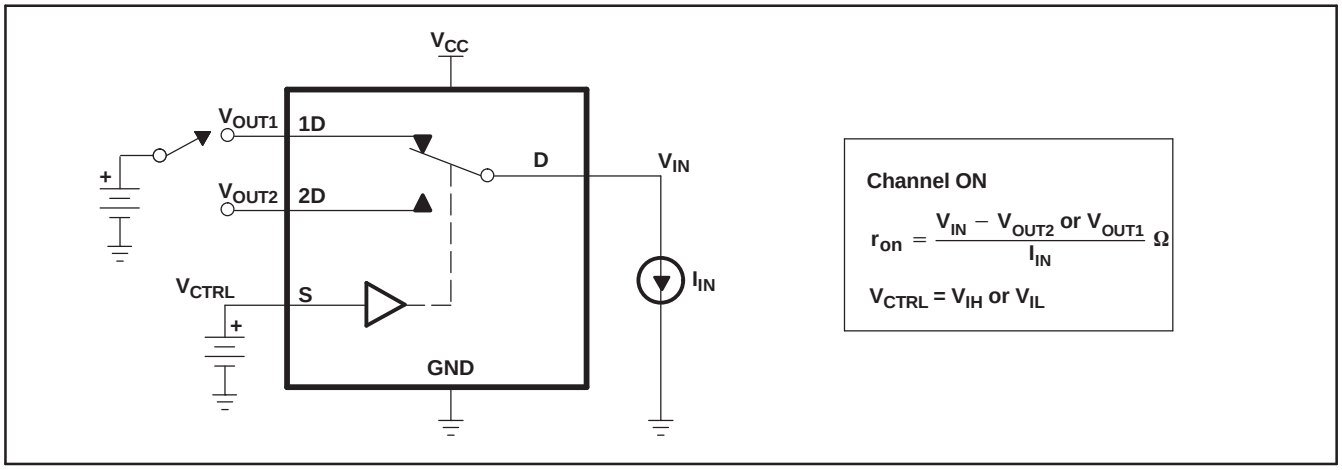



**Figure 12. ON-State Resistance ($r_{on}$)**

## Parameter Measurement Information (continued)

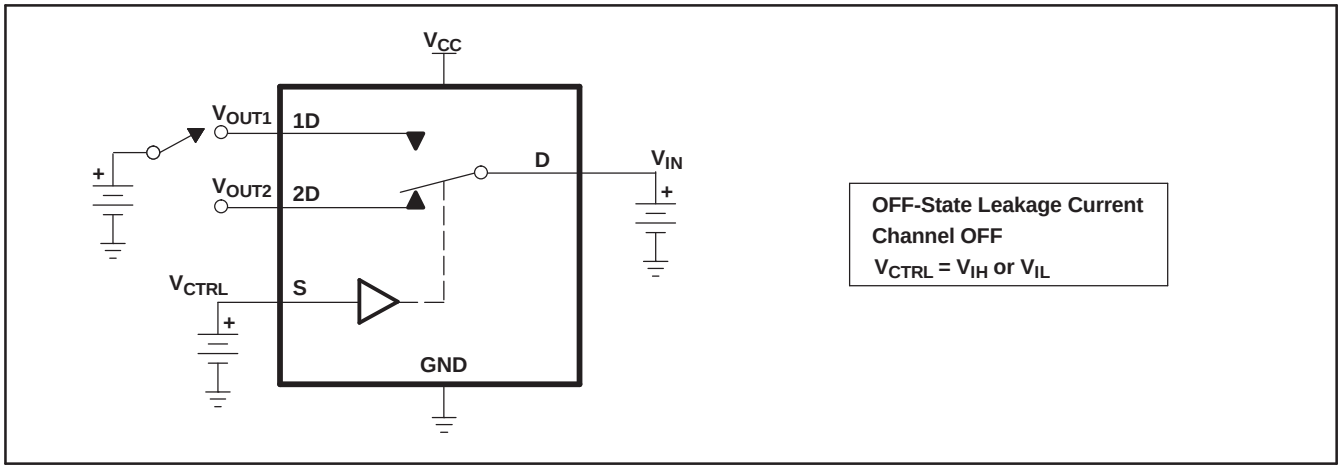



**Figure 13. OFF-State Leakage Current**

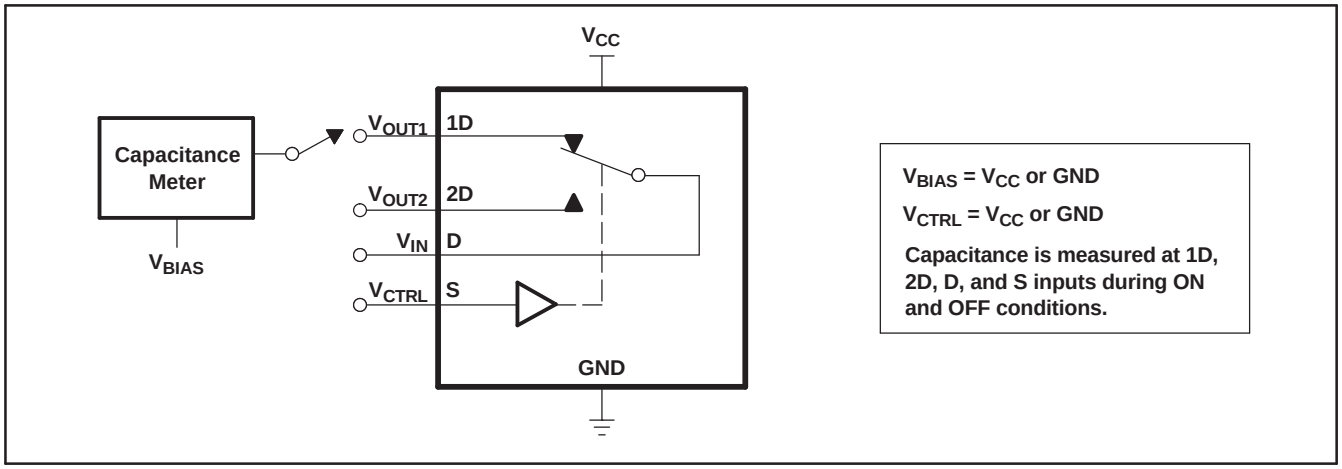



**Figure 14. Capacitance**

# 9 Detailed Description

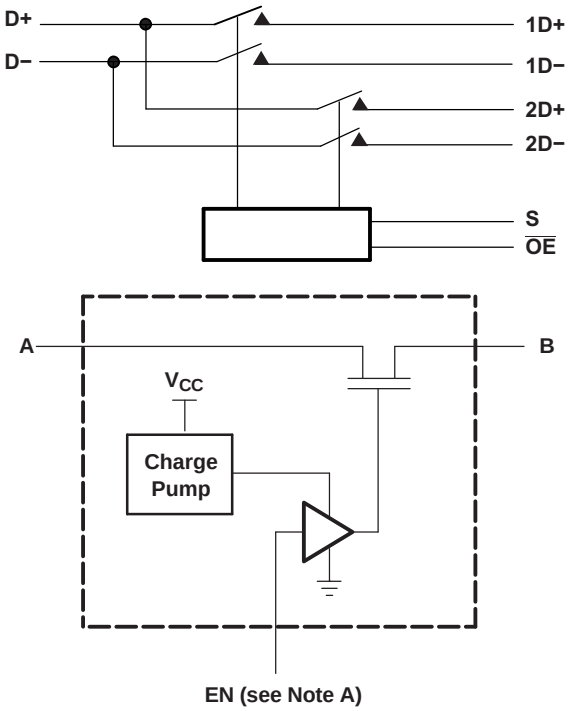
## 9.1 Overview

The TS3USB221A device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (900 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that will reduce the power consumption to 1 µA for portible applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221A device integrates ESD protection cells on all pins, is available in a tiny µQFN package (2 mm × 1.5 mm) and is characterized over the free air temperature range from –40°C to 85°C.

## 9.2 Functional Block Diagram




A. EN is the internal enable signal applied to the switch.

**Figure 15. Simplified Schematic of Each FET Switch (SW)**

## 9.1 Feature Description

### 9.1.1 Low Power Mode

The TS3USB221A has a low power mode that reduces the power consumption to 1 µA while the devices is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{OE}$ must be supplied with a logic "High" signal.

## 9.2 Device Functional Modes

**Table 1. Truth Table**

| S | $\overline{OE}$ | FUNCTION |
|---|---|---|
| X | H | Disconnect |
| L | L | D = 1D |
| H | L | D = 2D |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221A solution can effectively expand the limited USB I/Os by switching between multiple USB buses in order to interface them to a single USB hub or controller.

## 10.2 Typical Application

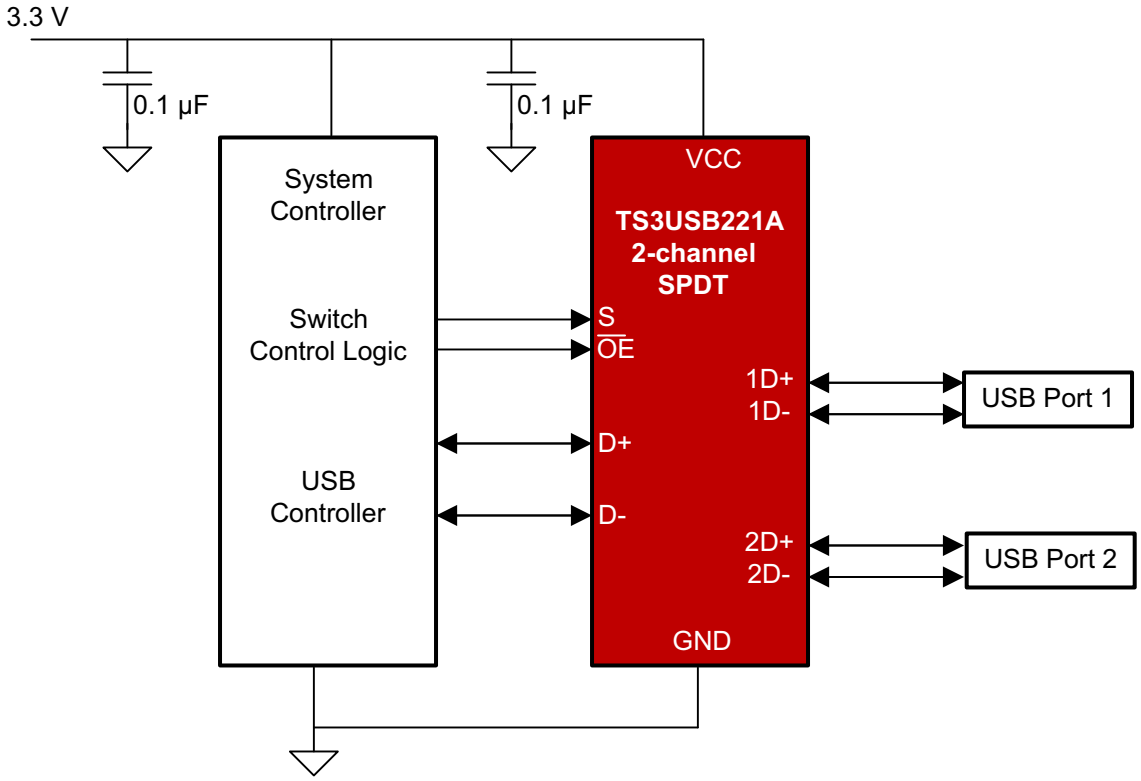



**Figure 16. Application Schematic**

## Typical Application (continued)

### 10.2.1 Design Requirements

Design requirements of the USB 1.0,1.1, and 2.0 standards should be followed.

It is recommended that the digital control pins S and $\overline{OE}$ be pulled up to $V_{CC}$ or down to GND to avoid undesired switch positions that could result from the floating pin.

### 10.2.2 Detailed Design Procedure

The TS3USB221A can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

### 10.2.3 Application Curves

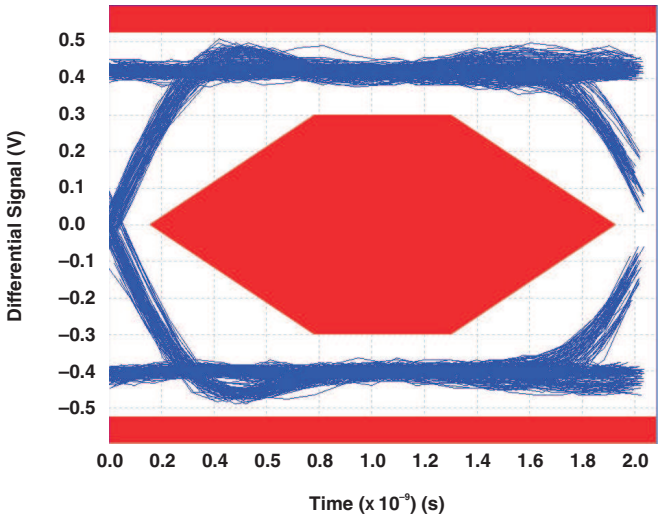



**Figure 17. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)**

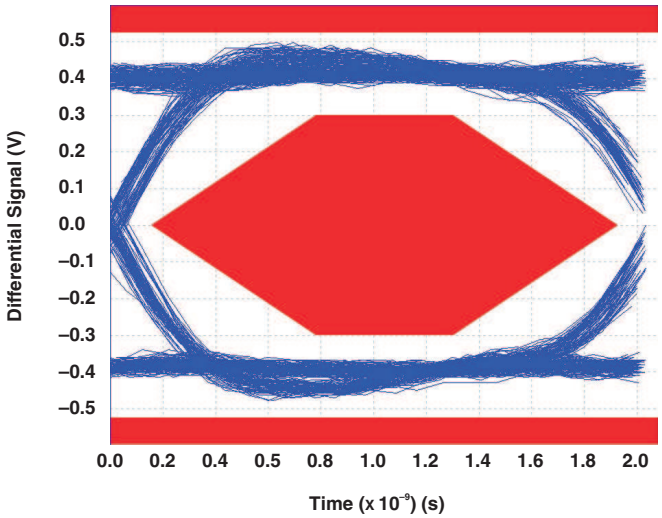



**Figure 18. Eye Pattern: 480-Mbps USB Signal With Switch NC Path**

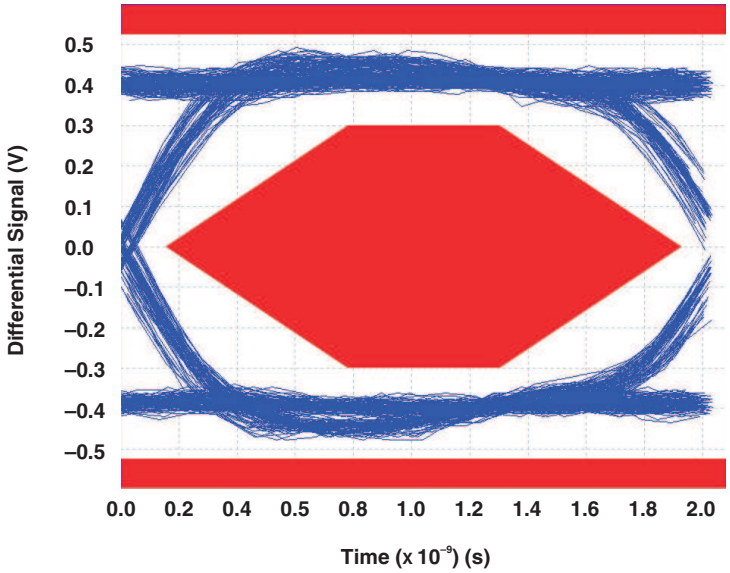



**Figure 19. Eye Pattern: 480-Mbps USB Signal With Switch NO Path**

# 11 Power Supply Recommendations

Power to the device is supplied through the VCC pin and should follow the USB 1.0, 1.1, and 2.0 standards. A bypass capacitor is recommended to be placed as close to the supply pin VCC to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

# 12 Layout

## 12.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D+/D- traces.

The high speed D+/D- traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D- traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 20.

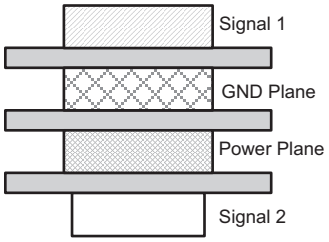



**Figure 20. Four-Layer Board Stack-Up**

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

## 12.2 Layout Example

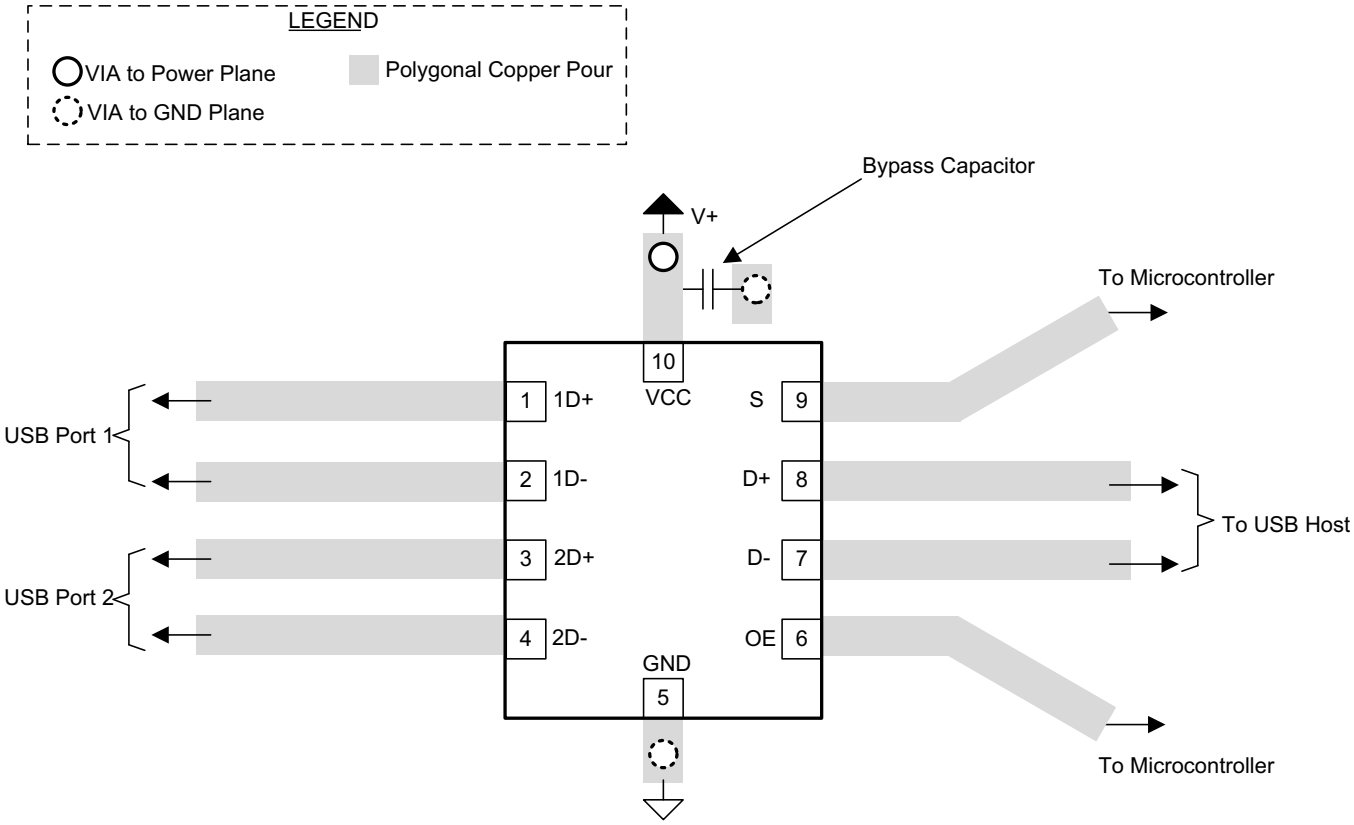



**Figure 21. Package Layout Diagram**

# 13 Device and Documentation Support

## 13.1 Trademarks

All trademarks are the property of their respective owners.

## 13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS3USB221ARSER | ACTIVE | UQFN | RSE | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (LH7 ~ LHR ~ LHV) | Samples |
| TS3USB221ARSERG4 | ACTIVE | UQFN | RSE | 10 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (LH7 ~ LHR ~ LHV) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TS3USB221A :**

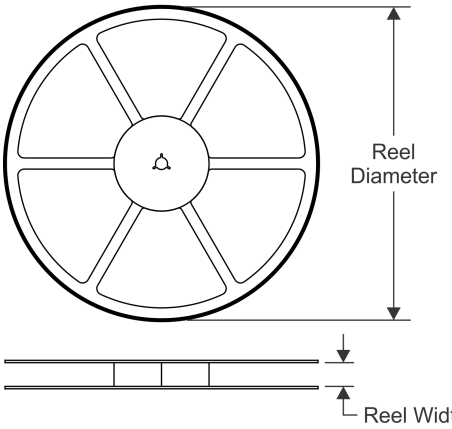
- Automotive: TS3USB221A-Q1

NOTE: Qualified Version Definitions:

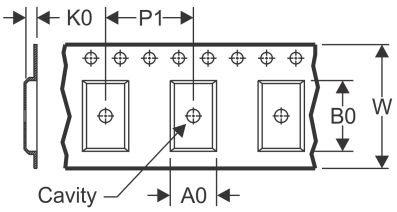
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

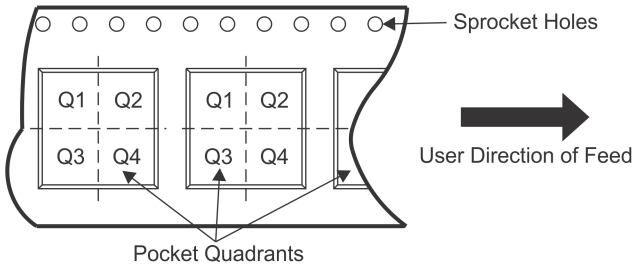



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

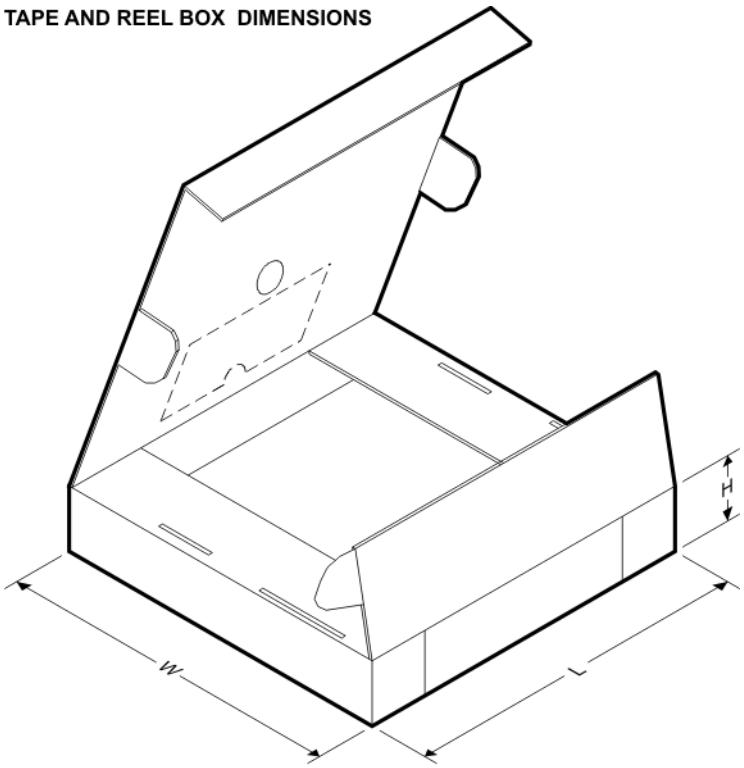
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS3USB221ARSER | UQFN | RSE | 10 | 3000 | 180.0 | 9.5 | 1.7 | 2.3 | 0.75 | 4.0 | 8.0 | Q1 |
| TS3USB221ARSER | UQFN | RSE | 10 | 3000 | 180.0 | 9.5 | 1.7 | 2.2 | 0.75 | 4.0 | 8.0 | Q1 |
| TS3USB221ARSER | UQFN | RSE | 10 | 3000 | 180.0 | 8.4 | 1.68 | 2.13 | 0.76 | 4.0 | 8.0 | Q1 |

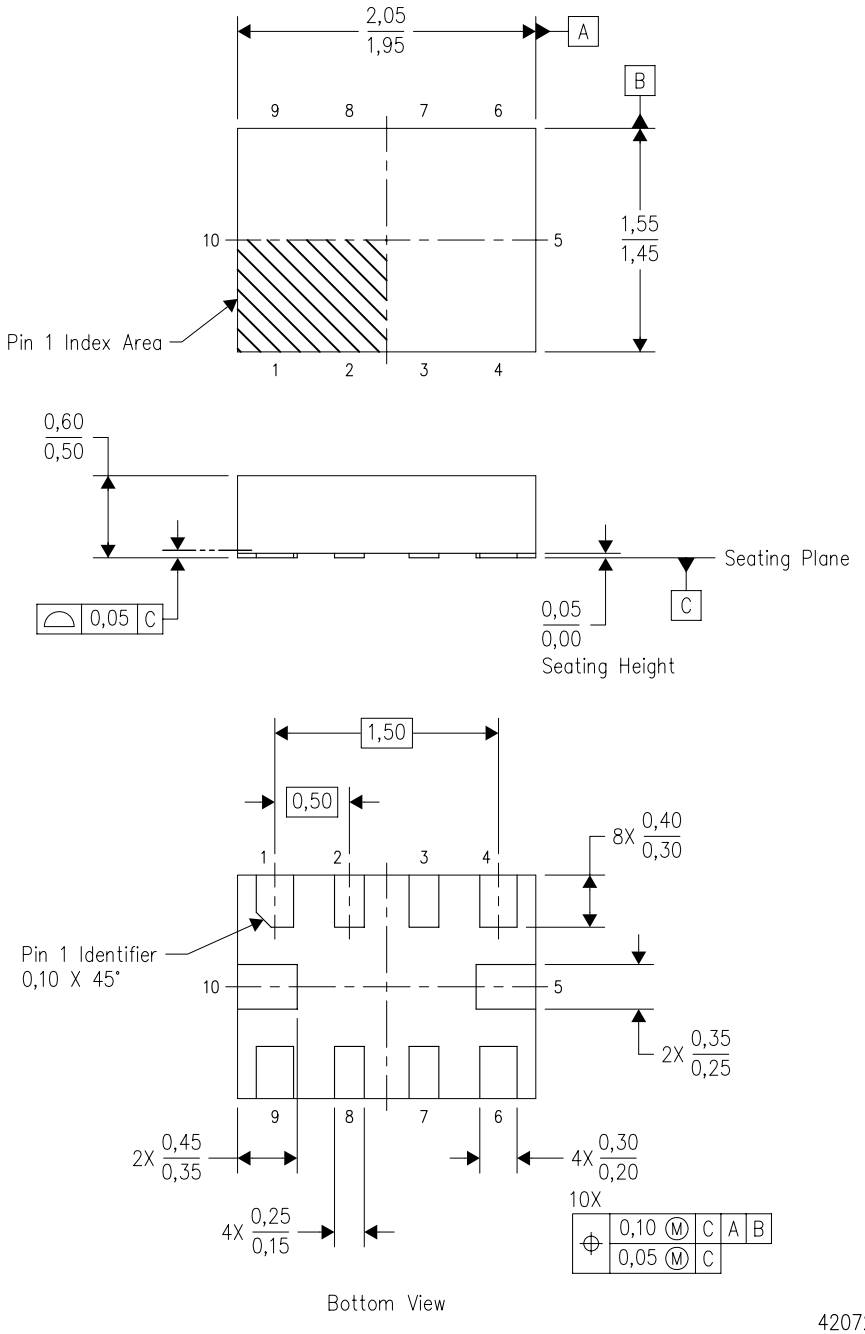
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS3USB221ARSER | UQFN | RSE | 10 | 3000 | 184.0 | 184.0 | 19.0 |
| TS3USB221ARSER | UQFN | RSE | 10 | 3000 | 189.0 | 185.0 | 36.0 |
| TS3USB221ARSER | UQFN | RSE | 10 | 3000 | 202.0 | 201.0 | 28.0 |

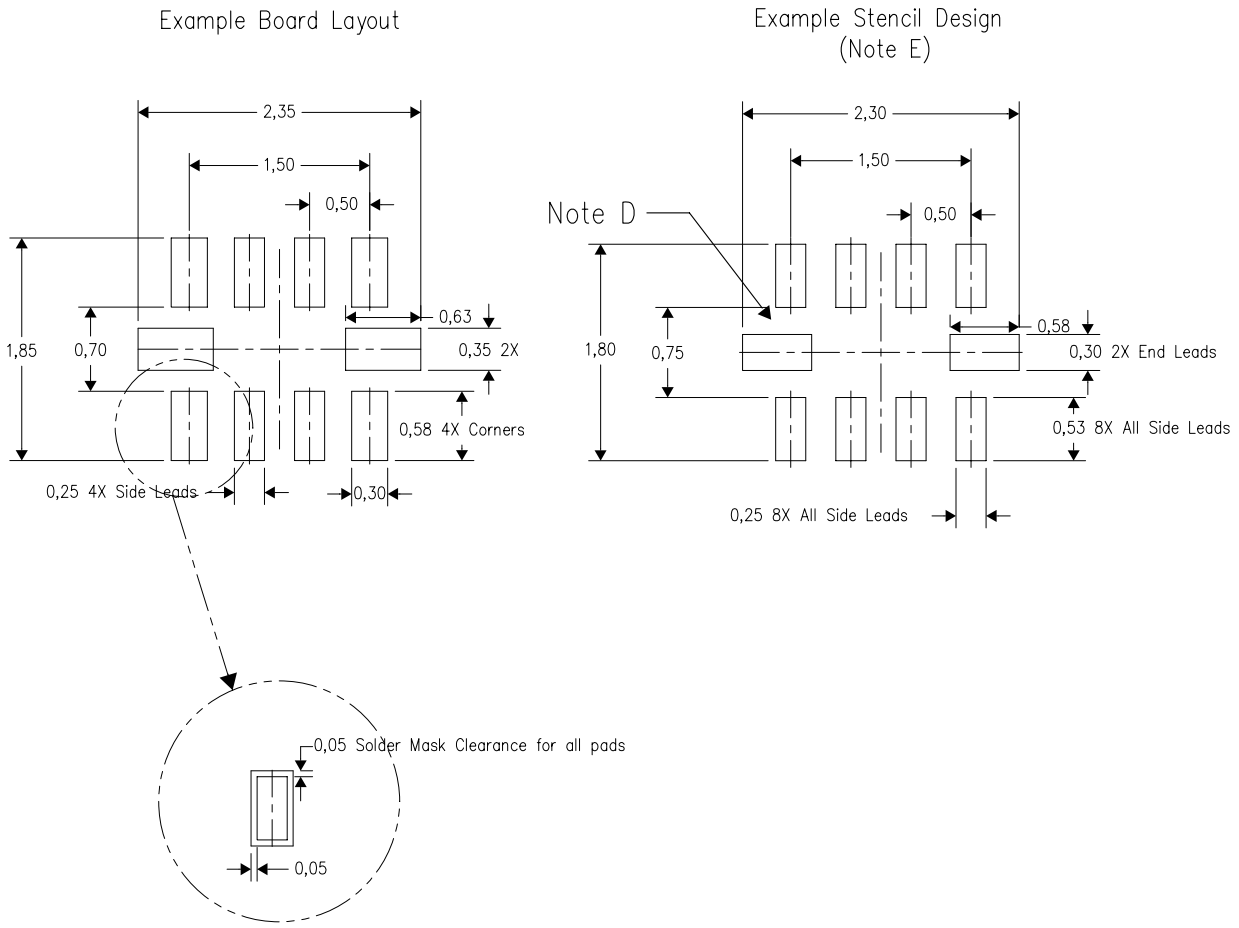
RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




4207268–3/D 01/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UEFD.

RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD




4208106–3/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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