

## Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

### FEATURES AND BENEFITS

- Accurate power monitoring for AC and DC applications
- UL 60950-1 (ed. 2) and UL 62368-1 (ed. 1) certified for reinforced isolation up to 517 V<sub>RMS</sub> in a single package
- Accurate measurements of active, reactive, and apparent power, as well as power factor
- Separate RMS and instantaneous measurements for both voltage and current channels
- Two programmable averaging blocks
- 0.85 mΩ primary conductor resistance for low power loss and high inrush current withstand capability
- Compatible with floating and non-floating GND
- Dedicated voltage or current zero crossing pin
- Fast, user-programmable overcurrent fault pin (5 μs typ.)
- User-programmable undervoltage and overvoltage RMS thresholds
- 1 kHz bandwidth
- Current sensing range up to 90 A
- Options for I<sup>2</sup>C or SPI digital interface protocols

### DESCRIPTION

The Allegro ACS37800 power monitoring IC greatly simplifies the addition of power monitoring to many AC or DC powered systems. The sensor may be powered from the same supply as the system's MCU, eliminating the need for multiple power supplies. The device's construction includes a copper conduction path that generates a magnetic field proportional to applied current. The magnetic field is sensed differentially to reject errors introduced by common mode fields.

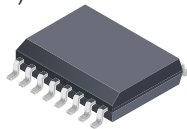
Allegro's Hall-effect-based, galvanically isolated current sensing technology achieves reinforced isolation ratings (4800 V<sub>RMS</sub>) in a small PCB footprint. These features enable isolated current sensing without expensive Rogowski coils, oversized current transformers, isolated operational amplifiers, or the power loss of shunt resistors.

The ACS37800 power monitoring IC offers key power measurement parameters that can easily be accessed through its SPI or I<sup>2</sup>C digital protocol interfaces. Dedicated and configurable I/O pins for voltage/current zero crossing, undervoltage and overvoltage reporting, and fast overcurrent fault detection are available in I<sup>2</sup>C mode. User configuration of the IC is available through on-chip EEPROM.

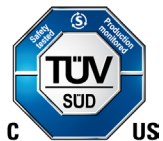
The ACS37800 is provided in a small low-profile surface mount SOIC16 wide-body package, is lead (Pb) free, and is fully calibrated prior to shipment from the Allegro factory. Customer calibration can further increase accuracy in application.

### PACKAGE

16-pin SOICW (suffix MA)



Not to scale



CB Certificate Number:  
US-32210-M1-UL  
US-36315-UL

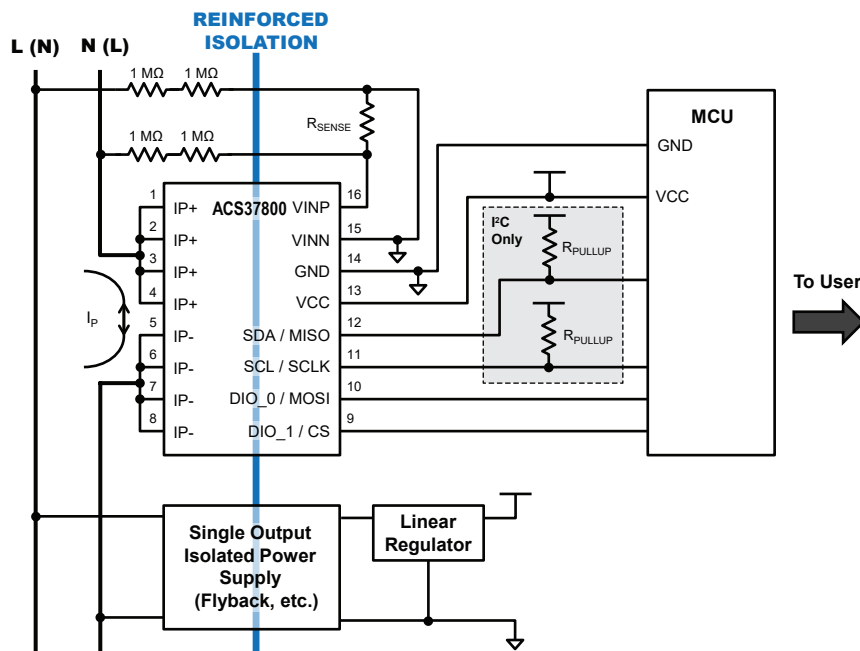


Figure 1: Typical Application

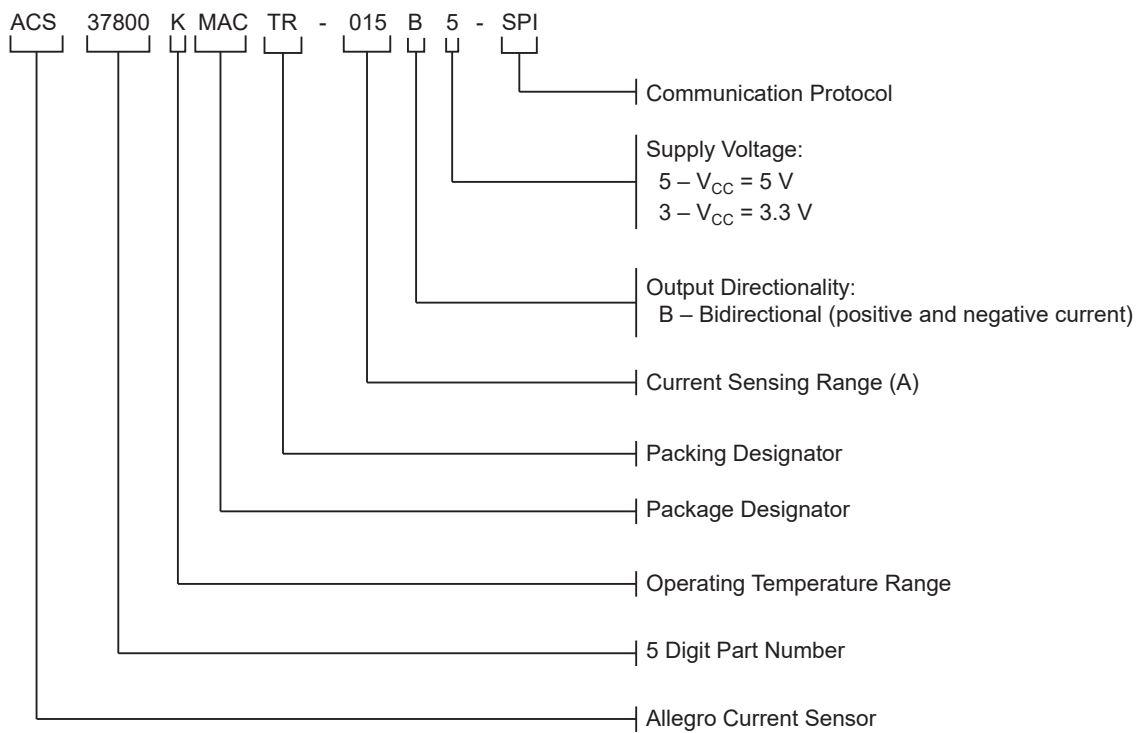
# ACS37800

## Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

### SELECTION GUIDE

Part Number	V <sub>CC(typ)</sub> (V)	I <sub>PR</sub> (A)	Communication Protocol	T <sub>A</sub> (°C)	Packing [1]
ACS37800KMACTR-015B5-SPI	5	±15	SPI	-40 to 125	Tape and reel, 1000 pieces per reel, 3000 pieces per box
ACS37800KMACTR-030B3-SPI	3.3	±30			
ACS37800KMACTR-030B3-I2C	3.3	±30	I2C		
ACS37800KMACTR-090B3-I2C	3.3	±90			

[1] Contact Allegro for additional packing options.



### ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	$V_{CC}$		6.5	V
Reverse Supply Voltage	$V_{RCC}$		-0.5	V
Input Voltage	$V_{INP}, V_{INN}$		$V_{CC} + 0.5$	V
Reverse Input Voltage	$V_{RNP}, V_{RNN}$		-0.5	V
Digital I/O Voltage	$V_{DIO}$	SPI, I <sup>2</sup> C, and general purpose I/O	6	V
Reverse Digital I/O Voltage	$V_{RDIO}$		-0.5	V
Maximum Continuous Current	$I_{CMAX}$	$T_A = 25^{\circ}C$	60	A
Operating Ambient Temperature	$T_A$	Range K	-40 to 125	$^{\circ}C$
Junction Temperature	$T_{J(max)}$		165	$^{\circ}C$
Storage Temperature	$T_{stg}$		-65 to 170	$^{\circ}C$

### ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage	$V_{ISO}$	Agency type-tested for 60 seconds per UL 60950-1 (edition 2) and UL 62368-1 (edition 1); Production tested at 3000 $V_{RMS}$ for 1 second, in accordance with UL 60950-1 (edition 2) and UL 62368-1 (edition 1)	4800	$V_{RMS}$
Working Voltage for Basic Isolation	$V_{WVBI}$	Maximum approved working voltage for basic (single) isolation according to UL 60950-1 (edition 2) and UL 62368-1 (edition 1)	1480	$V_{PK}$ or VDC
			1047	$V_{RMS}$
Working Voltage for Reinforced Isolation	$V_{WVRI}$	Maximum approved working voltage for reinforced isolation according to UL 60950-1 (edition 2) and UL 62368-1 (edition 1)	730	$V_{PK}$ or VDC
			517	$V_{RMS}$
Clearance	$D_{cl}$	Minimum distance through air from IP leads to signal leads	7.5	mm
Creepage	$D_{cr}$	Minimum distance along package body from IP leads to signal leads	7.9	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	90	$\mu m$
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

### ESD RATINGS

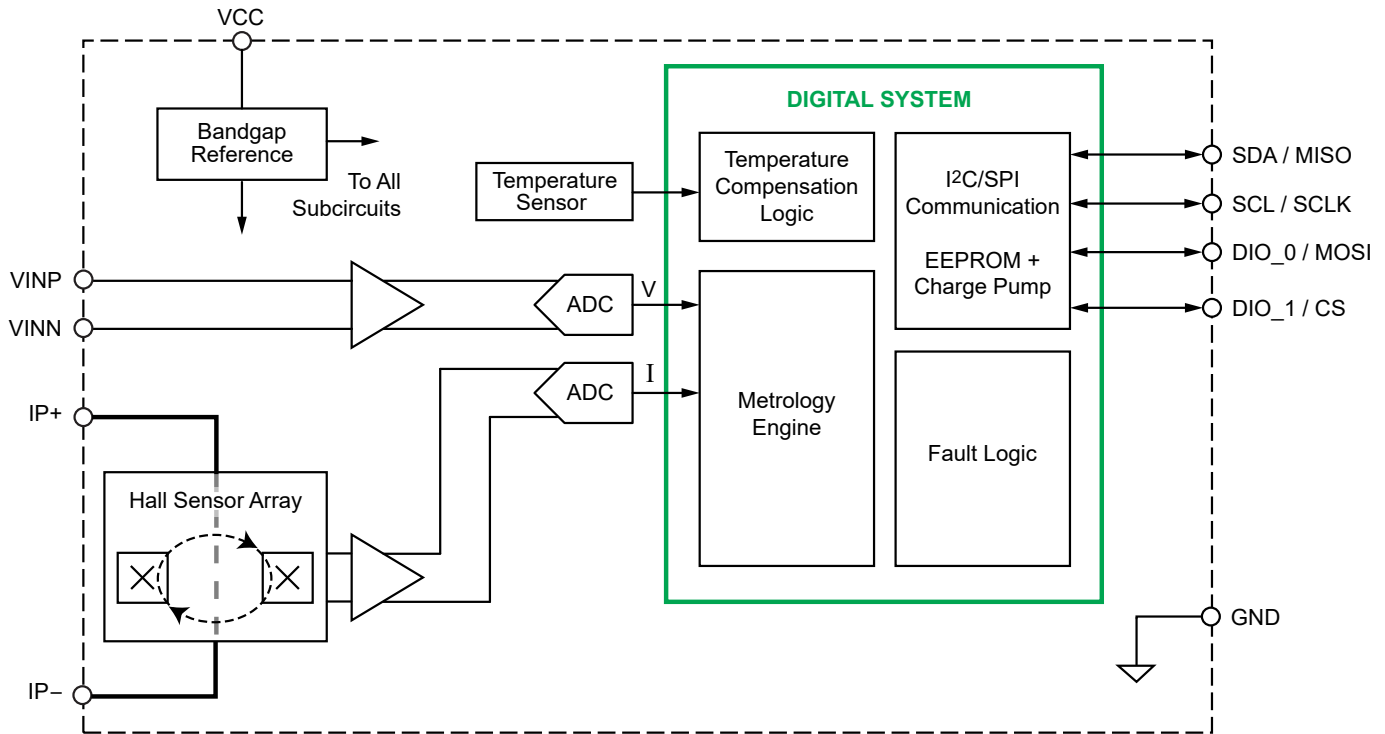
Characteristic	Symbol	Notes	Value	Unit
Human Body Model	$V_{HBM}$	Per JEDEC JS-001	$\pm 5$	kV
Charged Device Model	$V_{CDM}$	Per JEDEC JS-002	$\pm 1$	kV

### THERMAL CHARACTERISTICS

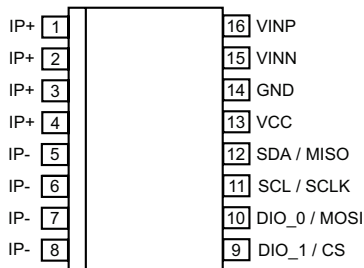
Characteristic	Symbol	Test Conditions [1]	Value	Units
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the Allegro ASEK37800 evaluation board with 750 mm <sup>2</sup> of 4 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB.	23	$^{\circ}C/W$
Package Thermal Resistance (Junction to Lead)	$R_{\theta JL}$	Mounted on the Allegro ACS37800 evaluation board.	5	$^{\circ}C/W$

[1] Refer to the Thermal Performance section below.

### FUNCTIONAL BLOCK DIAGRAM



### PINOUT DIAGRAM AND TERMINAL LIST



Pinout Diagram

Terminal List Table

Number	Name	Description	
		I2C	SPI
1, 2, 3, 4	IP+	Terminals for current being sensed; fused internally	
5, 6, 7, 8	IP-	Terminals for current being sensed; fused internally	
9	DIO_1 / CS	Digital I/O 1	Chip Select (CS)
10	DIO_0 / MOSI	Digital I/O 0	MOSI
11	SCL / SCLK	SCL	SCLK
12	SDA / MISO	SDA	MISO
13	VCC	Device power supply terminal	
14	GND	Device ground terminal	
15	VINN	Negative input voltage (always connect to GND)	
16	VINP	Positive input voltage	

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# ACS37800

## Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

**COMMON ELECTRICAL CHARACTERISTICS** [1]: Valid through the full range of  $T_A$  and  $V_{CC} = V_{CC(typ)}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>ELECTRICAL CHARACTERISTICS</b>						
Supply Voltage	$V_{CC}$	5 V variant	4.5	5	5.5	V
		3.3 V variant	2.97	3.3	3.63	V
Supply Current	$I_{CC}$	$V_{CC(min)} \leq V_{CC} \leq V_{CC(max)}$ , no load on output pins	–	12	15	mA
Supply Bypass Capacitor	$C_{BYPASS}$	$V_{CC}$ to GND recommended	0.1	–	–	mA
Power-On Time	$t_{PO}$		–	90	–	$\mu$ s
<b>VOLTAGE INPUT BUFFER</b>						
Differential Input Range	$\Delta V_{INR}$	$\Delta V_{IN} = V_{INP} - V_{INN(GND)}$	–250	–	250	mV
Dynamic Input Frequency	$f_{dyn\_in}$	<i>bypass_n_en</i> = 0	35	–	300	Hz
<b>VOLTAGE CHANNEL ADC</b>						
Sample Frequency	$f_{S\_V}$		–	32	–	kHz
Number of Bits	$ADC_{V\_B}$		–	16	–	bits
ADC Fullscale	$ADC_{V\_FS}$	$\Delta V_{IN} = \pm 250$ mV, $V_{INN} = GND$	–27500	–	27500	codes
Sensitivity	$Sens_{(V)}$	$\Delta V_{INR(min)} < \Delta V_{IN} < \Delta V_{INR(max)}$	–	110	–	LSB / mV
Voltage Channel Power Supply Error	$PSE_{V\_O}$	Ratio of change on $V_{CC}$ to change in offset at DC, 100% $\pm 10\%$ $V_{CC(typ)}$	–7	–	7	codes / % $V_{CC}$
	$PSE_{V\_S}$	Ratio of change on $V_{CC}$ to change in sensitivity at DC, 100% $\pm 10\%$ $V_{CC(typ)}$	–0.1	–	0.1	% / % $V_{CC}$
Voltage Channel Power Supply Rejection Ratio	$PSRR_{V\_O}$	Ratio of change on $V_{CC}$ to change in offset, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	60	70	–	dB
	$PSRR_{V\_S}$	Ratio of change on $V_{CC}$ to change in sensitivity, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	60	75	–	dB
<b>VOLTAGE CHANNEL</b>						
Internal Bandwidth	BW		–	1	–	kHz
RMS Noise	$N_V$	Input referred	–	$\pm 0.3$	–	mV
Linearity Error	$E_{LIN\_V}$		–	$\pm 0.2$	–	%
<b>CURRENT CHANNEL</b>						
Sample Frequency	$f_{S\_C}$		–	32	–	kHz
Number of Bits	$ADC_{I\_B}$		–	16	–	bits
ADC Fullscale	$ADC_{I\_FS}$	$I_P = I_{PR(min)}$ or $I_{PR(max)}$	–27500	–	27500	codes
Current Channel Power Supply Error	$PSE_{I\_O}$	Ratio of change on $V_{CC}$ to change in offset at DC, 100% $\pm 10\%$ $V_{CC(nom)}$	–60	–	60	codes / % $V_{CC}$
	$PSE_{I\_S}$	Ratio of change on $V_{CC}$ to change in sensitivity at DC, 100% $\pm 10\%$ $V_{CC(nom)}$	–0.3	–	0.3	% / % $V_{CC}$
Current Channel Power Supply Rejection Ratio	$PSRR_{I\_O}$	Ratio of change on $V_{CC}$ to change in offset, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	60	65	–	dB
	$PSRR_{I\_S}$	Ratio of change on $V_{CC}$ to change in sensitivity, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	20	40	–	dB
Internal Bandwidth	BW		–	1	–	kHz
Primary Conductor Resistance	$R_{IP}$	$T_A = 25^\circ C$	–	0.85	–	m $\Omega$

Continued on next page...

**COMMON ELECTRICAL CHARACTERISTICS [1] (continued):** Valid through the full range of  $T_A$  and  $V_{CC} = V_{CC(typ)}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>CURRENT CHANNEL (continued)</b>						
RMS Noise	$N_I$	Input referred	–	±0.1	–	A
Linearity Error	$E_{LIN_I}$		–	±1.5	–	%
<b>OVERCURRENT FAULT CHARACTERISTICS</b>						
Fault Response Time	$t_{RF}$	Time from $I_P$ rising above $I_{FAULT}$ until $V_{FAULT} < V_{FAULT(max)}$ for a current step from 0 to $1.2 \times I_{FAULT}$ ; 10 k $\Omega$ and 100 pF from DIO_1 to ground; $ftdly = 0$	–	5	–	$\mu s$
Internal Bandwidth	BW		–	200	–	kHz
Fault Hysteresis [2]	$I_{HYST}$		–	$0.06 \times FS$	–	A
Fault Range	$I_{FAULT}$	Set using <i>fault</i> field in EEPROM	$0.65 \times FS$	–	$2.00 \times FS$	A
<b>VOLTAGE ZERO CROSSING</b>						
Voltage Zero-Crossing Delay	$t_d$		–	250	–	$\mu s$
<b>DIO PINS</b>						
DIO Output High Level	$V_{OH(DIO)}$	$V_{CC} = 3.3 V$	3	–	–	V
DIO Output Low Level	$V_{OL(DIO)}$	$V_{CC} = 3.3 V$	–	–	0.3	V
DIO Input Voltage for Address Selection 0	$V_{ADD0}$	$V_{CC} = 3.3 V$	–	0	–	V
DIO Input Voltage for Address Selection 1	$V_{ADD1}$	$V_{CC} = 3.3 V$	–	1.1	–	V
DIO Input Voltage for Address Selection 2	$V_{ADD2}$	$V_{CC} = 3.3 V$	–	2.2	–	V
DIO Input Voltage for Address Selection 3	$V_{ADD3}$	$V_{CC} = 3.3 V$	–	3.3	–	V

[1] Device may be operated at higher primary current levels ( $I_P$ ), ambient temperatures ( $T_A$ ), and internal leadframe temperatures, provided that the maximum junction temperature ( $T_{J(max)}$ ) is not exceeded.

[2] After  $I_P$  goes above  $I_{FAULT}$ , tripping the internal fault comparator,  $I_P$  must go below  $I_{FAULT} - I_{HYST}$  before the internal fault comparator will reset.

# ACS37800

## Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

**ACS37800KMAC-015B5 PERFORMANCE CHARACTERISTICS:** Valid through the full operating temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $C_{\text{BYPASS}} = 0.1 \mu\text{F}$ , and  $V_{\text{CC}} = 5 \text{ V}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
<b>GENERAL CHARACTERISTICS</b>						
Nominal Supply Voltage	$V_{\text{CC}(\text{typ})}$		–	5	–	V
<b>NOMINAL PERFORMANCE – FACTORY CURRENT CHANNEL</b>						
Current Sensing Range	$I_{\text{PR}}$		–15	–	15	A
Sensitivity	$\text{Sens}_{(I)}$	$I_{\text{PR}(\text{min})} < I_{\text{P}} < I_{\text{PR}(\text{max})}$	–	1833.3	–	LSB/A
<b>NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]</b>						
Active Power Sensitivity	$\text{Sens}_{\text{Pd\_act}}$		–	6.15	–	LSB/mW
Imaginary Power Sensitivity	$\text{Sens}_{\text{Pd\_img}}$		–	12.31	–	LSB/mVAR
Apparent Power Sensitivity	$\text{Sens}_{\text{Pd\_app}}$		–	12.31	–	LSB/mVA
<b>TOTAL OUTPUT ERROR COMPONENTS [3] – CURRENT CHANNEL</b>						
Sensitivity Error	$E_{\text{SENS}(I)}$	Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1.1$	–	%
		Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 1.5$	–	%
Offset Error	$E_{\text{O}(I)}$	$I_{\text{P}} = 0 \text{ A}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 720$	–	LSB
		$I_{\text{P}} = 0 \text{ A}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 780$	–	LSB
Total Output Error	$E_{\text{TOT}(I)}$	Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 2.1$	–	%
		Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 2.7$	–	%
<b>TOTAL OUTPUT ERROR COMPONENTS [3] – VOLTAGE CHANNEL</b>						
Sensitivity Error	$E_{\text{SENS}(V)}$	Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1.2$	–	%
		Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 1.2$	–	%
Offset Error	$E_{\text{O}(V)}$	$\Delta V_{\text{IN}} = 0 \text{ mV}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 55$	–	LSB
		$\Delta V_{\text{IN}} = 0 \text{ mV}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 55$	–	LSB
Total Output Error	$E_{\text{TOT}(V)}$	Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1.4$	–	%
		Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 1.4$	–	%
<b>ACCURACY PERFORMANCE – ACTIVE POWER</b>						
Total Output Error	$E_{\text{TOT}(P)}$	$I_{\text{P}} = I_{\text{PR}(\text{max})}$ , measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 2.1$	–	%
		$I_{\text{P}} = I_{\text{PR}(\text{max})}$ , measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 3$	–	%

[1] Typical values are mean  $\pm 3$  sigma.

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivities.

[3]  $E_{\text{TOT}} = E_{\text{SENS}} + 100 \times V_{\text{OE}} / (\text{Sens} \times I_{\text{P}})$



# ACS37800

## Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

**ACS37800KMAC-030B3 PERFORMANCE CHARACTERISTICS:** Valid through the full operating temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $C_{\text{BYPASS}} = 0.1 \mu\text{F}$ , and  $V_{\text{CC}} = 3.3 \text{ V}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
<b>GENERAL CHARACTERISTICS</b>						
Nominal Supply Voltage	$V_{\text{CC}(\text{typ})}$		–	3.3	–	V
<b>NOMINAL PERFORMANCE – CURRENT CHANNEL</b>						
Current Sensing Range	$I_{\text{PR}}$		–30	–	30	A
Sensitivity	$\text{Sens}_{(I)}$	$I_{\text{PR}(\text{min})} < I_{\text{P}} < I_{\text{PR}(\text{max})}$	–	916.7	–	LSB/A
<b>NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]</b>						
Active Power Sensitivity	$\text{Sens}_{\text{Pd}_{\text{act}}}$		–	3.08	–	LSB/mW
Imaginary Power Sensitivity	$\text{Sens}_{\text{Pd}_{\text{img}}}$		–	6.15	–	LSB/mVAR
Apparent Power Sensitivity	$\text{Sens}_{\text{Pd}_{\text{app}}}$		–	6.15	–	LSB/mVA
<b>TOTAL OUTPUT ERROR COMPONENTS [3] – CURRENT CHANNEL</b>						
Sensitivity Error	$E_{\text{SENS}(I)}$	Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1$	–	%
		Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 1.5$	–	%
Offset Error	$E_{\text{O}(I)}$	$I_{\text{P}} = 0 \text{ A}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 510$	–	LSB
		$I_{\text{P}} = 0 \text{ A}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 570$	–	LSB
Total Output Error	$E_{\text{TOT}(I)}$	Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 2$	–	%
		Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 2.7$	–	%
<b>TOTAL OUTPUT ERROR COMPONENTS [3] – VOLTAGE CHANNEL</b>						
Sensitivity Error	$E_{\text{SENS}(V)}$	Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 0.75$	–	%
		Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 0.75$	–	%
Offset Error	$E_{\text{O}(V)}$	$\Delta V_{\text{IN}} = 0 \text{ mV}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 55$	–	LSB
		$\Delta V_{\text{IN}} = 0 \text{ mV}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 55$	–	LSB
Total Output Error	$E_{\text{TOT}(V)}$	Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1$	–	%
		Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 1$	–	%
<b>ACCURACY PERFORMANCE – ACTIVE POWER</b>						
Total Output Error	$E_{\text{TOT}(P)}$	$I_{\text{P}} = I_{\text{PR}(\text{max})}$ , measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 2.1$	–	%
		$I_{\text{P}} = I_{\text{PR}(\text{max})}$ , measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 3$	–	%

[1] Typical values are mean  $\pm 3$  sigma.

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivities.

[3]  $E_{\text{TOT}} = E_{\text{SENS}} + 100 \times V_{\text{OE}} / (\text{Sens} \times I_{\text{P}})$

# ACS37800

## Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

**ACS37800KMAC-090B3 PERFORMANCE CHARACTERISTICS:** Valid through the full operating temperature range,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $C_{\text{BYPASS}} = 0.1 \mu\text{F}$ , and  $V_{\text{CC}} = 3.3 \text{ V}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
<b>GENERAL CHARACTERISTICS</b>						
Nominal Supply Voltage	$V_{\text{CC}(\text{typ})}$		–	3.3	–	V
<b>NOMINAL PERFORMANCE – CURRENT CHANNEL</b>						
Current Sensing Range	$I_{\text{PR}}$		–90	–	90	A
Sensitivity	$\text{Sens}_{(I)}$	$I_{\text{PR}(\text{min})} < I_{\text{P}} < I_{\text{PR}(\text{max})}$	–	305.6	–	LSB/A
<b>NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]</b>						
Active Power Sensitivity	$\text{Sens}_{\text{Pd}_{\text{act}}}$		–	1.03	–	LSB/mW
Imaginary Power Sensitivity	$\text{Sens}_{\text{Pd}_{\text{img}}}$		–	2.05	–	LSB/mVAR
Apparent Power Sensitivity	$\text{Sens}_{\text{Pd}_{\text{app}}}$		–	2.05	–	LSB/mVA
<b>TOTAL OUTPUT ERROR COMPONENTS [3] – CURRENT CHANNEL</b>						
Sensitivity Error	$E_{\text{SENS}(I)}$	Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1$	–	%
		Measured at $I_{\text{P}} = I_{\text{PR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 1.5$	–	%
Offset Error	$E_{\text{O}(I)}$	$I_{\text{P}} = 0 \text{ A}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 180$	–	LSB
		$I_{\text{P}} = 0 \text{ A}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 210$	–	LSB
Total Output Error	$E_{\text{TOT}(I)}$	Measured at $I_{\text{P}} = 45 \text{ A}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 2$	–	%
		Measured at $I_{\text{P}} = 45 \text{ A}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 2.6$	–	%
<b>TOTAL OUTPUT ERROR COMPONENTS [3] – VOLTAGE CHANNEL</b>						
Sensitivity Error	$E_{\text{SENS}(V)}$	Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 0.75$	–	%
		Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 0.75$	–	%
Offset Error	$E_{\text{O}(V)}$	$\Delta V_{\text{IN}} = 0 \text{ mV}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 55$	–	LSB
		$\Delta V_{\text{IN}} = 0 \text{ mV}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 55$	–	LSB
Total Output Error	$E_{\text{TOT}(V)}$	Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1$	–	%
		Measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 1$	–	%
<b>ACCURACY PERFORMANCE – ACTIVE POWER</b>						
Total Output Error	$E_{\text{TOT}(P)}$	$I_{\text{P}} = 45 \text{ A}$ , measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$	–	$\pm 1.3$	–	%
		$I_{\text{P}} = 45 \text{ A}$ , measured at $\Delta V_{\text{IN}} = \Delta V_{\text{INR}(\text{max})}$ , $T_A = -40^\circ\text{C}$ to $25^\circ\text{C}$	–	$\pm 2.1$	–	%

[1] Typical values are mean  $\pm 3$  sigma.

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivities.

[3]  $E_{\text{TOT}} = E_{\text{SENS}} + 100 \times V_{\text{OE}} / (\text{Sens} \times I_{\text{P}})$

**xKMACTR-I2C OPERATING CHARACTERISTICS** [1]: Valid through the full range of  $T_A$ ,  $V_{CC} = V_{CC(typ)}$ ,  $R_{EXT} = 10\text{ k}\Omega$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>I<sup>2</sup>C INTERFACE CHARACTERISTICS</b> [2]						
Bus Free Time Between Stop and Start	$t_{BUF}$		1.3	–	–	$\mu\text{s}$
Hold Time Start Condition	$t_{hdSTA}$		0.6	–	–	$\mu\text{s}$
Setup Time for Repeated Start Condition	$t_{suSTA}$		0.6	–	–	$\mu\text{s}$
SCL Low Time	$t_{LOW}$		1.3	–	–	$\mu\text{s}$
SCL High Time	$t_{HIGH}$		0.6	–	–	$\mu\text{s}$
Data Setup Time	$t_{suDAT}$		100	–	–	$\mu\text{s}$
Data Hold Time	$t_{hdDAT}$		0	–	900	$\mu\text{s}$
Setup Time for Stop Condition	$t_{suSTO}$		0.6	–	–	$\mu\text{s}$
Logic Input Low Level (SDA, SCL pins)	$V_{IL}$		–	–	30	$\%V_{CC}$
Logic Input High Level (SDA, SCL pins)	$V_{IH}$		70	–	–	$\%V_{CC}$
Logic Input Current	$I_{IN}$	Input voltage on SDA or SCL = 0 V to $V_{CC}$	–1	–	1	$\mu\text{A}$
Output Low Voltage (SDA)	$V_{OL}$	SDA sinking = 1.5 mA	–	–	0.36	V
Clock Frequency (SCL pin)	$f_{CLK}$		–	–	400	kHz
Output Fall Time (SDA pin)	$t_f$	$R_{EXT} = 2.4\text{ k}\Omega$ , $C_B = 100\text{ pF}$	–	–	250	ns
I <sup>2</sup> C Pull-Up Resistance	$R_{EXT}$		2.4	10	–	k $\Omega$
Total Capacitive Load for Each of SDA and SCL Buses	$C_B$		–	–	20	pF

[1] Validated by characterization and design.

[2] These values are ratiometric to the supply voltage. I<sup>2</sup>C Interface Characteristics are ensured by design and not factory tested.

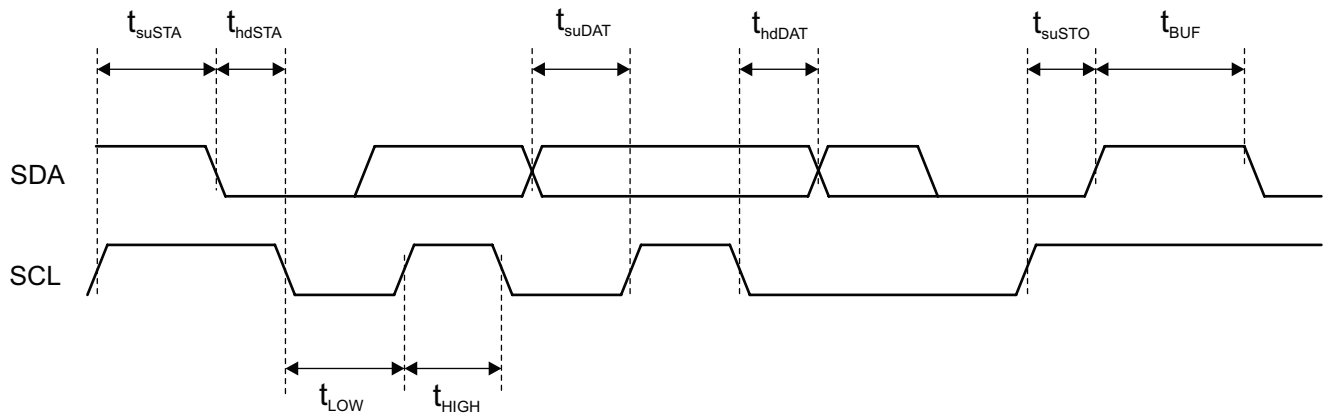


Figure 2: I<sup>2</sup>C Interface Timing

**xKMATR-SPI OPERATING CHARACTERISTICS** [1]: Valid through the full range of  $T_A$ ,  $V_{CC} = V_{CC(typ)}$ , unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>SPI INTERFACE CHARACTERISTICS</b>						
Digital Input High Voltage	$V_{IH}$	MOSI, SCLK, CS pins, $V_{CC} = 3.3\text{ V}$	2.8	–	3.63	V
		MOSI, SCLK, CS pins, $V_{CC} = 5\text{ V}$	4	–	5.5	V
Digital Input Low Voltage	$V_{IL}$	MOSI, SCLK, CS pins	–	–	0.5	V
SPI Output High Voltage	$V_{OH}$	MISO pin, $C_L = 20\text{ pF}$ , $T_A = 25^\circ\text{C}$ , $V_{CC(typ)} = 3.3\text{ V}$	2.8	3.3	3.8	V
		MISO pin, $C_L = 20\text{ pF}$ , $T_A = 25^\circ\text{C}$ , $V_{CC(typ)} = 5\text{ V}$	4	5	5.5	V
SPI Output Low Voltage	$V_{OL}$	MISO pin, $C_L = 20\text{ pF}$ , $T_A = 25^\circ\text{C}$	–	0.3	0.5	V
SPI Clock Frequency	$f_{SCLK}$	MISO pin, $C_L = 20\text{ pF}$	0.1	–	10	MHz
SPI Frame Rate	$t_{SPI}$		5.8	–	588	kHz
Chip Select to First SCLK Edge	$t_{CS}$	Time from CS going low to SCLK falling edge	50	–	–	ns
Data Output Valid Time	$t_{DAV}$	Data output valid after SCLK falling edge	–	40	–	ns
MOSI Setup Time	$t_{SU}$	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	$t_{HD}$	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time	$t_{CHD}$	Hold SCLK high time before CS rising edge	5	–	–	ns
Load Capacitance	$C_L$	Loading on digital output (MISO) pin	–	–	20	pF

[1] Validated by characterization and design.

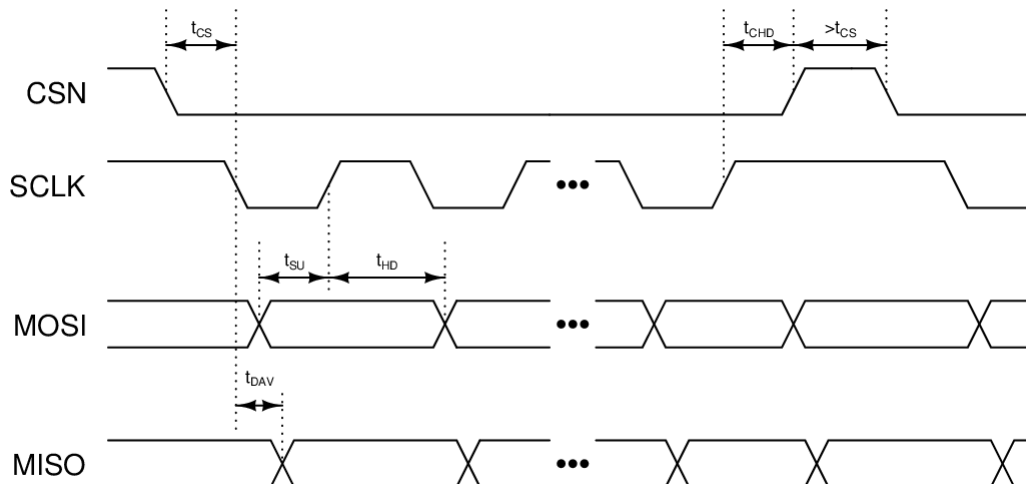


Figure 3: SPI Timing

## THEORY OF OPERATION

### Introduction

The ACS37800 provides a simple solution for voltage, current, and power monitoring in 60 Hz AC and DC applications and is particularly well suited for high isolation. The voltage is measured by resistor dividing it down to fit the input range of the on-board voltage sense amplifier, as well as to add isolation. The current is measured using the integrated current loop and galvanically isolated Hall sensor. Both analog signals are then sampled using high accuracy ADCs before entering the digital system. Here, the metrology engine is used to determine frequency, calculate RMS values of current, voltage, and power, as well as provide a range of averaging and configuration options. One can choose to read out all the different information provided using SPI or I<sup>2</sup>C. When using I<sup>2</sup>C, there are also options for using some of the digital I/O pins for overcurrent or zero crossing detection. Overall, with a high degree of configurability and integrated features, the ACS37800 can fit most power monitoring applications. The following sections will help explain in more detail these features and configuration options, as well as how to best use the ACS37800 for particular applications.

### Voltage and Current Measurements

The main signal paths for the current and voltage measurement, through the ADCs and internal filtering, have a bandwidth of 1 kHz and an update rate of 32 kHz. These “instantaneous”

current and voltage measurements are stored in the *icodes* and *vcodes* fields. The instantaneous apparent power, which is the product of *icodes* and *vcodes*, is stored in the field *pinstant*.

### Overcurrent Measurement Path

A separate filter on the current ADC is used to create a lower resolution but higher bandwidth sample rate measurement of the current to be used for overcurrent detection. This filter outputs a 12-bit word at a 1 MHz update rate and 200 kHz bandwidth. The overcurrent fault logic compares this auxiliary current value to the user-defined overcurrent fault threshold, defined by the field *fault*.

It is important to note that the trim for the main 16-bit current path is also applied to the overcurrent path, such that the overcurrent fault has the same level of accuracy as the main signal path.

### Trim Methods

The trim logic for the voltage and current channels is depicted in Figure 4 and Figure 5. Refer to the Register Details section for more information regarding trim fields. In general, each channel, voltage and current, is trimmed for gain and offset both at room and over temperature. This trim is done before the *icodes* and *vcodes* registers. The user has the ability to trim the nominal room temperature value.

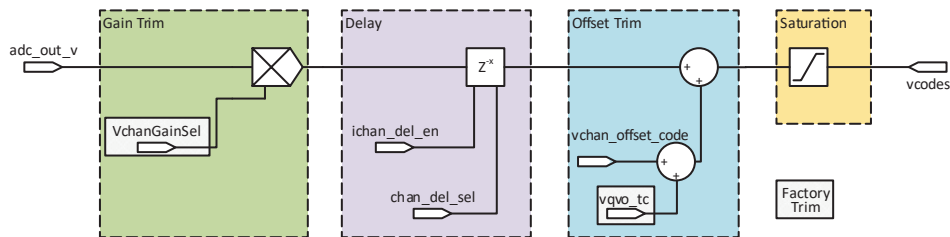


Figure 4: Voltage Channel Trim Flow

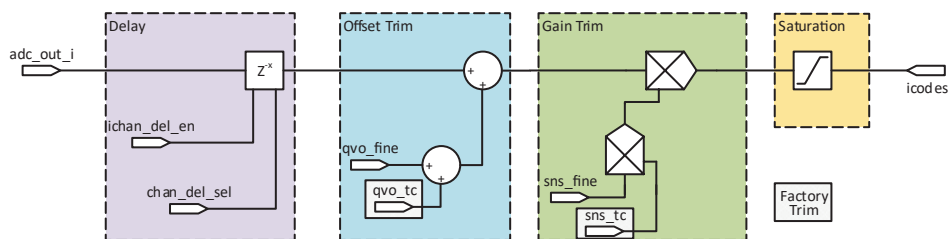


Figure 5: Current Channel Trim Flow

## Power Calculations

### VOLTAGE ZERO CROSSING

The RMS and power calculations of the ACS37800 are calculated over a window of N samples. By default, this window is calculated dynamically based on the zero crossings of the voltage signal. A rising voltage zero crossing triggers the start of a new window. N then increases with each 32 kHz sample until the next rising voltage zero crossing, recording the current and voltage readings at each sample. This ends the calculation window, and all RMS and power calculations are performed on the saved data. During this time, the next calculation window is started.

Voltage zero crossings are detected with time-based hysteresis that removes the possibility of noise causing multiple zero crossings to be reported at each true zero crossing.

### I<sub>RMS</sub> AND V<sub>RMS</sub>

The cycle-by-cycle calculation of the root mean square of both the current and voltage channels is:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{n=N-1} I_n^2}{N}} \quad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{n=N-1} V_n^2}{N}}$$

where  $I_n$  (*icodes*) and  $V_n$  (*vcodes*) are the instantaneous measurements of current and voltage, respectively.

### APPARENT POWER

The magnitude of the complex power being measured; calculated at the end of each cycle is:

$$|S| = I_{RMS} \times V_{RMS}$$

### ACTIVE POWER

The real component of power being measured, calculated cycle by cycle is:

$$P_{ACTIVE} = \frac{\sum_{n=0}^{n=N-1} P_n}{N} \quad P_n = I_n \times V_n$$

### REACTIVE POWER

The imaginary component of power being measured, calculated at the end of each cycle is:

$$Q = \sqrt{S^2 - P_{ACTIVE}^2}$$

## POWER FACTOR

The magnitude of the ratio of the real power to apparent power, calculated at the end of each cycle is:

$$|PF| = \frac{P_{ACTIVE}}{|S|}$$

## LEADING OR LAGGING POWER FACTOR

The current leading or lagging the voltage is communicated as a single bit, *posangle*. This bit represents the sign of the reactive power. The sign of the reactive power is determined by comparing the timing of the zero crossings of the current and voltage. As such, it is only meaningful in the case of a linear load.

The sign of the reactive power, *posangle*, along with the sign of the power factor, *pospf*, can be used to determine whether the load is inductive or capacitive, as well as whether power is being generated or consumed. This is shown in the four-quadrant figure below (refer to Figure 6).

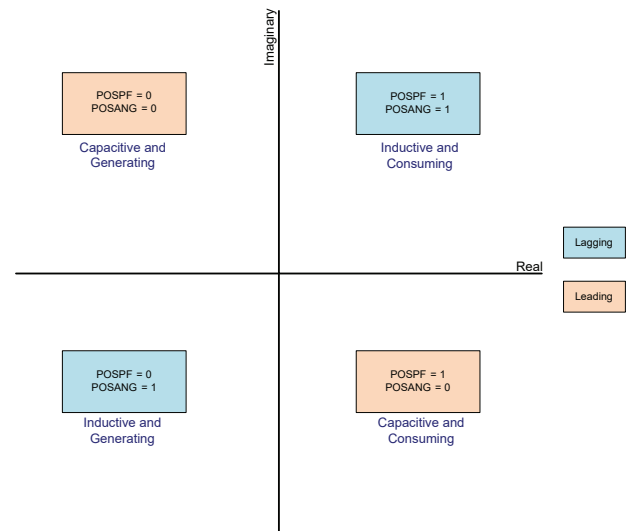


Figure 6: Four Quadrant, Power Factor

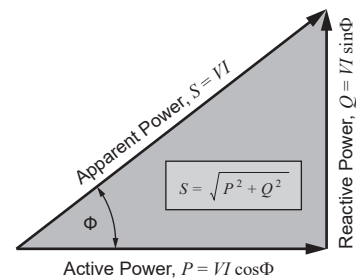


Figure 7: Power Triangle

## OPERATIONAL BLOCK DIAGRAM

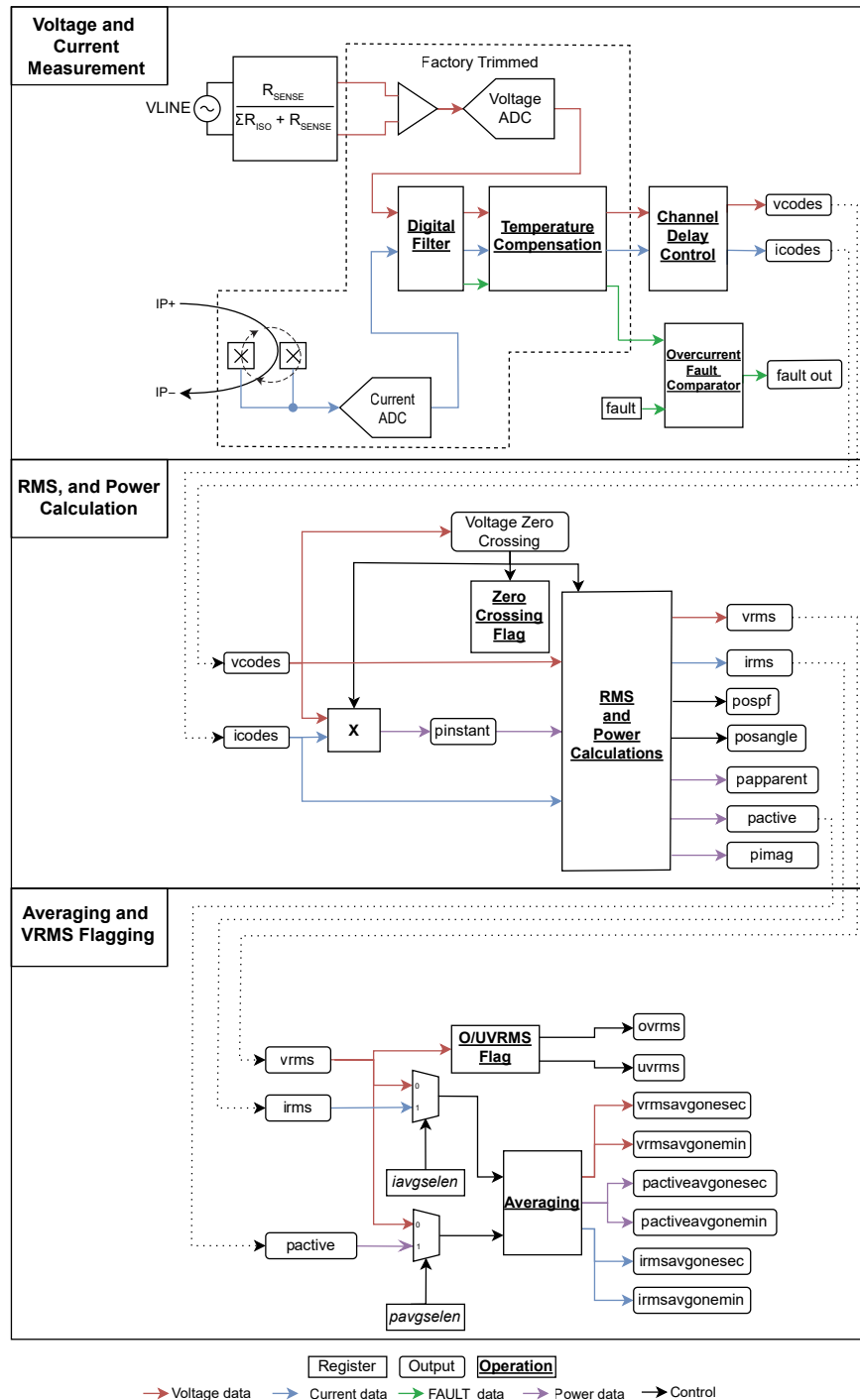


Figure 8: Operational Block Diagram

### Configurable Settings

#### PHASE DELAY

Phase delay may be introduced on either the voltage or current channel to account for known phase delay at other points in the system using the *ichan\_del\_en* and *chan\_del\_sel* fields. *ichan\_del\_en* determines if the voltage channel or current channel will be delayed. The chosen channel will be delayed by the configured amount in *chan\_del\_sel*, up to 5° of delay.

#### AVERAGING CHANNEL

The ACS37800 contains two averaging paths.  $V_{RMS}$ ,  $I_{RMS}$ , and  $P_{ACTIVE}$  can be routed to these average blocks as shown in Figure 8 using *iavgselen* and *pavgselen*.

#### AVERAGING TIME

Each averaging path on the ACS37800 consists of two averaging blocks that each allow for a configurable number of averages based on the EEPROM fields *rms\_avg\_1* and *rms\_avg\_2*.

The output of the first averaging block feeds into the input of the second averaging block. The output of each block is accessible for each channel.

#### OVERVOLTAGE AND UNDERVOLTAGE DETECTION FOR VRMS

This device has programmable overvoltage and undervoltage RMS flags that will signal when the *vrms* is above or below the respective thresholds. The *vrms* is compared to the overvoltage and undervoltage RMS thresholds set by the fields *overvreg* and *undervreg* to determine a flag condition. The number of successive sample sets required to trigger either the overvoltage or undervoltage RMS flag can be set by the *vevent\_cycles* field.

The *ovrms* and *uvrms* flags can be routed to the DIO pins when the device is used in I<sup>2</sup>C mode. See Configuring the DIO Pins.

#### OVERCURRENT DETECTION FOR INSTANTANEOUS CURRENT

The overcurrent fault threshold may be set from  $0.65 \times I_{PR}$  to  $2.0 \times I_{PR}$ . The user sets the trip point with the field *fault*. The user can add a digital delay to the overcurrent fault with the field *flt\_dly*. Up to 32  $\mu$ s delay can be added to the overcurrent fault.

#### BYPASSING THE DYNAMIC FRAMING OF THE RMS CALCULATION WINDOW

By default, the ACS37800 dynamically calculates the value of N to be used in the RMS and power calculations based on the zero crossings on the voltage channel. This functionality can be disabled using the *bypass\_n\_en* field.

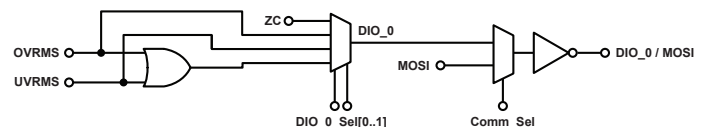
When *bypass\_n\_en* = 1, it is important to define the number of samples used to calculate RMS. This can be done in the field *n*. The field *n* is the number of 32 kHz samples that are used to calculate the RMS. The minimum effective *n* that is used when calculating RMS is 4. If a value of less than 4 is chosen for *n*, then 4 is internally used. The first useable RMS calculation on start up with *bypass\_n\_en* = 1 is after  $2 \times n$  samples.

### Configuring the DIO Pins (I2C Devices)

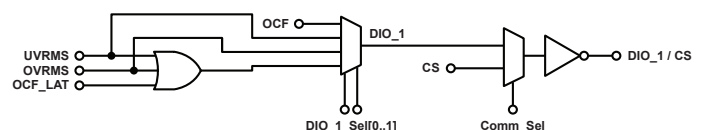
#### FLAGS TO BE ROUTED TO THE DIO PINS

When the device is configured to be in I<sup>2</sup>C mode (*comm\_sel* in EEPROM = 1), pins 9 and 10 become digital I/O pins, DIO\_1 and DIO\_0, respectively. The digital I/O pins are low true, meaning that a voltage below the DIO Output Low Level maximum ( $V_{OL(DIO)max}$ ) is to be interpreted as logic 1 and a voltage above DIO Output High Level minimum ( $V_{OH(DIO)min}$ ) is to be interpreted as a logic 0. The Digital I/O pins can be configured in EEPROM to represent the following functions:

DIO_0	
dio_0_sel value (EEPROM)	Function
0	ZC: zero crossing
1	ovrms: the VRMS overvoltage flag
2	uvrms: The VRMS undervoltage flag
3	The OR of ovrms and uvrms (if either flag is triggered, the DIO_0 pin will be asserted)



DIO_1	
dio_1_sel value (EEPROM)	Function
0	OCF: Overcurrent fault
1	uvrms: The VRMS undervoltage flag
2	ovrms: The VRMS overvoltage flag
3	The OR of ovrms and uvrms, and OCF_LAT [Latched Overcurrent Fault] (if any of the three flags are triggered, the DIO_1 pin will be asserted)





### ZERO CROSSING OUTPUT CONFIGURATIONS

The dynamic calculation of N for the RMS and power calculations uses exclusively the voltage zero crossing, but both current and voltage zero crossing can be flagged and reported on the DIO pins.

#### Voltage Zero Crossing (VZC)

The voltage zero crossing has two basic modes of operation, pulse mode and square wave mode.

#### Pulse Mode – VZC

In pulse mode, a voltage zero crossing is reported as a short pulse. There are three available configurations to customize the voltage zero crossing pulse mode operation: rising or falling edge selection, every edge selection, and pulse width.

#### Rising Edge or Falling Edge Aligned Pulse

The EEPROM field *zerocrossedgesel* is used to select whether the zero crossing output pulses are aligned to the rising zero crossing of the voltage channel or the falling zero crossing of the voltage channel.

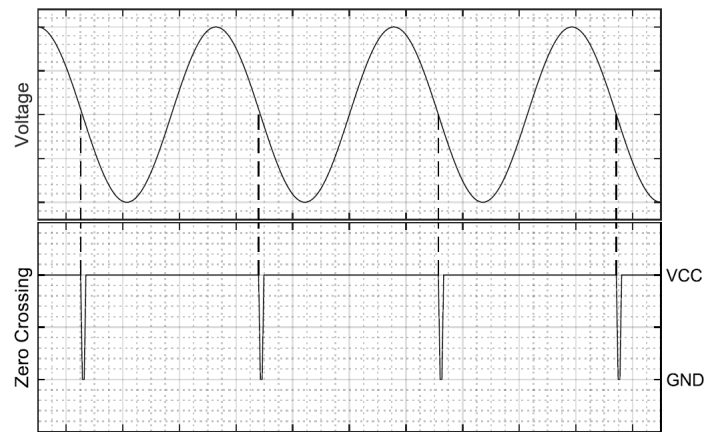


Figure 9: *zerocrossedgesel* = 0, Falling Zero Crossing

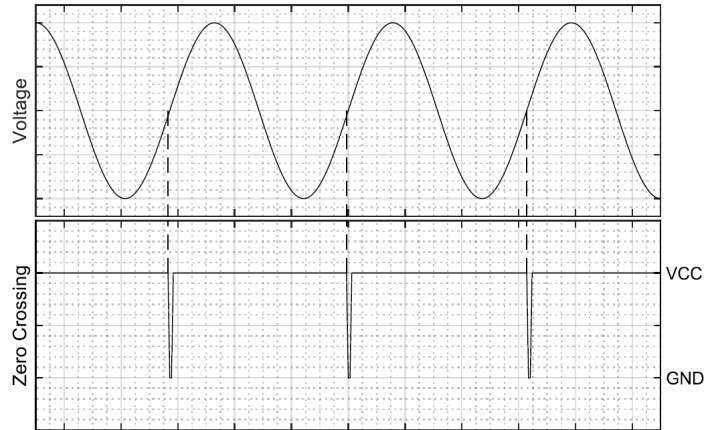


Figure 10: *zerocrossedgesel* = 1, Rising Zero Crossing

#### Pulse Every Edge

The EEPROM field *halfcycle\_en* is used to output a pulse at every zero crossing.

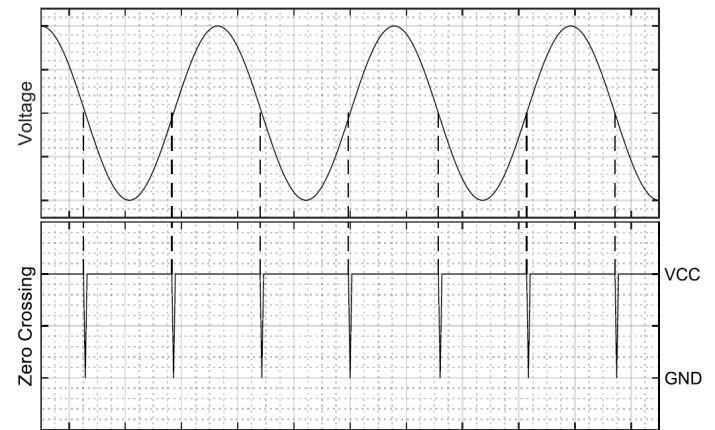


Figure 11: *halfcycle\_en* = 1, Both Rising and Falling Zero Crossings Signaled

#### Pulse Width Selection

The EEPROM field *delaycnt\_sel* is used to select the width of the voltage zero crossing pulse.

Table 1: *delaycnt\_sel*

Range	Value	Units
0	32	μs
1	256	μs

### Square Wave Mode

Square wave mode can be configured using the EEPROM field *squarewave\_en*. In square wave mode, a voltage zero crossing is reported as a square wave that changes state on each reported zero crossing. The *zerocrossedgesel* EEPROM field can be used to align the low to high transition of the flag with either the rising voltage zero crossing or the falling voltage zero crossing.

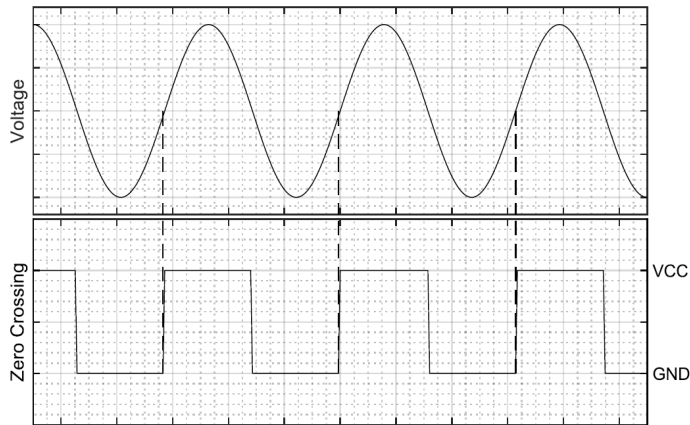


Figure 12: *zerocrossedgesel* = 0, Square Wave Mode

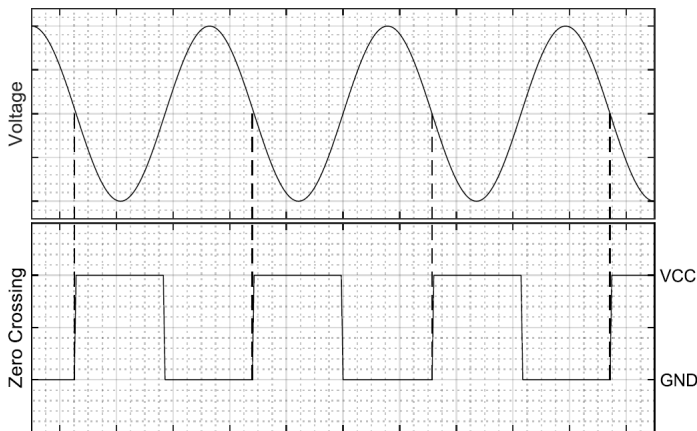


Figure 13: *zerocrossedgesel* = 1, Square Wave Mode

### Current Zero Crossing (CZC)

The current zero crossing function can be enabled using the EEPROM field *zerocrosschansel*. When the zero crossing flag is configured to flag zero crossings of the current path, this has no effect on the RMS and power calculations; the voltage zero crossing is still used for these calculations.

The current zero crossing has just one basic mode of operation: pulse mode.

### Pulse Mode – CZC

In pulse mode, a current zero crossing is reported as a short pulse. There are three available configurations to customize the current zero crossing pulse mode operation: rising or falling edge selection, every edge selection, and pulse width.

#### Rising Edge or Falling Edge Aligned Pulse

The EEPROM field *zerocrossedgesel* is used to select whether the zero crossing output pulses are aligned to the rising zero crossing of the current channel or the falling zero crossing of the current channel.

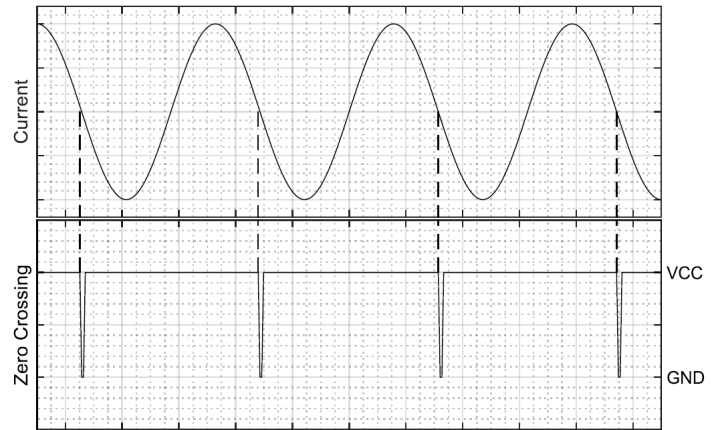


Figure 14: *zerocrossedgesel* = 0, Falling Zero Crossing

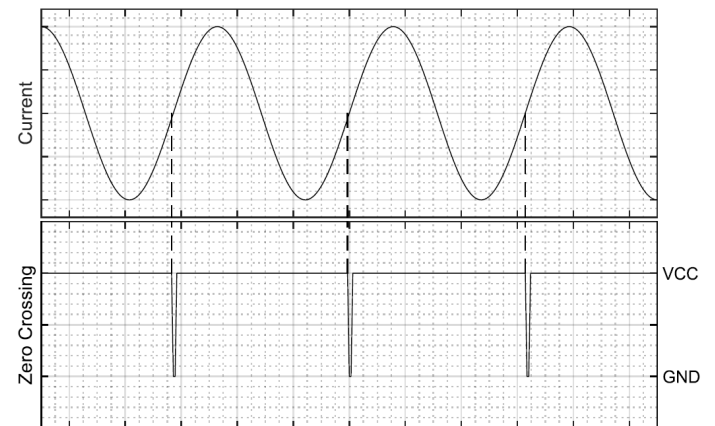
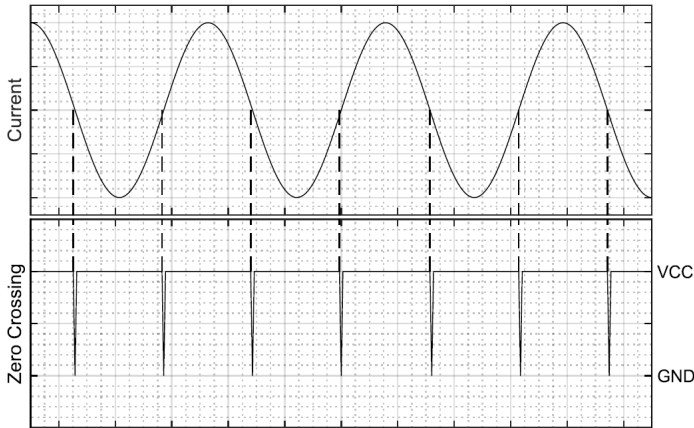


Figure 15: *zerocrossedgesel* = 1, Rising Zero crossing

### Pulse Every Edge

The EEPROM field *halfcycle\_en* is used to output a pulse at every zero crossing.



**Figure 16: *halfcycle\_en* = 1, Both Rising and Falling Zero Crossings Signaled**

## CONFIGURING THE DEVICE FOR AC APPLICATIONS

### Device EEPROM Settings

For AC power monitoring applications using the ACS37800, the following device settings are recommended:

### DYNAMIC CALCULATION OF N

Set *bypass\_n\_en* = 0 (default). This setting enables the device to dynamically calculate N based off the voltage zero crossings. See the Register Details – EEPROM section for additional details.

### Voltage Measurement

#### RECOMMENDED APPLICATION CIRCUITS

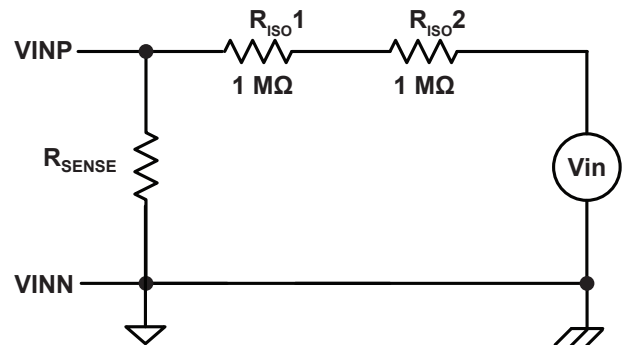
An important aspect to consider when designing in the ACS37800 into AC applications is the design of the voltage measurement path. Typically, a resistor divider network is employed to provide both isolation and transform the high voltage signal into the  $\pm 250$  mV signal that the ACS37800 can measure.

There are two basic application circuits recommended based on the isolation requirements of the system. The first, see Figure 17, is to be used when the ACS37800 GND and the neutral terminal of the voltage input are connected.  $R_{ISO1}$ ,  $R_{ISO2}$ , and  $R_{SENSE}$

form a resistor divider network where,

$$V_{IN} = V_{LINE} * \frac{R_{SENSE}}{R_{ISO1} + R_{ISO2} + R_{SENSE}}$$

$R_{ISO1}$  and  $R_{ISO2}$  should be equal. A value of 1 M $\Omega$  is appropriate for many applications, but ultimately, the resistance value used needs to comply with the required isolation of the system.

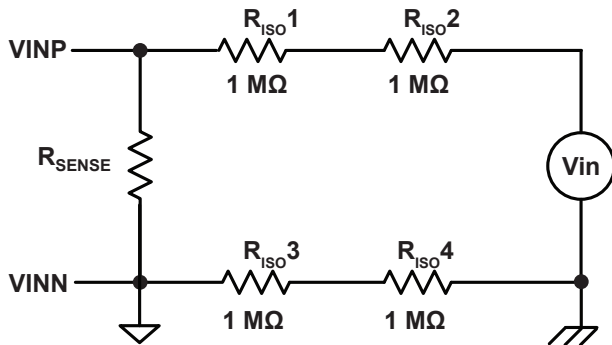


**Figure 17: Voltage Channel Application Circuit; Device GND is Connected to Neutral**

Another application circuit recommendation for the voltage channel is shown in Figure 18. This is to be used in systems where the ACS37800 GND and the neutral terminal of the voltage input are to be isolated. Here,  $R_{ISO3}$  and  $R_{ISO4}$  are added to the resistor divider network.

$$V_{IN} = V_{LINE} * \frac{R_{SENSE}}{R_{ISO1} + R_{ISO2} + R_{ISO3} + R_{ISO4} + R_{SENSE}}$$

$R_{ISO1}$ ,  $R_{ISO2}$ ,  $R_{ISO3}$ , and  $R_{ISO4}$  should be equal and their value is determined by the isolation requirements of the system. A value of 1 MΩ is appropriate for many applications, but ultimately, the resistance value used needs to comply with the required isolation of the system.



**Figure 18: Voltage Channel Application; Device GND is Isolated from Neutral**

To determine the value of  $R_{SENSE}$  required for a particular application using either of the recommended circuits, the following equation can be used:

$$R_{SENSE} = \frac{\Delta V_{INR(MAX)}}{V_{LINE(MAX)} - \Delta V_{INR(MAX)}} * R_{ISO}$$

Where  $\Delta V_{INR(MAX)} = 250$  mV,  $V_{LINE(MAX)}$  is the maximum  $V_{LINE}$  voltage to be measured, and  $R_{ISO}$  is the sum of all of the isolation resistors.

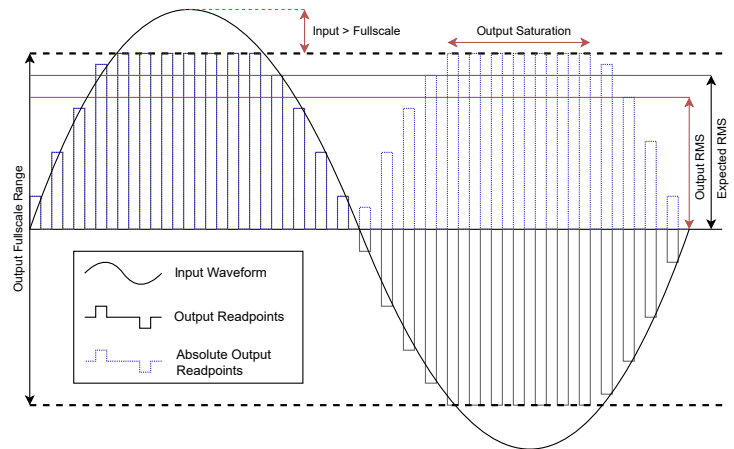
If using the overvoltage detection functionality of the ACS37800, this should be considering when determining the maximum  $V_{LINE}$  voltage to be measured. For example, in an application when the nominal  $V_{LINE}$  is equal to 120  $V_{RMS}$  and a 50% over-voltage detection is required,  $V_{LINE(MAX)}$  is:

$$120 V_{RMS} \times \sqrt{2} \times 1.5 = 255 V,$$

where the  $\sqrt{2}$  is used to approximate the peak voltage assuming a sinusoidal input.

Additionally, the tolerance of the all resistors should be considered when determining  $R_{SENSE}$ . The minimum tolerance of the isolation resistors should be used along with the maximum tolerance of  $R_{SENSE}$ .

If the  $R_{SENSE}$  is not sized appropriately, this can lead to the voltage input to the ACS37800 exceeding the maximum input range, which can cause the instantaneous voltage measurement to saturate. This can lead to errors in the RMS calculations as shown in Figure 19.



**Figure 19: Output Saturation**

### Current Measurement

For the current path, there are two current ranges to consider: the range of RMS current to be measured and the range required for overcurrent fault detection.

When considering the range of RMS current to be measured, the Current Sensing Range ( $I_{PR}$ ) is not to be exceeded. This can lead to saturation, as shown in Figure 19, and lead to error in the RMS calculations.

The overcurrent fault detection can exceed  $I_{PR}$  and is defined as Fault Range Max,  $I_{FAULT(MAX)}$ . Once the current exceeds  $I_{PR}$ , the RMS calculations will no longer be accurate.

### CONFIGURING THE DEVICE FOR DC APPLICATIONS OR FOR APPLICATIONS WITH NO VOLTAGE ZERO CROSSING

The follow recommendations are provided for DC applications, as well as any other applications where there is no voltage zero crossing. Possible applications include current sensing only, sensing of a rectified voltage signal, or applications where the nominal frequency on the voltage channel is greater than 300 Hz.

#### Device EEPROM Settings

For DC power monitoring applications using the ACS37800 or applications only using the current measurement capability of the ACS37800, the following device settings are recommended.

#### FIXED SETTING OF N

Set *bypass\_n\_en* = 1. This setting disables the dynamic calculation of *n* based off voltage zero crossings and sets *n* to a fixed

value, which is set using EEPROM field *n*. See the Register Details – EEPROM section for additional details.

#### Voltage Measurement

#### RECOMMENDED APPLICATION CIRCUITS

The recommended application circuit for the voltage channel in DC operation is the same as the AC application circuit where Device GND is connected to Neutral (refer to Figure 17).

#### Current Measurement

The same considerations for AC applications can be used for the current path for DC applications.

### RMS AND POWER ACCURACY VS. OPERATION POINT

#### RMS and Power Output Error vs. Applied Input

When using the ACS37800 to measure for RMS calculations and power monitoring, it is important to consider the error specifications of the device.

For DC applications, the impact of offset and gain error on the final output is straightforward, but for RMS and power calculations, the impact of any errors, specifically offset errors, becomes dependent on the magnitude of the applied signal.

Figure 20 shows an example system where the maximum measurable power is ~1.3 kW, based on the system design. The over-temperature offset performance of the ACS37800 causes an error in the measured power that is larger when the applied power is close to 0 W.

The offset performance of the voltage channel is such that its contribution to this error is negligible. The current RMS measurement and the power calculations are where this error is observed.

The following figures (Figure 21 through Figure 26) display the measurement error for the RMS current and active power for each available device variant.

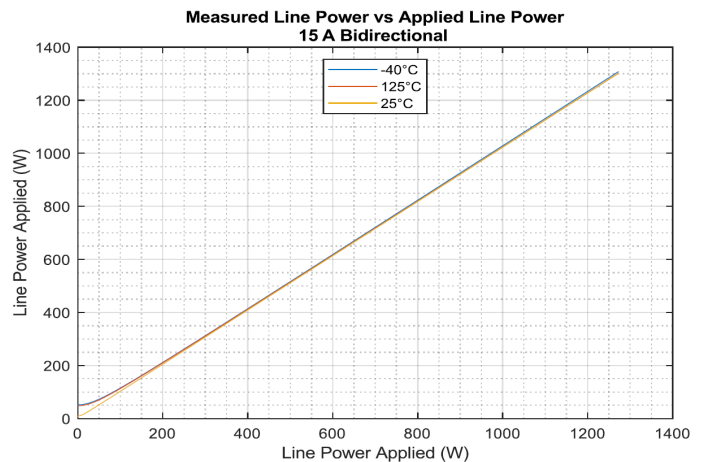


Figure 20: Measured Line Power [W] vs. Applied Line Power, 15B5 Device

## 15B5 I<sub>RMS</sub> and Power Error

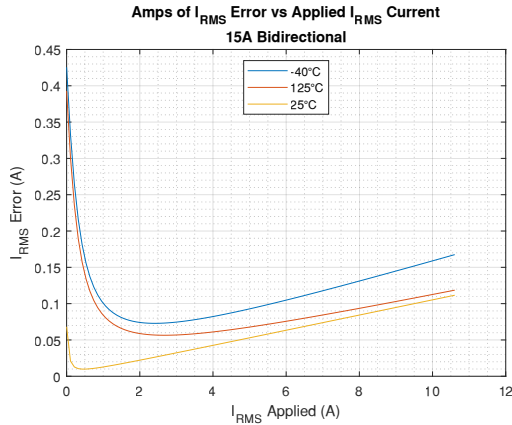


Figure 21: I<sub>RMS</sub> Error [A] vs. Applied I<sub>RMS</sub> [A]

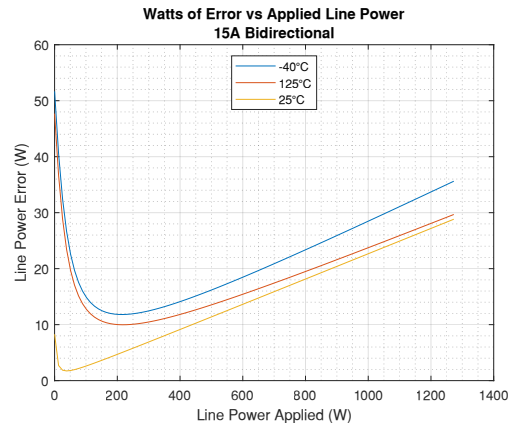


Figure 22: Line Power Error [W] vs. Applied Line Power [W]

## 30B3 I<sub>RMS</sub> and Power Error

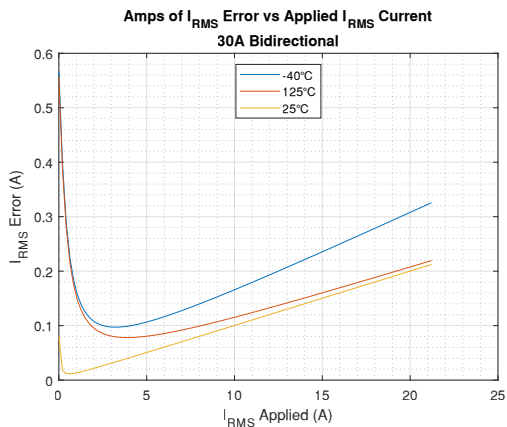


Figure 23: I<sub>RMS</sub> Error [A] vs. Applied I<sub>RMS</sub> [A]

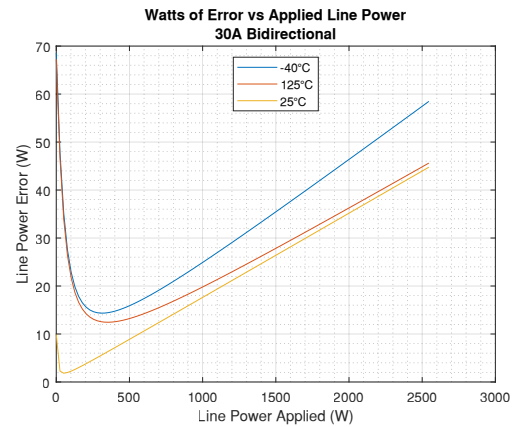


Figure 24: Line Power Error [W] vs. Applied Line Power [W]

## 90B3 I<sub>RMS</sub> and Power Error

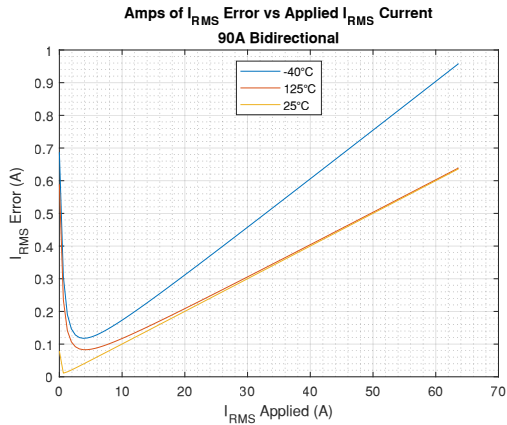


Figure 25: I<sub>RMS</sub> Error [A] vs. Applied I<sub>RMS</sub> [A]

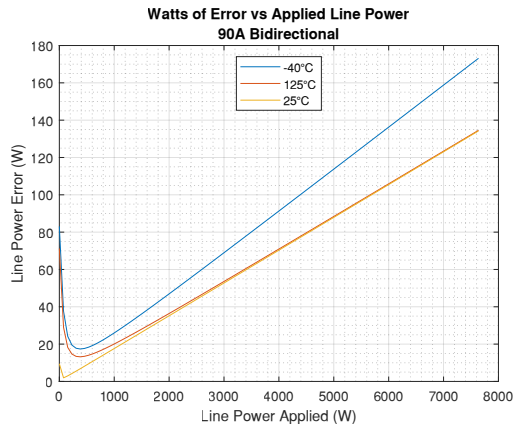


Figure 26: Line Power Error [W] vs. Applied Line Power [W]

### DIGITAL COMMUNICATION

#### Communication Interfaces

The ACS37800 supports communication over 1 MHz I<sup>2</sup>C and 10 MHz SPI. However, the communication protocol is fixed during factory programming. The ACS37800 MISO pin continues to drive the MISO line when CS goes high. This may prevent other devices from communicating properly. It is recommended that the ACS37800 be the only device on the SPI bus if using SPI communication.

#### SPI

The SPI frame consists of:

- The Master writes on the MOSI line the 7-bit address of the register to be read from or written to.
- The next bit on the MOSI line is the read/write (RW) indicator. A high state indicates a Read and a low state indicates a Write.
- The device sends a 32-bit response on the MISO line. The contents correspond to the previous command.
- On the MOSI line, if the current command is a write, the 32 bits correspond to the Write data, and in the case of a read, the data is ignored.

#### Registers and EEPROM

##### WRITE ACCESS

The ACS37800 supports factory and customer EEPROM space as well as volatile registers. The customer access code must be sent prior to writing these customer EEPROM spaces. In addition, the device includes a set of free space EEPROM registers that are accessible with or without writing the access code.

##### READ ACCESS

All EEPROM and volatile registers may be read at any time regardless of the access code.

##### EEPROM

At power up, all shadow registers are loaded from EEPROM, including all configuration parameters. The shadow registers can be written to in order to change the device behavior without having to perform an EEPROM write. Any changes made in shadow memory are volatile and do not persist through a reset event.

##### WRITING

The Timing Diagram for an EEPROM write is shown in Figure 27 and Figure 28.

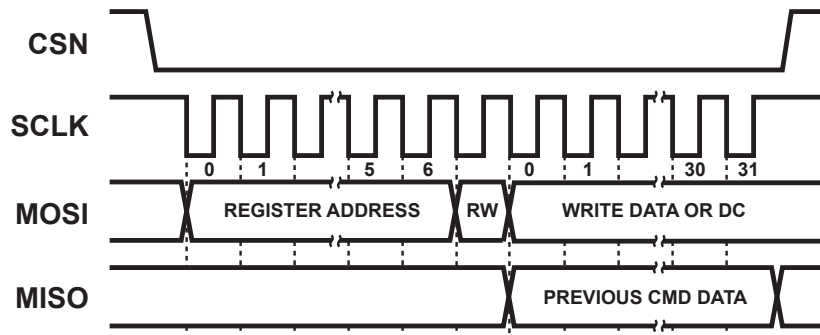


Figure 27: EEPROM Write – SPI Mode

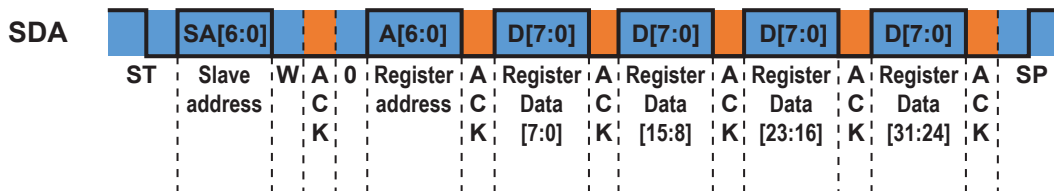
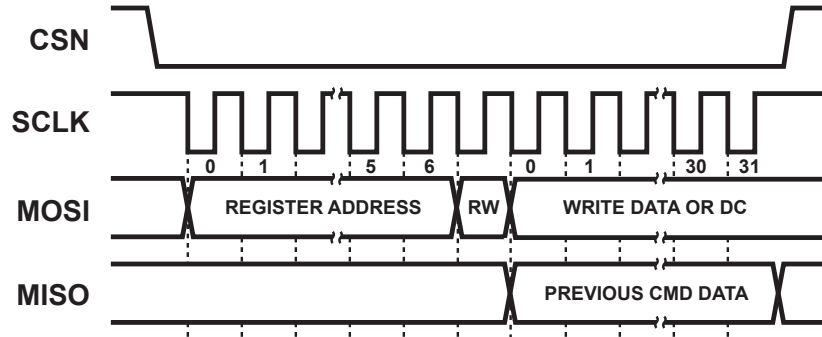


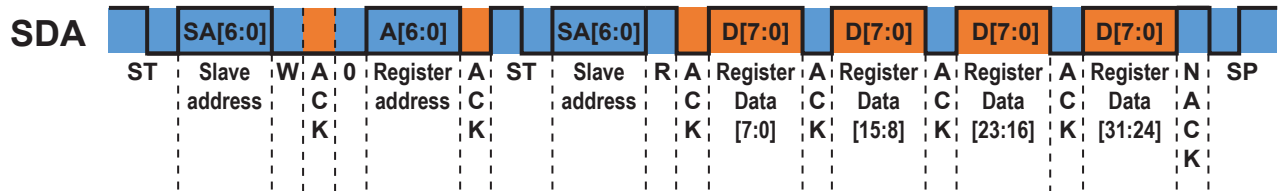
Figure 28: EEPROM Write – I<sup>2</sup>C Mode  
Blue represents data sent by the master and orange is the data sent by the slave.

### READING

The timing diagram for an EEPROM read is shown in Figure 29 and Figure 30.



**Figure 29: EEPROM Read – SPI Mode**  
For SPI, the read data will be sent out during the above command.



**Figure 30: EEPROM Read – I<sup>2</sup>C Mode**  
Blue represents data sent by the master and orange is the data sent by the slave.



### EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction (ECC). ECC is enabled after power-up.

The ACS37800 analyzes message data sent by the controller and the ECC bits are added. The first 6 bits sent from the device to the controller are dedicated to ECC. The device always returns 32 bits.

#### EEPROM ECC Errors

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

### I<sup>2</sup>C Slave Addressing

The ACS37800 supports I<sup>2</sup>C communication over the SCL and SDA lines at speeds of up to 400 kHz. When the device first powers on, it measures the voltage level on the two DIO pins. It converts both voltage levels into a 4-bit code for a total of sixteen slave addresses. Table 2 shows the sixteen possible I<sup>2</sup>C configurations that can be set with externally applied voltage. If both pins are pulled to V<sub>CC</sub>, then the internal slave address stored in EEPROM is used. By default, the value of *i2c\_slv\_addr* is programmed at the Allegro factory to 127, but this can be changed with programming by the customer.

If for any reason the external slave address setting feature is not desired, the DIO polling can be disabled by setting the *i2c\_dis\_slv\_addr*. When this bit is set, the ACS37800 will automatically use the number stored in *i2c\_slv\_addr* as the I<sup>2</sup>C slave address regardless of the voltage on the DIO pins. Note that the device must be repowered for these changes to take effect.

**Table 2: DIO Startup Voltage Addressing**

DIO_1	DIO_2	A6	A5	A4	A3	A2	A1	A0	Slave Address (decimal)
0	0	0	0	1	1	0	0	0	97
0	0	0	1	1	1	0	0	0	97
0	0	1	0	1	1	0	0	0	98
0	0	1	1	1	1	0	0	0	99
0	1	0	0	1	1	0	0	1	100
0	1	0	1	1	1	0	0	1	101
0	1	1	0	1	1	0	0	1	102
0	1	1	1	1	1	0	0	1	103
1	0	0	0	1	1	0	1	0	104
1	0	0	1	1	1	0	1	0	105
1	0	1	0	1	1	0	1	0	106
1	0	1	1	1	1	0	1	0	107
1	1	0	0	1	1	0	1	1	108
1	1	0	1	1	1	0	1	1	109
1	1	1	0	1	1	0	1	1	110
1	1	1	1	EE	EE	EE	EE	EE	EEPROM value

### MEMORY MAP

#### EEPROM/Shadow Memory

	Address	Bits																																					
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
EEPROM	0x0B	ECC								paavgsel	iaavgsel	crs_sns			sns_fine								qvo_fine																
	0x0C	ECC				vchan_offset_code						rms_avg_2								rms_avg_1																			
	0x0D	ECC								ftdly			fault										chan_del_sel			ichan_del_en													
	0x0E	ECC								zerocrossedgesel	zerocrosschansel	squarewave_en	halfcycle_en	delaycnt_sel	undervreg								overvreg								vevent_cycs								
	0x0F	ECC								bypass_n_en	n								dio_1_sel		dio_0_sel		i2c_dis_slv_addr		i2c_slv_addr														
Shadow	0x1B																																						
	0x1C																																						
	0x1D																																						
	0x1E																																						
	0x1F																																						

### Register Details – EEPROM

#### Register 0x0B/0x1B

Bits	Name	Default Value	Description
8:0	<i>qvo_fine</i>	Device Specific	Offset fine trimming on current channel
18:9	<i>sns_fine</i>	Device Specific	Fine gain trimming on the current channel
21:19	<i>crs_sns</i>	Selection Specific	Coarse gain setting
22	<i>iavgselen</i>	0	Current Averaging selection
23	<i>pavgselen</i>	0	Power Averaging selection
31:26	<i>ecc</i>	–	Error Code Correction

#### *qvo\_fine*

Offset adjustment for the current channel. This is a signed 9-bit number with an input range of –256 to 255. With a step size of 64 LSB, this equates to an offset trim range of –16384 to 16320 LSB, which is added to the *icodes* value. The current channel’s offset trim should be applied before the gain is trimmed. *qvo\_fine* is further described in Table 3.

Table 3: *qvo\_fine*

Range	Value	Units
–256 to 255	–16,384 to 16,320	LSB

#### *sns\_fine*

Gain adjustment for the current channel. This is a signed 9-bit number with an input range of –256 to 255. This gain adjustment is implemented as a percentage multiplier centered around 1 (i.e. writing a 0 to this field multiplies the gain by 1, leaving the gain unaffected). The fine sensitivity parameter ranges from 50% to 150% of IP. The current channel’s offset trim should be applied before the gain is trimmed. *sns\_fine* is further described in Table 4.

Table 4: *sns\_fine*

Range	Value	Units
–256 to 255	50 to 100	%

#### *crs\_sns*

Coarse gain adjustment for the current channel. This gain is implemented in the analog domain before the ADC. This is a 3-bit number that allows for 8 gain selections. Adjustments to *crs\_sns* may impact the device’s performance over temperature. Datasheet limits apply only to the factory settings for *crs\_sns*. The gain settings map to 1×, 2×, 3×, 3.5×, 4×, 4.5×, 5.5×, and 8×. *crs\_sns* is further described in Table 5.

Table 5: *crs\_sns*

Range	Value	Units
0	1×	–
1	2×	–
2	3×	–
3	3.5×	–
4	4×	–
5	4.5×	–
6	5.5×	–
7	8×	–

#### *iavgselen*

Current Averaging selection enable. 0 will select *vrms* for averaging. 1 will select *irms* for averaging.

#### *pavgselen*

Power Averaging selection enable. 0 will select *vrms* for averaging. 1 will select *active* for averaging.

### Register 0x0C/0x1C

Bits	Name	Default Value	Description
6:0	<i>rms_avg_1</i>	0	Average of the <i>rms</i> voltage or current – stage 1
16:7	<i>rms_avg_2</i>	0	Average of the <i>rms</i> voltage or current – stage 2
24:17	<i>vchan_offset_code</i>	Device Specific	Controls the room offset for the voltage channel
31:26	<i>ecc</i>	–	Error Code Correction

#### *rms\_avg\_1*

Number of averages for the first averaging stage (*vrmsavgonesec* or *irmsavgonesec*). The value written into this field directly maps to the number of averages ranging from 0 to 127. For optimal performance, an even number of averages should be used. The channel to be averaged is selected by the current average select enable bit (*iavgselect*). *rms\_avg\_1* is further described in Table 6.

**Table 6: *rms\_avg\_1***

Range	Value	Units
0 to 127	0 to 127	number of averages

#### *rms\_avg\_2*

Number of averages for the second averaging stage (*vrmsavgone-min* or *irmsavgone-min*). This stage averages the outputs of the first averaging stage. The value written into this field directly maps to the number of averages ranging from 0 to 1023. For optimal performance, an even number of averages should be used. The channel to be averaged is selected by the current average select enable bit (*iavgselect*). *rms\_avg\_2* is further described in Table 7.

**Table 7: *rms\_avg\_2***

Range	Value	Units
0 to 1023	0 to 1023	number of averages

#### *vchan\_offset\_code*

This controls the offset of the voltage channel at room.

**Table 8: *vchan\_offset\_code***

Range	Value	Units
–128 to 127	–2048 to 2032	codes

### Register 0x0D/0x1D

Bits	Name	Default Value	Description
7	<i>ichan_del_en</i>	0	Enable phase delay on voltage or current channel
11:9	<i>chan_del_sel</i>	0	Sets phase delay on voltage or current channel
20:13	<i>fault</i>	70	Sets the overcurrent fault threshold
23:21	<i>ftdly</i>	0	Sets the overcurrent fault delay
31:26	<i>ecc</i>	–	Error Code Correction

#### *ichan\_del\_en*

Enables delay for either the voltage or current channel. Setting to 1 enables delay for the current channel. *ichan\_del\_en* is further described in Table 9.

**Table 9: *ichan\_del\_en***

Range	Value	Units
0	0 – voltage channel	LSB
1	1 – current channel	LSB

#### *chan\_del\_sel*

Sets the amount of delay applied to the voltage or current channel (set by *ichan\_del\_en*). *chan\_del\_sel* is further described in Table 10.

**Table 10: *chan\_del\_sel***

Range	Value	Units
0 to 7	0 to 219	μs

#### *fault*

Over-current fault threshold. This is an unsigned 8-bit number with an input range of 0 to 255, which equates to a fault range of 65% to 200% of IP. The factory setting of this field is 70. *fault* is further described in Table 11.

**Table 11: *fault***

Range	Value	Units
0 to 255	56 to 225	% of IP

#### *ftdly*

Fault delay setting of the amount of delay applied before flagging a fault condition. *ftdly* is further described in Table 12.

**Table 12: *ftdly***

Range	Value	Units
0	0	μs
1	0	μs
2	4.75	μs
3	9.25	μs
4	13.75	μs
5	18.5	μs
6	23.25	μs
7	27.75	μs

### Register 0x0E/0x1E

Bits	Name	Default Value	Description
5:0	<i>vevent_cycs</i>	0	Sets the number of qualifying cycles needed to flag overvoltage or undervoltage
13:8	<i>overvreg</i>	0	Sets the overvoltage fault threshold
19:14	<i>undervreg</i>	0	Sets the undervoltage fault threshold
20	<i>delaycnt_sel</i>	0	Sets the width of the voltage zero-crossing output pulse
21	<i>halfcyc_en</i>	0	Sets the zero crossing flag triggering on half or full cycle (default: full cycle)
22	<i>squarewave_en</i>	0	Sets the zero crossing pulse characteristics (default: pulse)
23	<i>zercrosschansel</i>	0	Sets the channel that triggers the zero crossing flag (default: voltage)
24	<i>zercrossedgesel</i>	0	Sets the edge that triggers zero crossing flag
31:26	<i>ecc</i>	–	Error Code Correction

#### ***vevent\_cycs***

Sets the number of cycles required to assert the *ovrms* flag or the *uvrms*. This is an unsigned 6-bit number with an input range of 0 to 63. The value in this field directly maps to the number of cycles. *vevent\_cycs* is further described in Table 13.

**Table 13: *vevent\_cycs***

Range	Value	Units
0 to 63	1 to 64	cycles

#### ***overvreg***

Sets the threshold of the overvoltage *rms* flag (*ovrms*). This is a 6-bit number ranging from 0 to 63. This trip level spans the entire range of the *vrms* register. The flag is set if the *rms* value is above this threshold for the number of cycles selected in *vevent\_cycs*. *overvreg* is further described in Table 14.

**Table 14: *overvreg***

Range	Value	Units
0 to 63	0 to 65536	LSB

#### ***undervreg***

Sets the threshold of the undervoltage *rms* flag (*uvrms*). This is a 6-bit number ranging from 0 to 63. This trip level spans one entire range of the *vrms* register. The flag is set if the *rms* value is below this threshold for the number of cycles selected in *vevent\_cycs*. *undervreg* is further described in Table 15.

**Table 15: *undervreg***

Range	Value	Units
0 to 63	0 to 65536	LSB

#### ***delaycnt\_sel***

Selection bit for the width of pulse for a voltage zero-crossing event. When set to 0, the pulse is 32  $\mu$ s. When set to 1, the pulse is 256  $\mu$ s. When the *squarewave\_en* bit is set, this field is ignored. *delaycnt\_sel* is further described in Table 16.

**Table 16: *delaycnt\_sel***

Range	Value	Units
0	32	$\mu$ s
1	256	$\mu$ s

#### ***halfcycle\_en***

Setting for the zero crossing flag. When set to 0, the voltage zero-crossing will be indicated on every edge determined by *zercrossedgesel*. When set to 1, the voltage zero-crossing will be indicated on both rising and falling edges.

#### ***squarewave\_en***

Setting for the zero crossing flag. When set to 0, the zero-crossing event will be indicated by a pulse on the DIO pin. When set to 1, the zero-crossing event will be indicated by a level change on the DIO pin.

#### ***zercrossingchansel***

Determines which channel will trigger the zero crossing flag. 0 is the voltage channel. 1 is the current channel with zero crossing flag for rising and falling with only one customizable register *delaycnt\_sel*.

#### ***zercrossedgesel***

This determines whether the zero crossing flag triggers on rising or falling. Note: if *halfcycle\_en* = 1, this setting does not matter.

### Register 0x0F/0x1F

Bits	Name	Default Value	Description
8:2	<i>i2c_slv_addr</i>	127	I <sup>2</sup> C slave address selection
9	<i>i2c_dis_slv_addr</i>	0	Disable I <sup>2</sup> C slave address selection circuit
11:10	<i>dio_0_sel</i>	0	Digital output 0 multiplexor selection bits
13:12	<i>dio_1_sel</i>	0	Digital output 1 multiplexor selection bits
23:14	<i>n</i>	0	Sets the number of samples used in RMS calculations when <i>bypass_n_en</i> = 1
24	<i>bypass_n_en</i>	0	Set whether RMS is calculated based on voltage zero crossing or <i>n</i> samples from the above registers
31:26	<i>ecc</i>	–	Error Code Correction

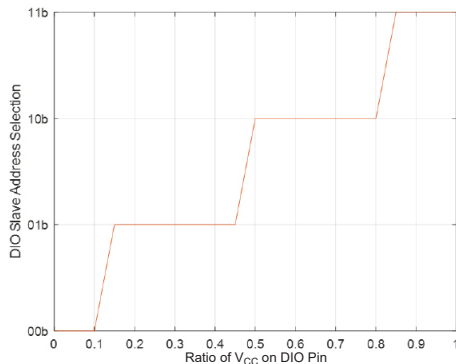
#### *i2c\_slv\_addr*

Settings for the I<sup>2</sup>C slave address externally. When *i2c\_dis\_slv\_addr* is set to 0, the voltage on the DIO pins are measured at power on and are used to set the device’s slave address.

Each DIO pin has 4 voltage “bins” which may be used to set the I<sup>2</sup>C slave address. These voltages may be set using resistor divider circuits from  $V_{CC}$  to GND. *i2c\_slv\_addr* is further described in Table 17.

Table 17: *i2c\_slv\_addr*

DIO_1 (decimal)	DIO_0 (decimal)	Slave Address (decimal)
0	0	96
0	1	97
0	2	98
0	3	99
1	0	100
1	1	101
1	2	102
1	3	103
2	0	104
2	1	105
2	2	106
2	3	107
3	0	108
3	1	109
3	2	110
3	3	EEPROM value



#### *i2c\_dis\_slv\_addr*

When *i2c\_dis\_slv\_addr* is set to 1, the address is set through EEPROM field *i2c\_slv\_addr*[6:0]. This enables or disables the analog I<sup>2</sup>C slave address feature at power on. When this bit is set, the I<sup>2</sup>C slave address will map directly to *i2c\_slv\_addr*.

#### *dio\_0\_sel*

Determines which flags are output on the DIO0 pin. Only used when the device is in I<sup>2</sup>C programming mode.

#### *dio\_1\_sel*

Determines which flags are output on the DIO1 pin. Only used when the device is in I<sup>2</sup>C programming mode.

### Volatile Memory

Address	Bits																																															
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
0x20	<i>irms</i>																<i>vrms</i>																															
0x21	<i>pimag</i>																<i>pactive</i>																															
0x22				<i>pospf</i>	<i>posangle</i>																												<i>papparent</i>															
0x23																																																
0x24																																																
0x25																																																
0x26	<i>irmsavgonesec</i>																<i>vrmsavgonesec</i>																															
0x27	<i>irmsavgonemin</i>																<i>vrmsavgonemin</i>																															
0x28																																																
0x29																																																
0x2A	<i>icodes</i>																<i>vcodes</i>																															
0x2B																																																
0x2C																	<i>pinstant</i>																															
0x2D																																																
0x2E																																																
0x2F	<i>access_code</i>																																															
0x30																																<i>customer_access</i>																
0x31																																																

VOLATILE



### Register Details – Volatile

#### Register 0x20

Bits	Name	Description
15:0	<i>vrms</i>	Voltage RMS value
31:16	<i>irms</i>	Current RMS value

##### *vrms*

RMS voltage output. This field is an unsigned 16-bit fixed point number with 16 fractional bits, where  $\Delta V_{IN(MAX)} = 0.84$ , and  $\Delta V_{IN(min)} = -0.84$ . To convert the value (input voltage) to line voltage, divide the input voltage by the  $R_{SENSE}$  and  $R_{ISO}$  voltage divider ratio using actual resistor values.

Table 18: *vrms*

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.84	$[0 \text{ to } \sim 1] \times \Delta V_{IN(MAX)} \times 1.19$	mV

##### *irms*

RMS current output. This field is a signed 16-bit fixed point number with 15 fractional bits, where  $I_{IP(MAX)} = 0.84$ , and  $I_{IP(MIN)} = -0.84$ .

Table 19: *irms*

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.84	$[0 \text{ to } \sim 1] \times I_{PR(MAX)} \times 1.19$	A

#### Register 0x21

Bits	Name	Description
15:0	<i>pactive</i>	Active power
31:16	<i>pimag</i>	Reactive power

##### *pactive*

Active power output. This field is a signed 16-bit fixed point number with 15 fractional bits, where positive MaxPow = 0.704, and negative MaxPow = -0.704. To convert the value (input power) to line power, divide the input power by the  $R_{SENSE}$  and  $R_{ISO}$  voltage divider ratio using actual resistor values.

Table 20: *pactive*

Register Range	Valid Range	Value	Units
-1 to ~1	-0.704 to ~0.704	$[1 \text{ to } \sim 1] \times \text{MaxPow} \times 1.42$	mW

##### *pimag*

Reactive power output. This field is an unsigned 16-bit fixed point number with 16 fractional bits, where MaxPow = 0.704. To convert the value (input power) to line power, divide the input power by the  $R_{SENSE}$  and  $R_{ISO}$  voltage divider ratio using actual resistor values.

Table 21: *pimag*

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.704	$[0 \text{ to } \sim 1] \times \text{MaxPow} \times 1.42$	mVA

### Register 0x22

Bits	Name	Description
15:0	<i>papparent</i>	Apparent power magnitude
26:16	<i>pfactor</i>	Power factor
27	<i>posangle</i>	Sign of the power angle
28	<i>pospf</i>	Sign of the power factor

#### *papparent*

Apparent power output magnitude. This field is an unsigned 16-bit fixed point number with 16 fractional bits, where  $\text{MaxPow} = 0.704$ . To convert the value (input power) to line power, divide the input power by the  $R_{\text{SENSE}}$  and  $R_{\text{ISO}}$  voltage divider ratio using actual resistor values.

Table 22: *papparent*

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.704	$[0 \text{ to } \sim 1] \times \text{MaxPow} \times 1.42$	mVAR

#### *pfactor*

Power factor output. This field is a signed 11-bit fixed point number with 10 fractional bits. It ranges from  $-1$  to  $\sim 1$  with a step size of  $2^{-10}$ . *pfactor* is further described in Table 23.

Table 23: *pfactor*

Range	Value	Units
$-1$ to $\sim 1$	$-1$ to $\sim 1$	–

### Register 0x25

Bits	Name	Description
9:0	<i>numptsout</i>	Number of samples of current and voltage used for calculations

#### *numptsout*

Number of points used in the *rms* calculation. This will be the dynamic value that is evaluated internal to the device based on full cycle zero crossings of the voltage channel. *numptsout* is further described in Table 24.

Table 24: *numptsout*

Range	Value	Units
0 to 1023	0 to 1023	samples

#### *posangle*

Bit to represent leading or lagging. A 0 represents the current leading and a 1 represents the current lagging.

#### *pospf*

Sign bit to represent if the power is being generated (0) or consumed (1).

### Register 0x26

Bits	Name	Description
15:0	<i>vrmsavgonesec</i>	Averaged voltage RMS value; duration set by <i>rms_avg_1</i> . This register will be zero if <i>iavgselectn</i> = 1
31:16	<i>irmsavgonesec</i>	Averaged current RMS value; duration set by <i>rms_avg_1</i> . This register will be zero if <i>iavgselectn</i> = 0

#### ***vrmsavgonesec***

Voltage RMS value averaged according to *rms\_avg\_1*. This register will be zero if *iavgselectn* = 1.

#### ***irmsavgonesec***

Current RMS value averaged according to *rms\_avg\_1*. This register will be zero if *iavgselectn* = 0.

### Register 0x27

Bits	Name	Description
15:0	<i>vrmsavgonemin</i>	Averaged voltage RMS value; duration set by <i>rms_avg_2</i> . This register will be zero if <i>iavgselectn</i> = 1
31:16	<i>irmsavgonemin</i>	Averaged current RMS value; duration set by <i>rms_avg_2</i> . This register will be zero if <i>iavgselectn</i> = 0

#### ***vrmsavgonemin***

Voltage RMS value averaged according to *rms\_avg\_2*. This register will be zero if *iavgselectn* = 1.

#### ***irmsavgonemin***

Current RMS value averaged according to *rms\_avg\_2*. This register will be zero if *iavgselectn* = 0.

### Register 0x28

Bits	Name	Description
15:0	<i>pactavgonesec</i>	Active Power value averaged over up to one second; duration set by <i>rms_avg_1</i>

#### ***pactavgonesec***

Active power value averaged according to *rms\_avg\_1*.

### Register 0x29

Bits	Name	Description
15:0	<i>pactavgonemin</i>	Active Power value averaged over up to one minute; duration set by <i>rms_avg_2</i>

#### ***pactavgonemin***

Active power value averaged according to *rms\_avg\_2*.

### Register 0x2A

Bits	Name	Description
15:0	<i>vcodes</i>	Instantaneous voltage measurement
31:16	<i>icodes</i>	Instantaneous current measurement

#### *vcodes*

This field contains the instantaneous voltage measurement before any RMS calculations are done. It is a 16-bit signed fixed point number with 15 fractional bits, where  $\Delta V_{IN(MAX)} = 0.84$  and  $\Delta V_{IN(MIN)} = -0.84$ . To convert the value (input voltage) to line voltage, divide the input voltage by the  $R_{SENSE}$  and  $R_{ISO}$  voltage divider ratio using the resistor values.

Table 25: *vcodes*

Register Range	Valid Range	Value	Units
-1 to ~1	-0.84 to ~0.84	$[-1 \text{ to } \sim 1] \times \Delta V_{IN(MAX)} \times 1.19$	mV

#### *icodes*

This field contains the instantaneous current measurement before any RMS calculations are done. This field is a signed 16-bit fixed point number with 15 fractional bits, where  $I_{IP(MAX)} = 0.84$ , and  $I_{IP(MIN)} = -0.84$ .

Table 26: *icodes*

Register Range	Valid Range	Value	Units
-1 to ~1	-0.84 to ~0.84	$[-1 \text{ to } \sim 1] \times I_{PR(MAX)} \times 1.19$	A

### Register 0x2C

Bits	Name	Description
15:0	<i>pinstant</i>	Instantaneous power – Multiplication of <i>vcodes</i> and <i>icodes</i>

#### *pinstant*

This field contains the instantaneous power measurement before any RMS calculations are done. This field is a signed 16-bit fixed point number with 15 fractional bits, where positive MaxPow = 0.704, and negative MaxPow = -0.704. To convert the value (input power) to line power, divide the input power by the  $R_{SENSE}$  and  $R_{ISO}$  voltage divider ratio using the resistor values.

Table 27: *pinstant*

Register Range	Valid Range	Value	Units
-1 to ~1	-0.704 to ~0.704	$[-1 \text{ to } \sim 1] \times \text{MaxPow} \times 1.42$	mVAR

### Register 0x2D

Bits	Name	Description
0	<i>zerocrossout</i>	Zero-crossing output
1	<i>faultout</i>	Current fault output
2	<i>faultlatched</i>	Current fault output latched
3	<i>overvoltage</i>	Overvoltage flag
4	<i>undervoltage</i>	Undervoltage flag

#### **zerocrossout**

Flag for the zero-crossing events. This will be present and active regardless of *DIO\_0\_sel* and *DIO\_1\_sel*. This flag will still follow the *halfcycle\_en* and *squarewave\_en* settings.

#### **faultout**

Flag for the overcurrent events. This will be present and active regardless of *DIO\_0\_sel* and *DIO\_1\_sel* and will only be set when *fault* is present.

#### **faultlatched**

Flag for the overcurrent events. This bit will latch and will remain 1 as soon as an overcurrent event is detected. This can be reset by writing a 1 to this field. This will be present and active regardless of DIO settings.

#### **overvoltage**

Flag for the overvoltage events. This will be present and active regardless of *DIO\_0\_sel* and *DIO\_1\_sel* and will only be set when *fault* is present.

#### **undervoltage**

Flag for the undervoltage events. This will be present and active regardless of *DIO\_0\_sel* and *DIO\_1\_sel* and will only be set when *fault* is present.

### Register 0x2F

Bits	Name	Description
31:0	<i>access_code</i>	Access code register: Customer code: 0x4F70656E

### Register 0x30

Bits	Name	Description
0	<i>customer_access</i>	Customer write access enabled. 0 = Non-Customer mode. 1 = Customer mode.

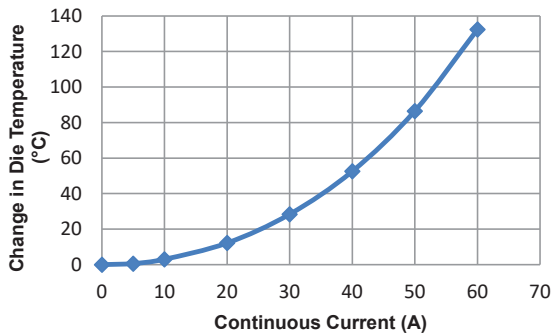
## THERMAL PERFORMANCE

### Thermal Rise vs. Primary Current

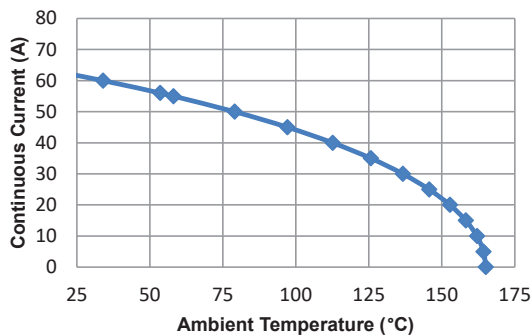
Self-heating due to the flow of current should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat as current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current, current “on-time”, and duty cycle. While the data presented in this section was collected with direct current (DC), these numbers may be used to approximate thermal response for both AC signals and current pulses.

The plot in Figure 31 shows the measured rise in steady-state die temperature of the ACS37800 versus continuous current at an ambient temperature,  $T_A$ , of 25 °C. The thermal offset curves may be directly applied to other values of  $T_A$ . Conversely, Figure 32 shows the maximum continuous current at a given  $T_A$ . Surges beyond the maximum current listed in Figure 32 are allowed given the maximum junction temperature,  $T_{J(MAX)}$  (165°C), is not exceeded.



**Figure 31: Self Heating in the MA Package Due to Current Flow**

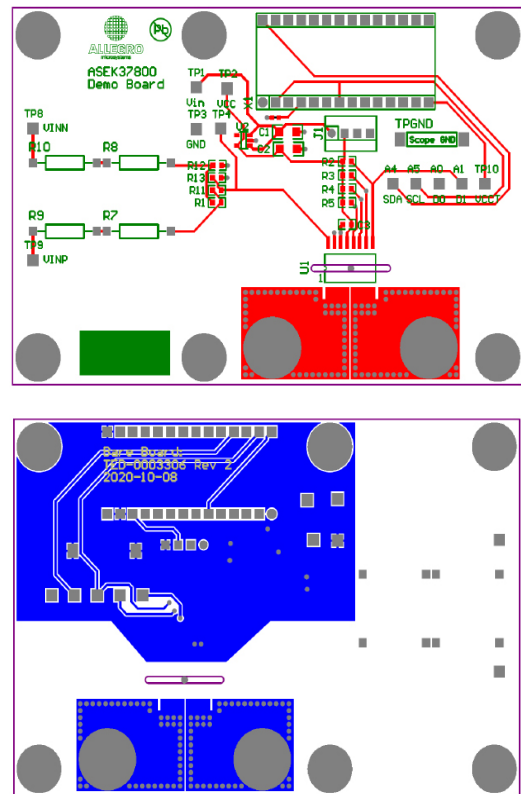


**Figure 32: Maximum Continuous Current at a Given  $T_A$**

The thermal capacity of the ACS37800 should be verified by the end user in the application’s specific conditions. The maximum junction temperature,  $T_{J(MAX)}$  (165°C), should not be exceeded. Further information on this application testing is available in the [DC and Transient Current Capability application note](#) on the Allegro website.

### ASEK37800 Evaluation Board Layout

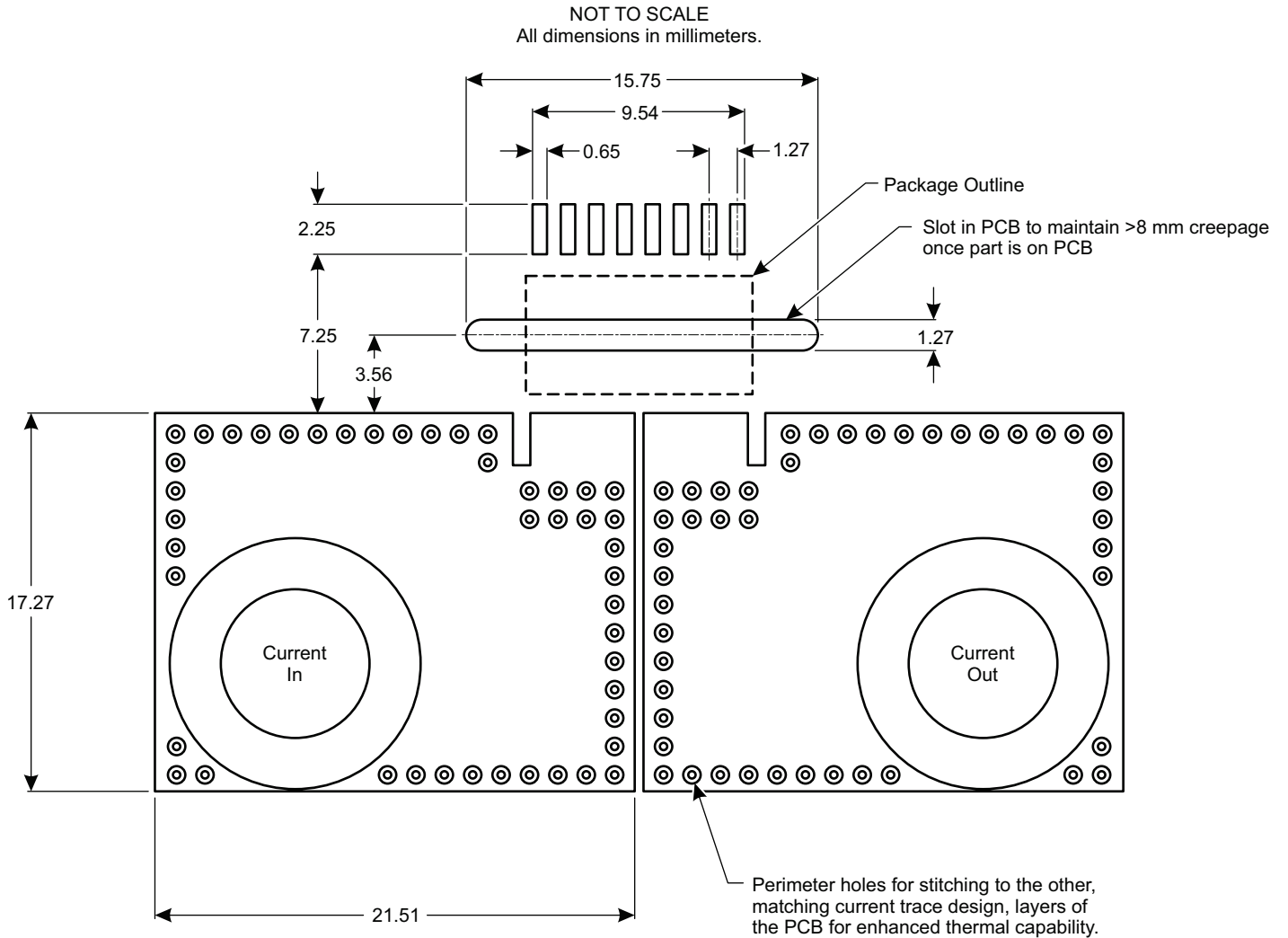
Thermal data shown in Figure 31 and Figure 32 was collected using the ASEK37800 Evaluation Board (TED-0003306). This board includes 750 mm<sup>2</sup> of 4 oz. copper (0.0694 mm) connected to pins 1 through 4, and to pins 5 through 8, with thermal vias connecting the layers. Top and Bottom layers of the PCB are shown below in Figure 33.



**Figure 33: Top and Bottom Layers for ASEK37800 Evaluation Board**

Gerber files for the ASEK37800 evaluation board are available for download from the Allegro website. See the technical documents section of the ACS37800 device webpage.

**RECOMMENDED PCB LAYOUT**



**Figure 34: Recommended PCB Layout**

## PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MS-013AA)

NOT TO SCALE

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

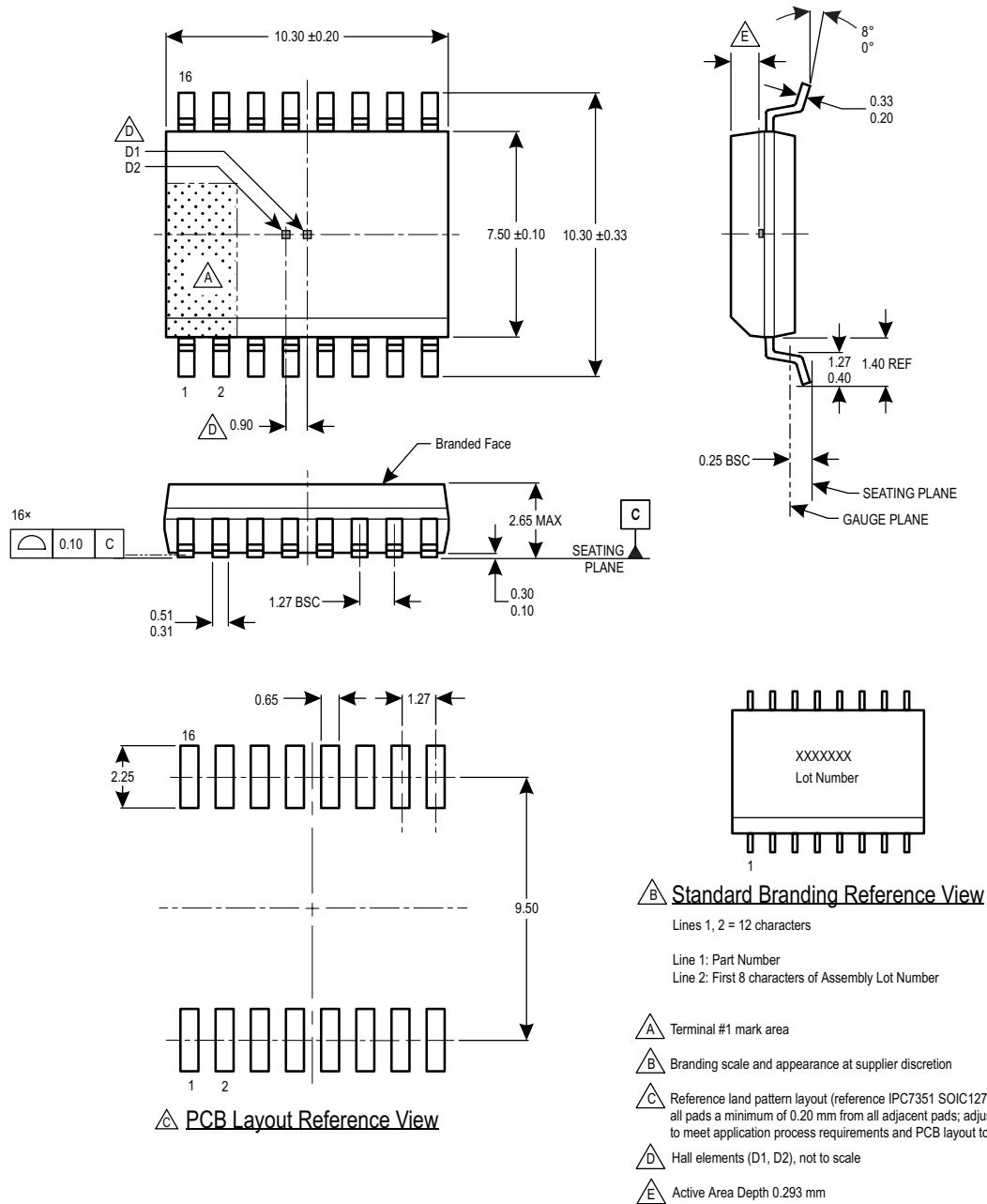


Figure 35: Package MA, 16-Pin SOICW



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# ACS37800

## Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

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### Revision History

Number	Date	Description
-	November 30, 2020	Initial release

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