0.7V to V_{CC}-1V, 4A 1ch Ultra Low Dropout Linear Regulator

BD3522EFV

General Description

BD3522EFV is an ultra low-dropout linear chipset regulator that operates from a very low input supply. It offers ideal performance in low input voltage to low output voltage applications. The input-to-output voltage difference is minimized by using a built-in N-Channel power MOSFET with a maximum ON-Resistance of R_{ON} =50mΩ(Max). By lowering the dropout voltage, the regulator achieves high output current of up to (I_{OUTMAX}=4.0A), thereby, reducing conversion loss, making it comparable to a switching regulator and its power transistor, choke coil, and rectifier diode constituents. BD3522EFV is a low-cost design and is available in significantly downsized package profiles. The external resistor allows the entire range of output voltage configurations between 0.65V and 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to a required power supply sequence.

Features

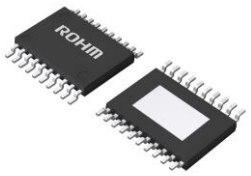
- Internal High-Precision Reference Voltage Circuit (0.65V±1%)
- Built-in VCC Undervoltage Lockout Circuit (V_{CC}=3.80V)
- NRCS (Soft start) Function Reduces the Magnitude of In-rush Current
- Internal N-Channel MOSFET Driver Offers Low ON-Resistance
- Built-in Short Circuit Protection (SCP)
- Built-in Current Limit Circuit (4.0A min)
- Built-in Thermal Shutdown (TSD) Circuit
- Tracking Function

Key Specifications

- IN Input Voltage Range: 0.7V to V_{CC}-1V
- VCC Input Voltage Range: 4.3V to 5.5V
- Output voltage range: 0.65V to 2.7V
- Output Current: 4.0A (Max)
- ON-Resistance: 28mΩ(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -10°C to +100°C

Package

W(Typ) x D(Typ) x H(Max)

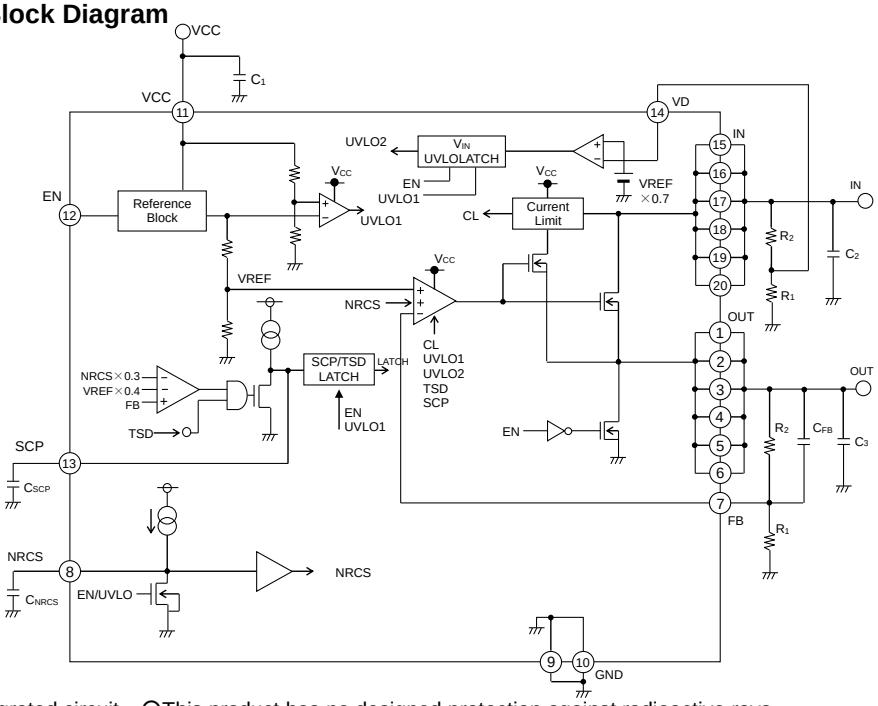


HTSSOP-B20
6.50mm x 6.40mm x 1.00mm

Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

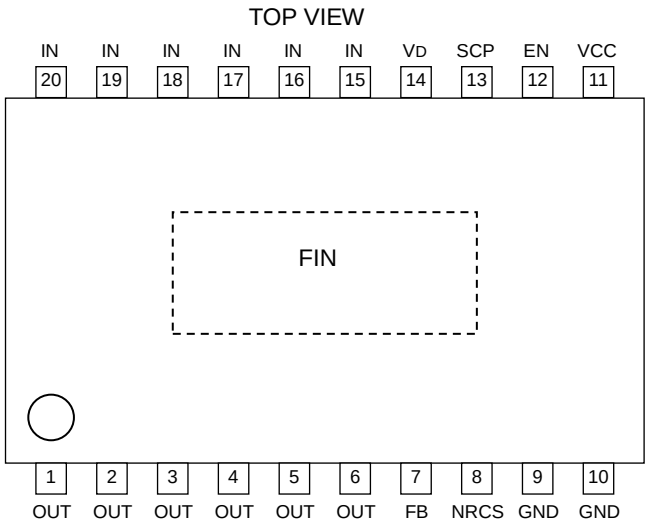
Typical Application Circuit and Block Diagram



○Product structure：Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration



Pin Descriptions

Pin No.	Pin name	Pin Function
1	OUT	Output voltage pin
2	OUT	Output voltage pin
3	OUT	Output voltage pin
4	OUT	Output voltage pin
5	OUT	Output voltage pin
6	OUT	Output voltage pin
7	FB	Reference voltage feedback pin
8	NRCS	In-rush current protection (NRCS) capacitor connection pin
9	GND	Ground pin
10	GND	Ground pin
11	VCC	Power supply pin
12	EN	Enable input pin
13	SCP	SCP delay time setting capacitor connection pin
14	VD	IN input voltage detect pin
15	IN	Input voltage pin
16	IN	Input voltage pin
17	IN	Input voltage pin
18	IN	Input voltage pin
19	IN	Input voltage pin
20	IN	Input voltage pin
-	FIN	Connected to heatsink and GND

Description of Blocks

1. AMP
   This is an error amp that compares the reference voltage (0.65V) with FB voltage to drive the output N-Channel FET. Frequency optimization aids in attaining rapid transient response, and to support the use of ceramic capacitors on the output. AMP output voltage ranges from GND to VCC. When EN is OFF, or when UVLO is active, output goes LOW and the output of the N-Channel FET switches OFF state.

2. EN
   The EN block controls the ON and OFF state of the regulator via the EN logic input pin. During OFF state, circuit voltage stabilizes at 0μA which minimizes the current consumption during standby mode. The FET is switched ON to enable the discharge of the NRCS and OUT, thereby draining the excess charge and preventing the load side of an IC from malfunctioning. Since there is no electrical connection required (e.g. between the VCC pin and the ESD prevention diode), module operation is independent of the input sequence.

3. VCCUVLO
   To prevent malfunctions that can occur during a sudden decrease in VCC, the UVLO circuit switches the output to OFF state, and (like the EN block) discharges NRCS and OUT. Once the UVLO threshold voltage (TYP3.80V) is reached, the power-on reset is triggered and output is restored.

4. VDUVLO
   VD pin is the IN voltage detect pin. When VD voltage exceeds the threshold voltage, VDUVLO becomes active. Once active, the status of output voltage remains ON even if VD voltage drops. (When IN voltage drops, SCP engages and output switches OFF.) Unlike EN and VCC, it is active at output startup. VDUVLO can be restored either by reconnecting the EN pin or VCC pin.

5. CURRENT LIMIT
   During ON state, the current limit function monitors the output current of the IC against the current limit value. When the output current exceeds this value, this block lowers the output current to protect the load of the IC. When it overcomes the overcurrent state, output voltage is restored to the normal value. However when the output voltage falls below the SCP startup voltage, the SCP function becomes active and the output switches OFF.

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Description of Blocks –continued

6. NRCS (Non Rush Current on Start-up)
The soft start function enabled by connecting an external capacitor between the NRCS pin and GND. Output ramp-up can be set for any period up to the time the NRCS pin reaches V_{FB} (0.65V). During startup, the NRCS pin serves as a 20μA (TYP) constant current source to charge the external capacitor. Output start time is calculated by the formula below.

$$t_{NRCS}(typ) = \frac{C_{NRCS} \times V_{FB}}{I_{NRCS}}$$

7. TSD (Thermal Shut down)
The shutdown (TSD) circuit is automatically latched OFF when the chip temperature exceeds the threshold temperature after the programmed time period elapses, thus protecting the IC against “thermal runaway” and heat damage. Since the TSD circuit is designed only to shut down the IC in the occurrence of extreme heat, it is important that the Tj (max) parameter should not be exceeded in the thermal design, in order to avoid potential problems with the TSD.

$$t_{TSD}(typ) = \frac{C_{SCP} \times V_{SCPTH}}{20\mu A}$$

8. IN
The IN line acts as the major current supply line, and is connected to the output N-Channel FET drain. Since there is no electrical connection (such as between the VCC pin and the ESD protection diode) required, IN operates independent of the input sequence. However, since an output N-Channel FET body diode exists between IN and OUT, a V_{IN}-V_{OUT} electric (diode) connection is present. Therefore, when output is switched ON or OFF, reverse current may flow from OUT to IN.

9. SCP
When output voltage (OUT) drops, the IC assumes that OUT pin is shorted to GND and switches the output voltage OFF. After the GND short has been detected and the programmed delay time has elapsed, the output is latched OFF. SCP is also effective during output startup. SCP condition can be cleared either by reconnecting the EN pin or VCC pin. Delay time is calculated by the formula below.

$$t_{SCP}(typ) = \frac{C_{SCP} \times V_{SCPTH}}{I_{SCP}}$$

Absolute Maximum Ratings（Ta=25°C）

Parameter	Symbol	Limit	Unit
Input Voltage 1	V_{CC}	6.0 (Note 1)	V
Input Voltage 2	V_{IN}	6.0 (Note 1)	V
Maximum Output Current	I_{OUT}	4(Note 1)	A
Enable Input Voltage	V_{EN}	6.0	V
Power Dissipation 1	Pd1	1.00 (Note 2)	W
Power Dissipation 2	Pd2	1.45 (Note 3)	W
Power Dissipation 3	Pd3	2.31 (Note 4)	W
Power Dissipation 4	Pd4	3.20 (Note 5)	W
Operating Temperature Range	Topr	-10 to +100	°C
Storage Temperature Range	Tstg	-55 to +125	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Should not exceed Pd.
(Note 2) Derate by 8mW/°C for Ta above 25°C (when mounted on a 70mm x 70mm x 1.6mm glass-epoxy board, no copper foil area)
(Note 3) Derate by 11.6mW/°C for Ta above 25°C (when mounted on a 70mm x 70mm x 1.6mm glass-epoxy board, 2-layer, copper foil area : 15mm x 15mm)
(Note 4) Derate by 18.5mW/°C for Ta above 25°C (when mounted on a 70mm x 70mm x 1.6mm glass-epoxy board, 2-layer, copper foil area : 70mm x 70mm)
(Note 5) Derate by 25.6mW/°C for Ta above 25°C (when mounted on a 70mm x 70mm x 1.6mm glass-epoxy board, 4-layer, copper foil area : 70mm x 70mm)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

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Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating		Unit
		Min	Max	
Input Voltage 1	V_{CC}	4.3	5.5	V
Input Voltage 2	V_{IN}	0.7	V_{CC}-1 (Note 6)	V
Output Voltage Setting Range	V_{OUT}	V_{FB}	2.7	V
Enable Input Voltage	V_{EN}	-0.3	+5.5	V
NRCS Capacitance	C_{NRCS}	0.001	1	μF

(Note 6) VCC and IN do not have to be implemented in the order listed.

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{CC}=5V, V_{EN}=3V, V_{IN}=1.7V, R_1=3.9kΩ, R_2=3.3kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Bias Current	I_{CC}	-	1.4	2.2	mA	
VCC Shutdown Mode Current	I_{ST}	-	0	10	μA	V_{EN}=0V
Output Current	I_{OUT}	4.0	-	-	A	
Feedback Voltage 1	V_{FB1}	0.643	0.650	0.657	V	
Feedback Voltage 2	V_{FB2}	0.637	0.650	0.663	V	Tj=-10°C to +100°C
Line Regulation 1	REG.I1	-	0.1	0.5	%/V	V_{CC}=4.3V to 5.5V
Line Regulation 2	REG.I2	-	0.1	0.5	%/V	V_{IN}=1.2V to 3.3V
Load Regulation	REG.L	-	0.5	10	mV	I_{OUT}=0A to 4A
Output ON-Resistance	R_{ON}	-	28	50	mΩ	I_{OUT}=4A,V_{IN}=1.2V Tj=-10°C to +100°C
Standby Discharge Current	I_{DEN}	1	-	-	mA	V_{EN}=0V, V_{OUT}=1V
[ENABLE]						
Enable Pin Input Voltage High	V_{ENHIGH}	2	-	-	V	
Enable Pin Input Voltage Low	V_{ENLOW}	-0.2	-	+0.8	V	
Enable Input Bias Current	I_{EN}	-	6	10	μA	V_{EN}=3V
[FEEDBACK]						
Feedback Pin Bias Current	I_{FB}	-100	0	+100	nA	
[NRCS]						
NRCS Charge Current	I_{NRCS}	12	20	28	μA	
NRCS Standby Voltage	V_{STB}	-	0	50	mV	V_{EN}=0V
[UVLO]						
VCC Undervoltage Lockout Threshold Voltage	V_{CCUVLO}	3.5	3.8	4.1	V	VCC: Sweep-up
VCC Undervoltage Lockout Hysteresis Voltage	V_{CCHYS}	100	160	220	mV	VCC: Sweep-down
VD Undervoltage Lockout Threshold Voltage	V_{DUVLO}	V_{REF} x 0.6	V_{REF} x 0.7	V_{REF} x 0.8	V	VD: Sweep-up
[SCP]						
SCP Start up Voltage	V_{OUTSCP}	V_{OUT} x 0.3	V_{OUT} x 0.4	V_{OUT} x 0.5	V	
SCP Threshold Voltage	V_{SCPTH}	1.05	1.15	1.25	V	
Charge Current	I_{SCP}	2	4	6	μA	
Standby Voltage	$V_{SCPSTBY}$	-	-	50	mV	

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Typical Waveforms

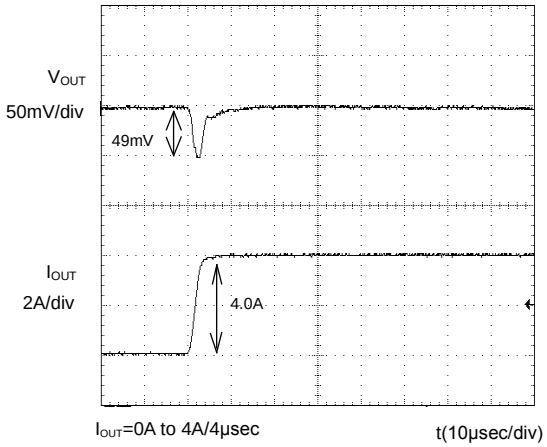


Figure 1. Transient Response
(0A to 4A)
C_{OUT}=22μF, C_{FB}=1000pF

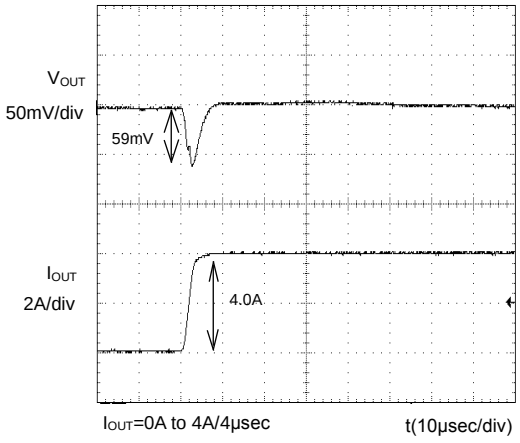


Figure 2. Transient Response
(0A to 4A)
C_{OUT}=100μF

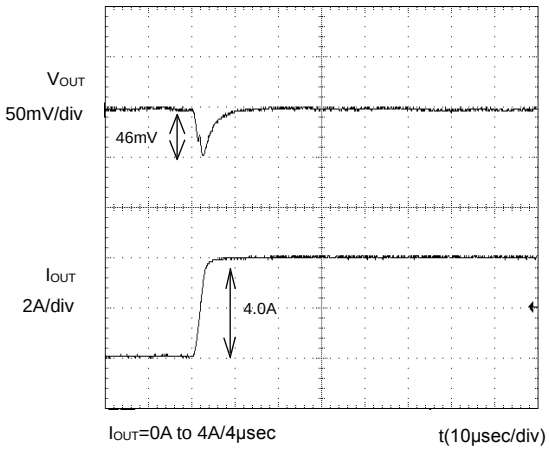


Figure 3. Transient Response
(0A to 4A)
C_{OUT}=100μF, C_{FB}=1000pF

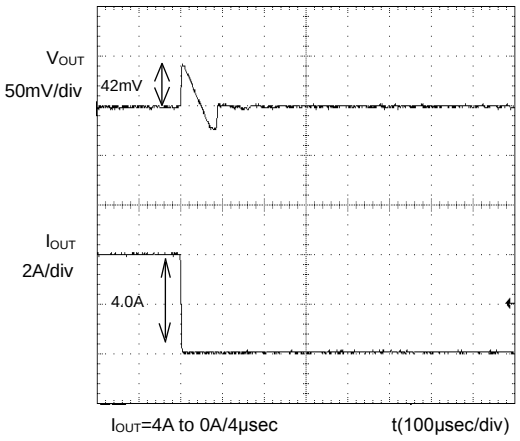


Figure 4. Transient Response
(4A to 0A)
C_{OUT}=22μF, C_{FB}=1000pF

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Typical Waveforms – continued

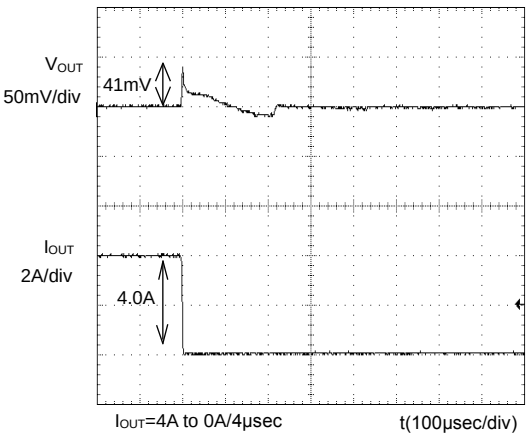


Figure 5. Transient Response
(4A to 0A)
C_{OUT}=100μF

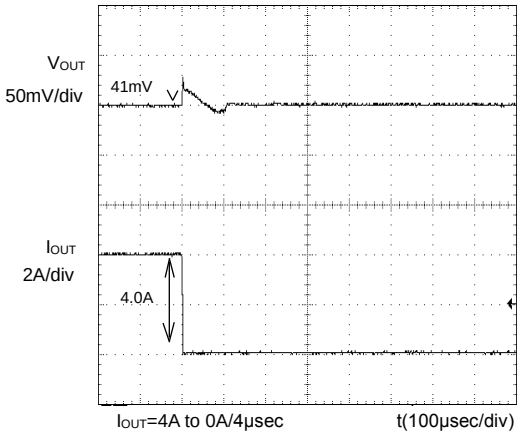


Figure 6. Transient Response
(4A to 0A)
C_{OUT}=100μF, C_{FB}=1000pF

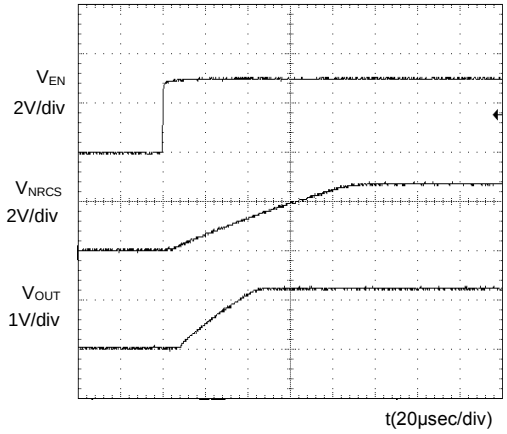


Figure 7. Waveform at Output Start

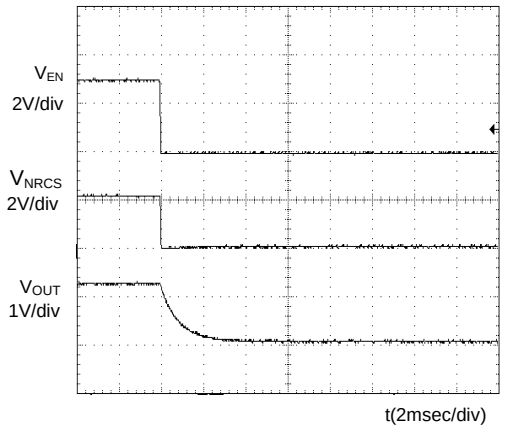


Figure 8. Waveform at Output OFF

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Typical Waveforms – continued

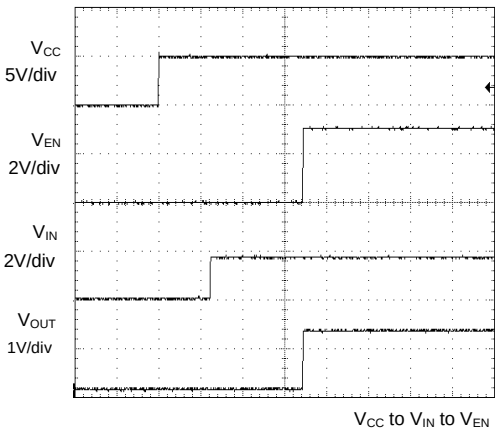


Figure 9. Input Sequence

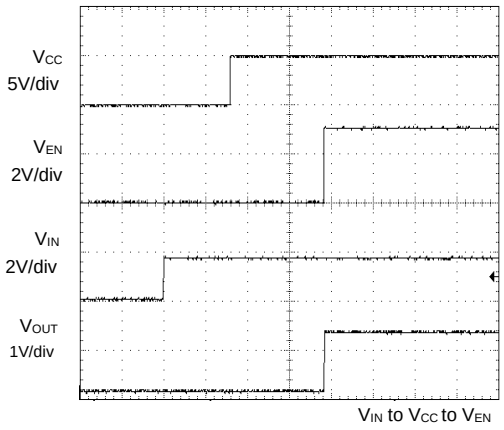


Figure 10. Input Sequence

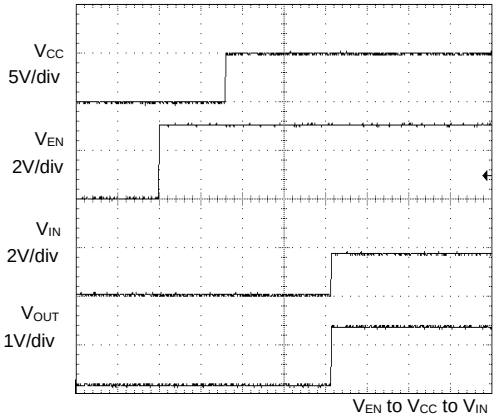


Figure 11. Input Sequence

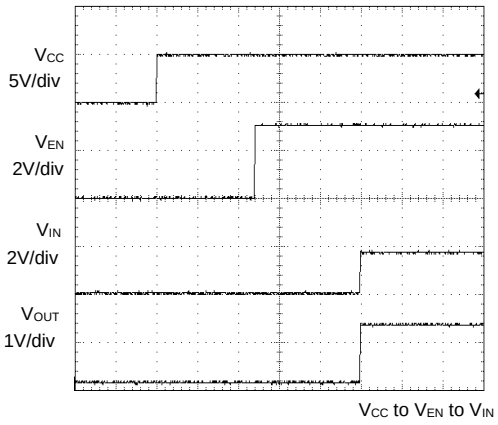


Figure 12. Input Sequence

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Typical Waveforms – continued

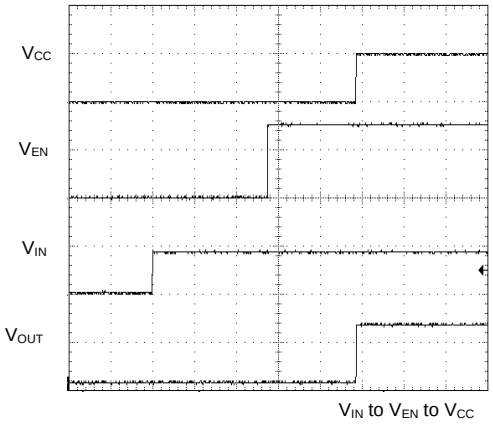


Figure 13. Input Sequence

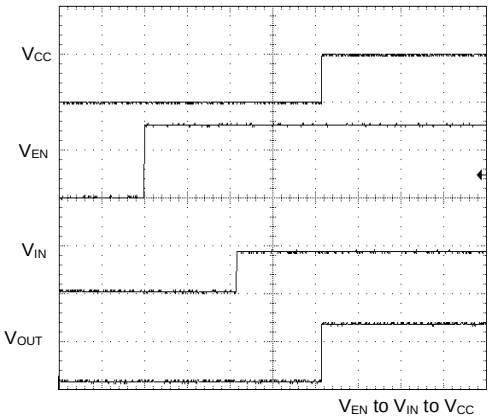


Figure 14. Input Sequence

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Typical Performance Curves

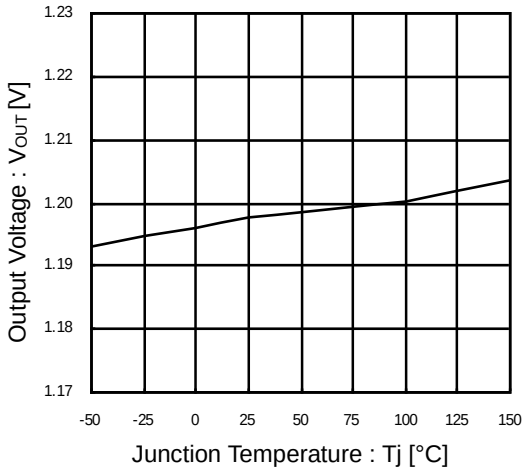


Figure 15. Output Voltage vs Junction Temperature

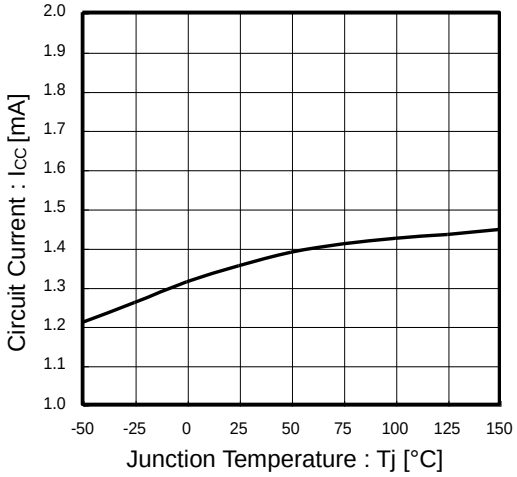


Figure 16. Circuit Current vs Junction Temperature

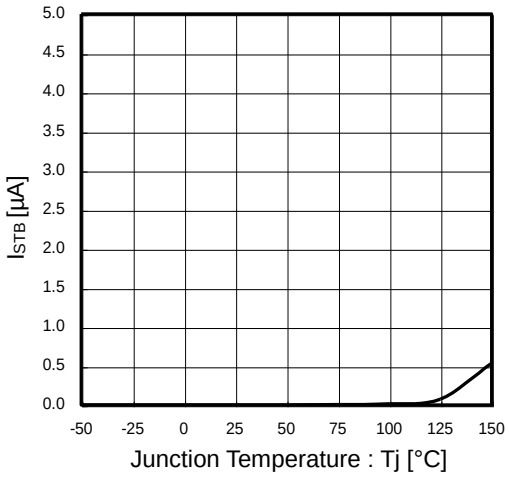


Figure 17. I_{STB} vs Junction Temperature

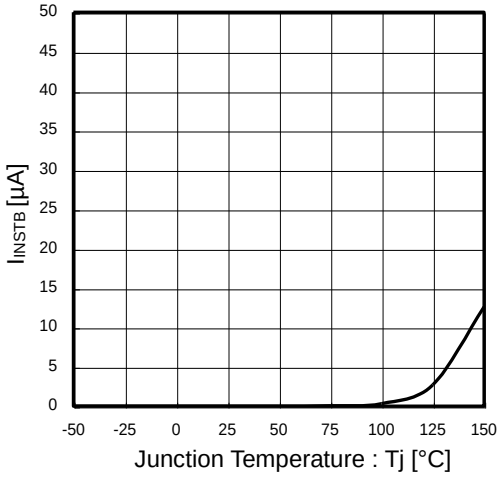


Figure 18. I_{INSTB} vs Junction Temperature

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Typical Performance Curves – continued

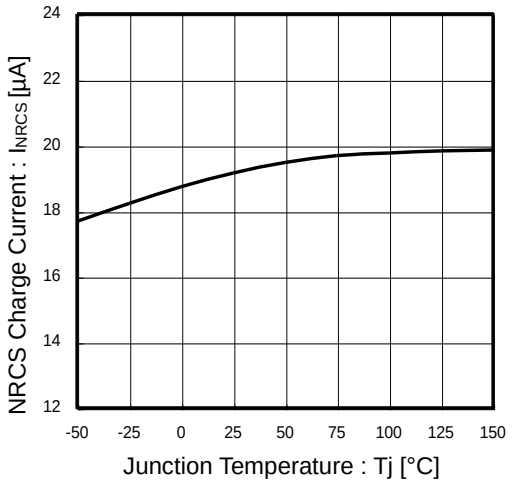


Figure 19. NRCS Charge Current vs Junction Temperature

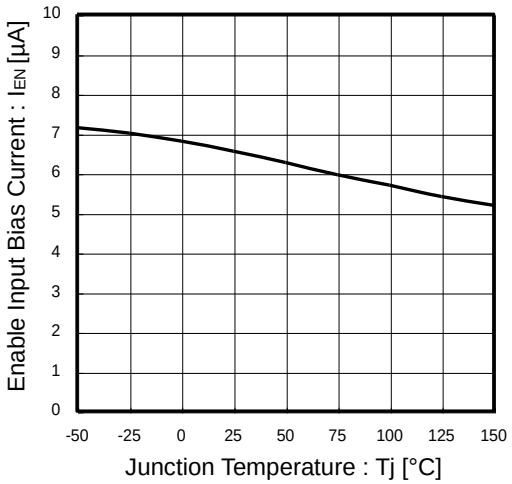


Figure 20. Enable Input Bias Current vs Junction Temperature

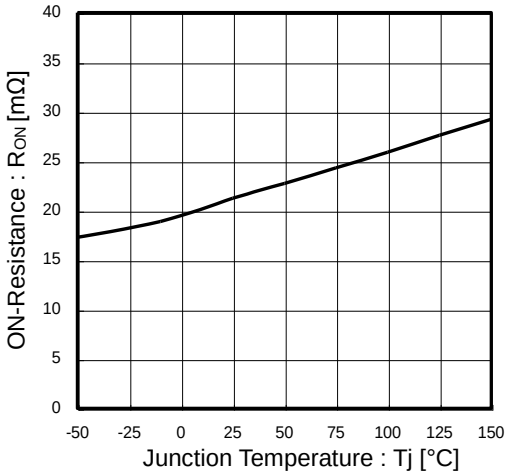


Figure 21. ON-Resistance vs Junction Temperature
(V_{CC}=5V/V_{OUT}=1.2V)

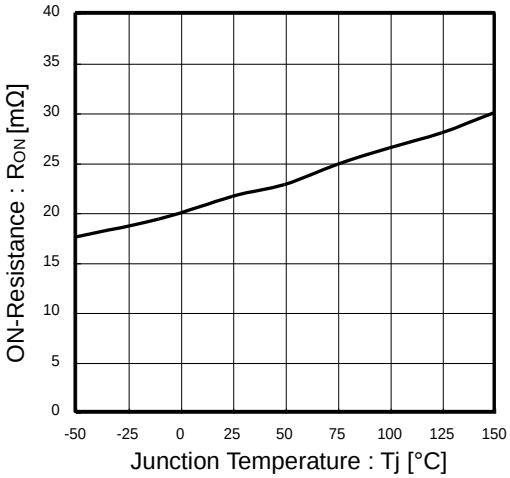


Figure 22. ON-Resistance vs Junction Temperature
(V_{CC}=5V/V_{OUT}=1.5V)

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Typical Performance Curves – continued

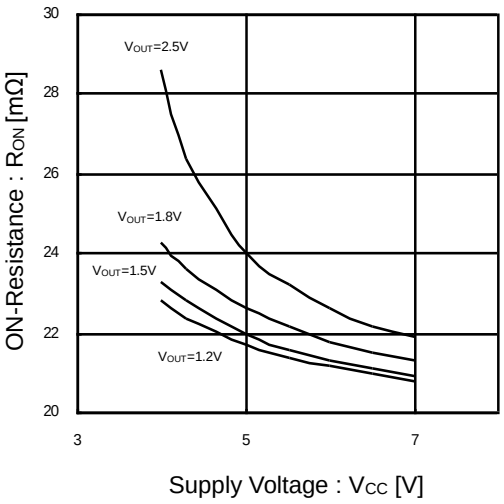
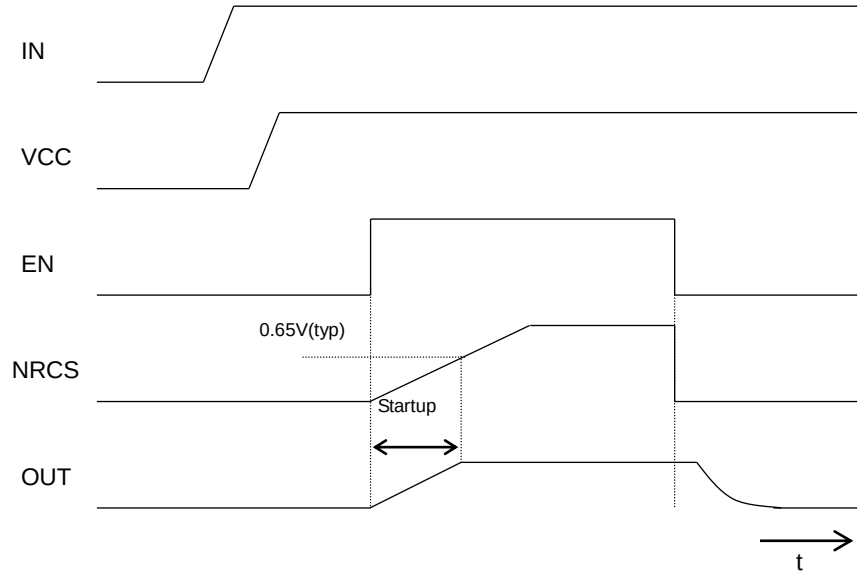


Figure 23. ON-Resistance vs Supply Voltage

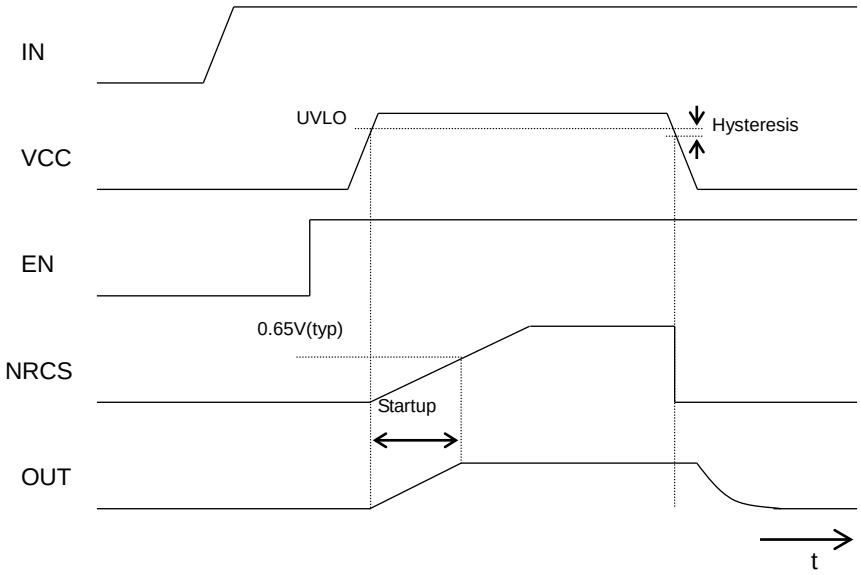
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Timing Chart

EN ON/OFF



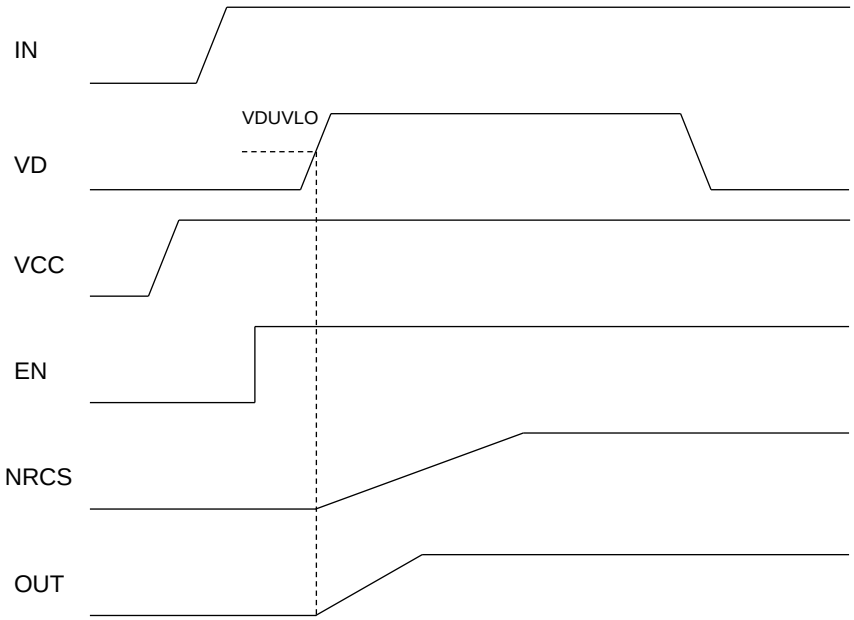
VCC ON/OFF



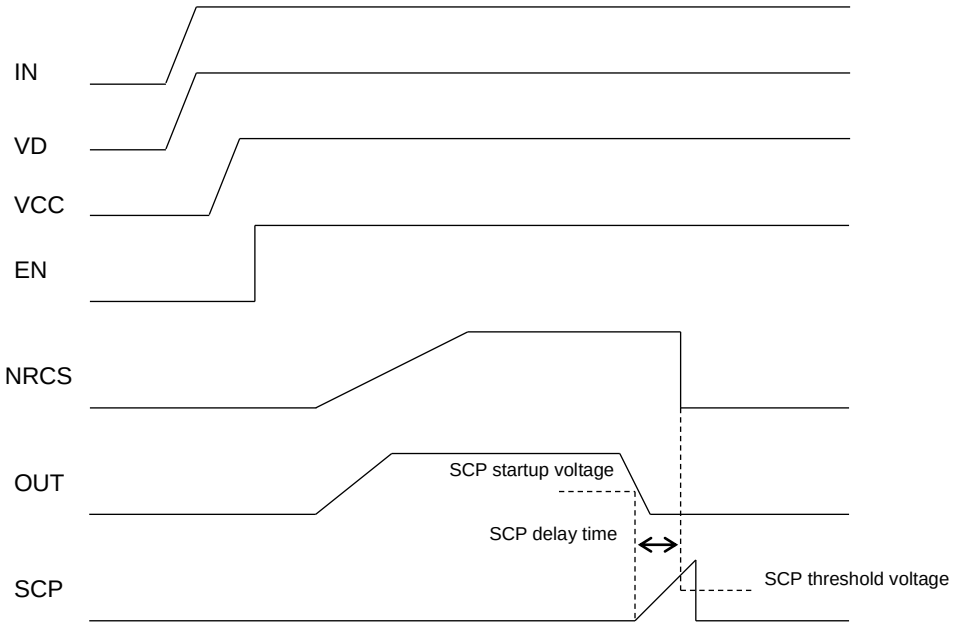
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Timing Chart - continued

VD ON



SCP OFF

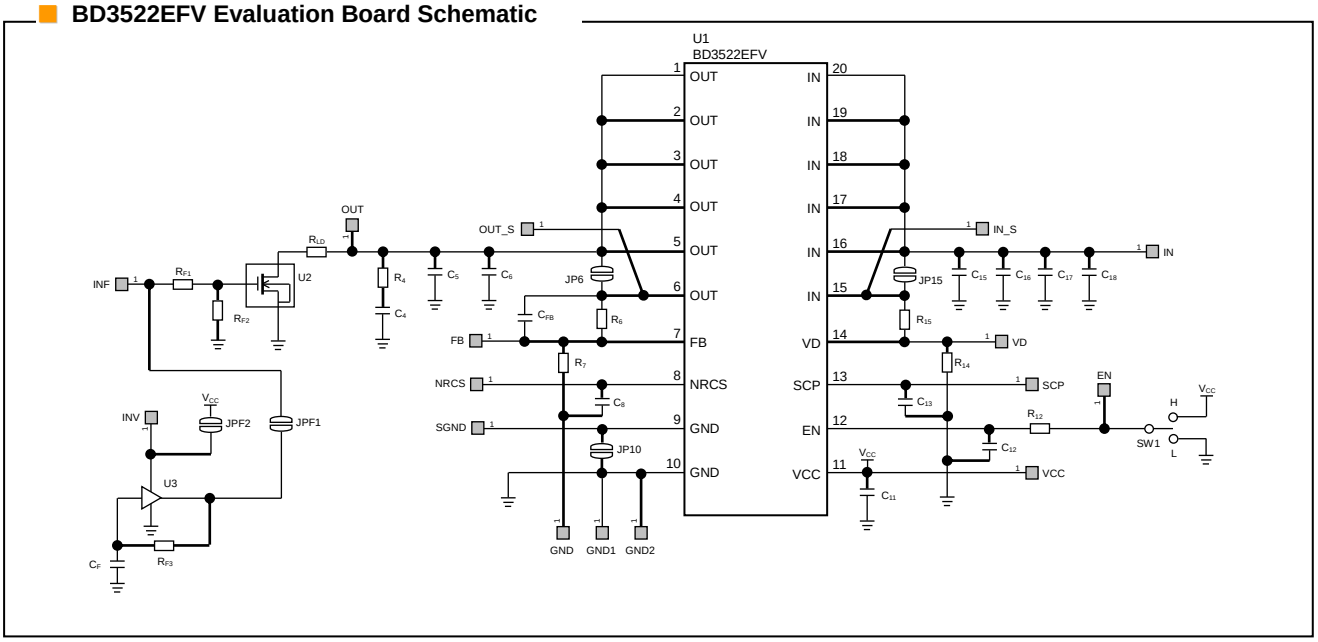


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Application Information

1. Evaluation Board

BD3522EFV Evaluation Board Schematic



BD3522EFV Evaluation Board List

Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD3522EFV
C_6	22µF	KYOCERA	CM316B226M06A
C_8	0.01µF	MURATA	GRM188B11H103KD
C_{11}	1µF	MURATA	GRM188B11A105KD
C_{13}	330pF	MURATA	GRM188B11H331KD
C_{15}	10µF	KYOCERA	CM21B106M06A
C_{18}(Note 1)	150µF	SANYO	6TPB150M

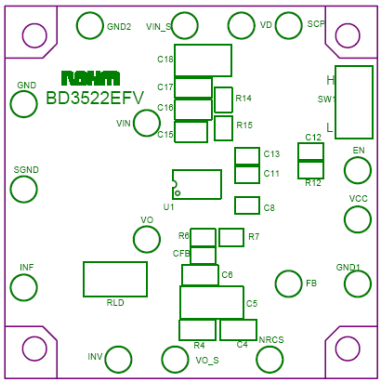
Component	Rating	Manufacturer	Product Name
C_{FB}	1000pF	MURATA	GRM188B11H102KD
R_6 (@V_{OUT}=1.2V)	3.3kΩ	ROHM	MCR03EZPF3301
R_7	3.9kΩ	ROHM	MCR03EZPF3901
R_{12}	0Ω	-	jumper
R_{14}	3.9kΩ	ROHM	MCR03EZPF3901
R_{15}(@V_{OUT}=1.2V)	3.3kΩ	ROHM	MCR03EZPF3301

(Note 1) provision for supply impedance of instruments

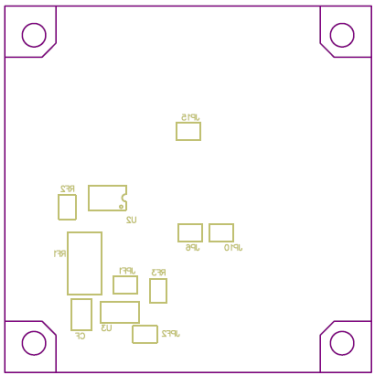
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BD3522EFV Evaluation Board Layout

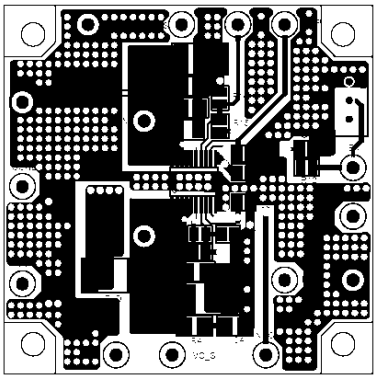
Silk Screen (Top)



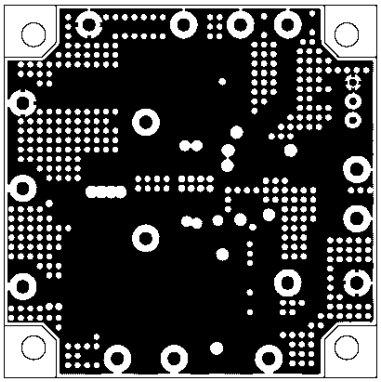
Silk Screen (Bottom)



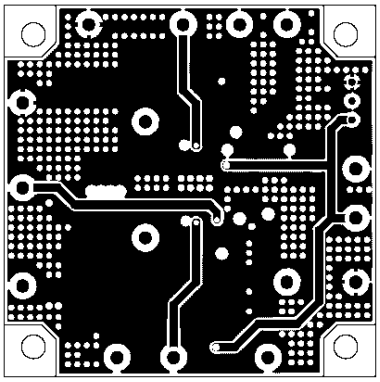
TOP Layer



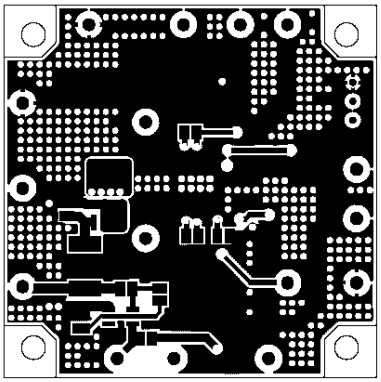
Middle Layer_1



Middle Layer_2

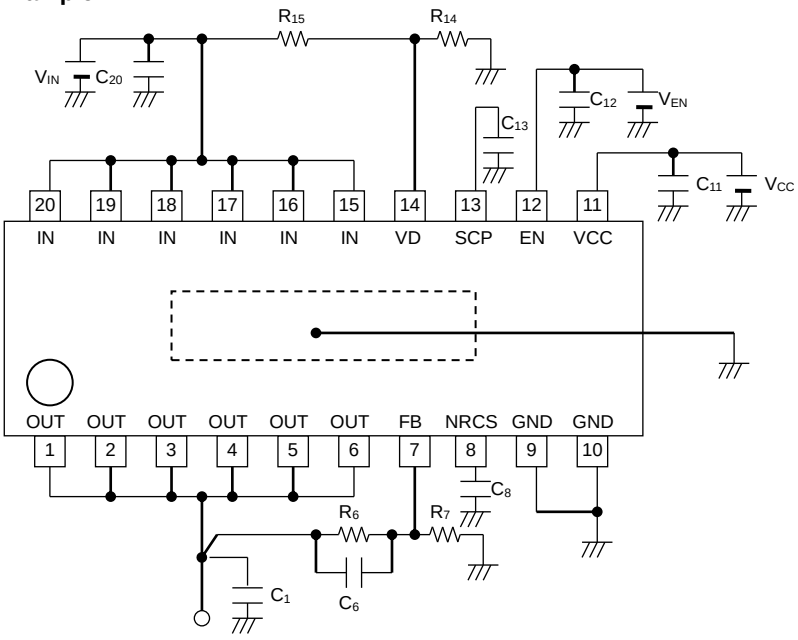


Bottom Layer



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2. Recommended Circuit Example



Component	Recommended Value	Programming Notes and Precautions
R_6/R_7	3.3k /3.9k	IC output voltage can be set with a configuration formula V_{FB} X (R_6+R_7) / R_7 using the values for the internal reference output voltage (V_{FB}) and the output voltage resistors (R_6, R_7). Select resistance values that will avoid the impact of the FB bias current (±100nA). The recommended total resistance value is 10KΩ.
C_1	22µF	To ensure output voltage stability, make sure that the output capacitors are connected between OUT pin and GND. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22µF ceramic capacitor is recomended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. Please confirm operation across a variety of temperature and load conditions.
C_{11}/C_{20}	1µF/10µF	Input capacitors reduce the output impedance of the voltage supply source connected to the input pins (VCC, IN). If the impedance of this power supply were to increase, input voltage (V_{CC}, V_{IN}) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 1µF/10µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C_8	0.01µF	The Non-Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (IN to OUT) and affects output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or when the UVLO function is deactivated. The temporary reference voltage is proportional to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportional to this reference voltage. Capacitors with low susceptibility to temperature are recommended, to ensure a stable soft-start time.
C_6	1000pF	This component is employed when the C_1 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.
C_{13}	330pF	The Short Circuit Protection (SCP) function and the Thermal Shut Down (TSD) function are built into the IC. Constant current comes from the SCP pin when SCP function or TSD function is operated. (SCP:4µA, TSD:20µA TYP) When the voltage at SCP pin exceeds the threshold voltage, the output of voltage becomes OFF. Capacitors with low susceptibility to temperature (330pF or more) are recommended, in order to assure a stable TSD delay setting time. Please confirm operation with the capacitor value to prevent defective startup.

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3. Heat Loss

In thermal design, consider the temperature range wherein the IC is guaranteed to operate and apply appropriate margins. The temperature conditions that need to be considered are listed below:

(1) Ambient temperature Ta can be no higher than 100°C.
(2) Chip junction temperature (Tj) can be no higher than 150°C.

Chip junction temperature can be determined as follows:

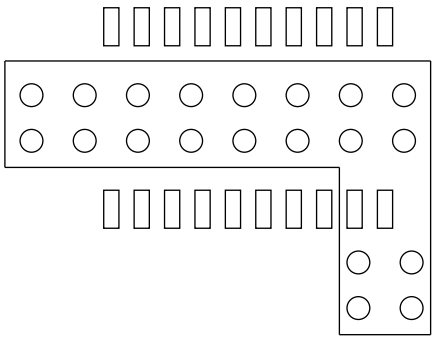
① Calculation based on ambient temperature (Ta)

$$Tj = Ta + \theta j - a \times W$$

<Reference values>

θj-a: HTSSOP-B20
125°C/W 1-layer substrate (no copper foil area)
86.2°C/W 2-layer substrate (copper foil area : 15mm x 15mm)
54.1°C/W 2-layer substrate (copper foil area : 70mm x 70mm)
39.1°C/W 4-layer substrate (copper foil area : 70mm x 70mm)
Substrate size: 70 x 70 x 1.6mm^3 (substrate with thermal via)

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). This package is so small (size: 6.5mm x 6.4mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and increasing the number of VIA as shown in the figure below, enable to achieve superior heat radiation characteristic. (This figure is an image only. It is recommended that the VIA size and number are designed suitable for the actual situation.).



Most of the heat loss in the BD3522EFV occurs at the output N-Channel FET. Power loss is determined by the total V_{IN}-V_{OUT} voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the IN and OUT in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD3522EFV) make sure to factor in conditions such as substrate size into the thermal design.

Power consumption (W) = { Input voltage (V_{IN}) - Output voltage (V_{OUT}) } x I_{OUT}(Ave)

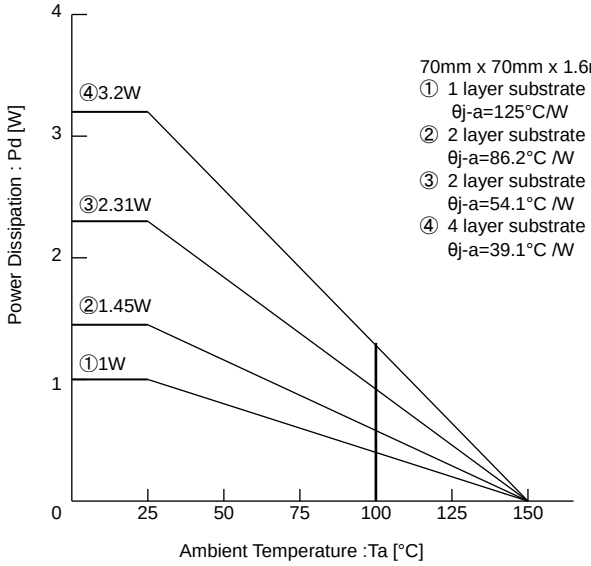
Example) Where V_{IN}=1.7V, V_{OUT}=1.2V, I=(Ave) = 4A,

$$\text{Power consumption}(W) = \{1.7(V) - 1.2(V)\} \times 4.0(A)$$
$$= 2.0(W)$$

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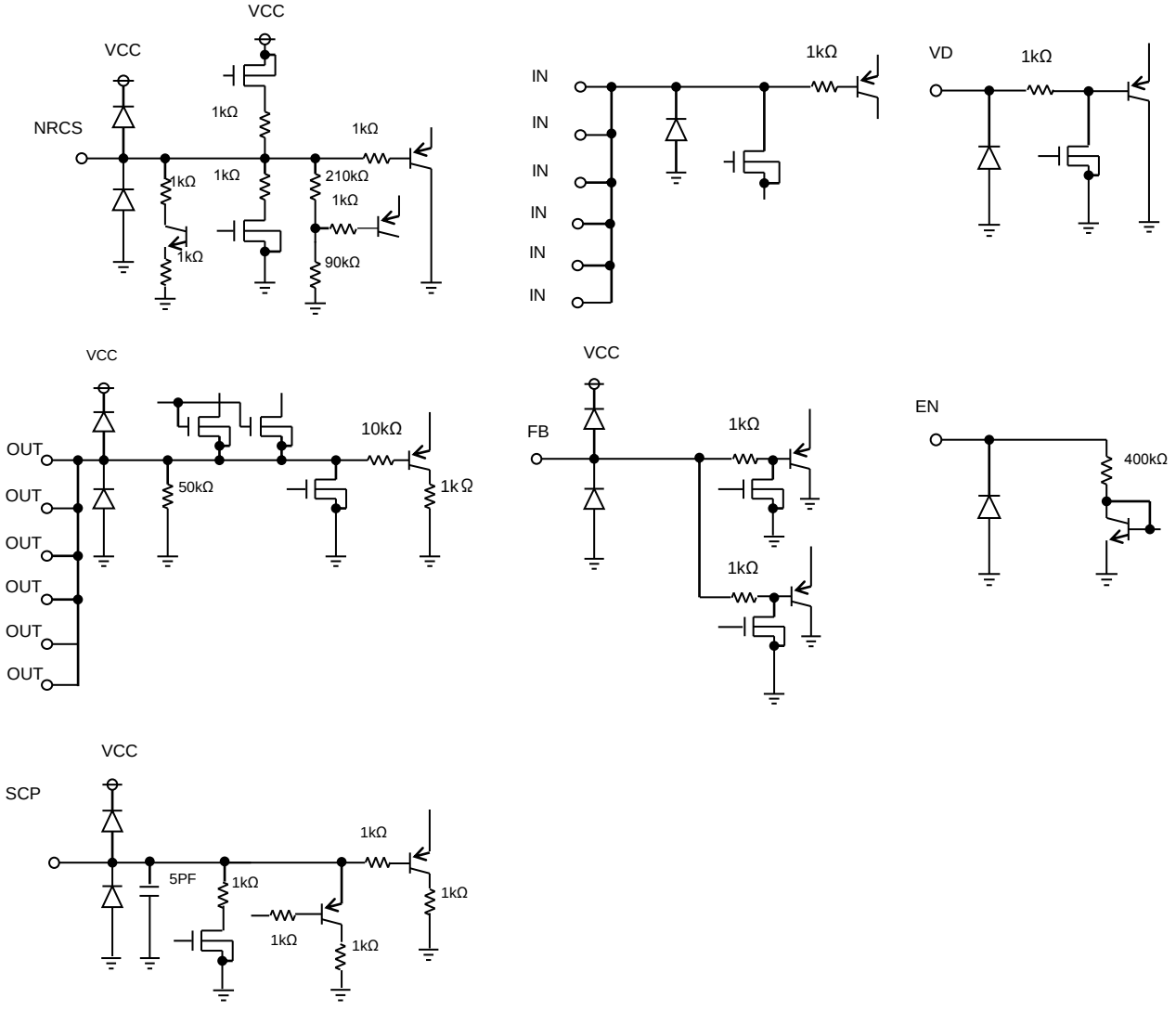
Power Dissipation

◎HTSSOP-B20



70mm x 70mm x 1.6mm (PCB with Thermal Via)
① 1 layer substrate (substrate surface copper foil area:0mm x 0mm)
θj-a=125°C/W
② 2 layer substrate (substrate surface copper foil area:15mm x 15mm)
θj-a=86.2°C /W
③ 2 layer substrate (substrate surface copper foil area:70mm x 70mm)
θj-a=54.1°C /W
④ 4 layer substrate (substrate surface copper foil area:70mm x 70mm)
θj-a=39.1°C /W

I/O Equivalent Circuits



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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

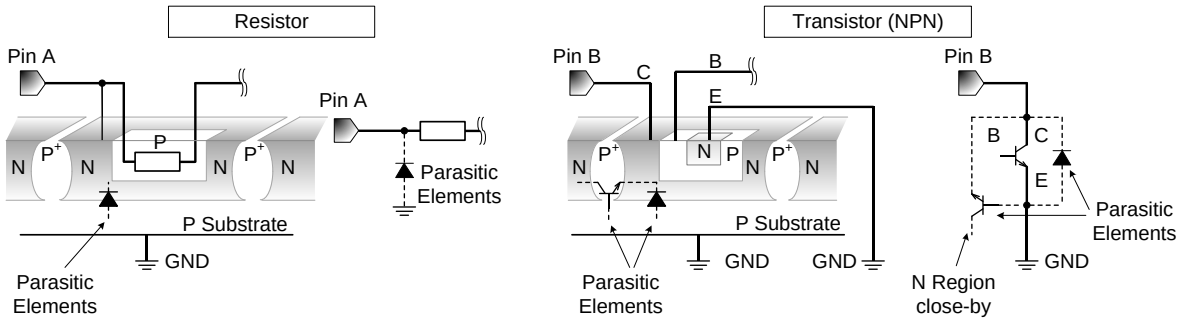


Figure 24. Example of monolithic IC structure

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

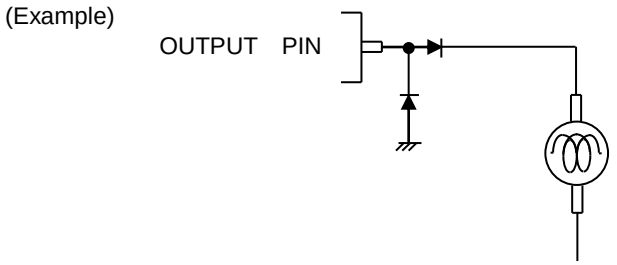
14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

	TSD ON Temperature [°C] (typ)
BD3522EFV	175

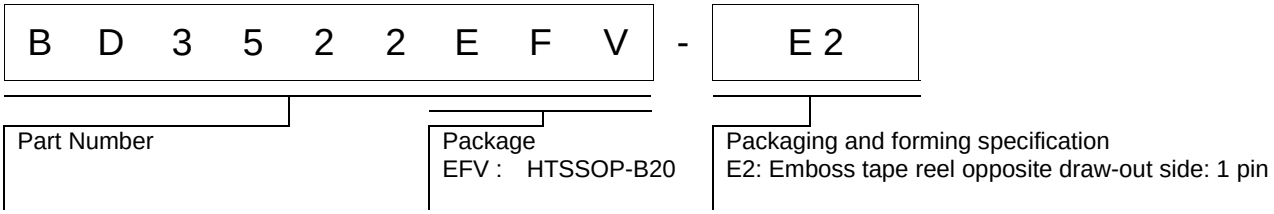
15. Output Pin

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

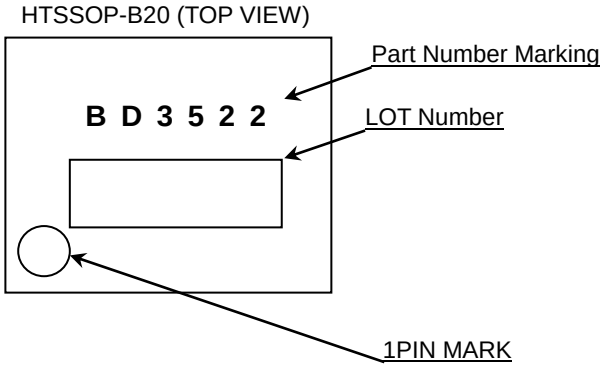


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Ordering Information



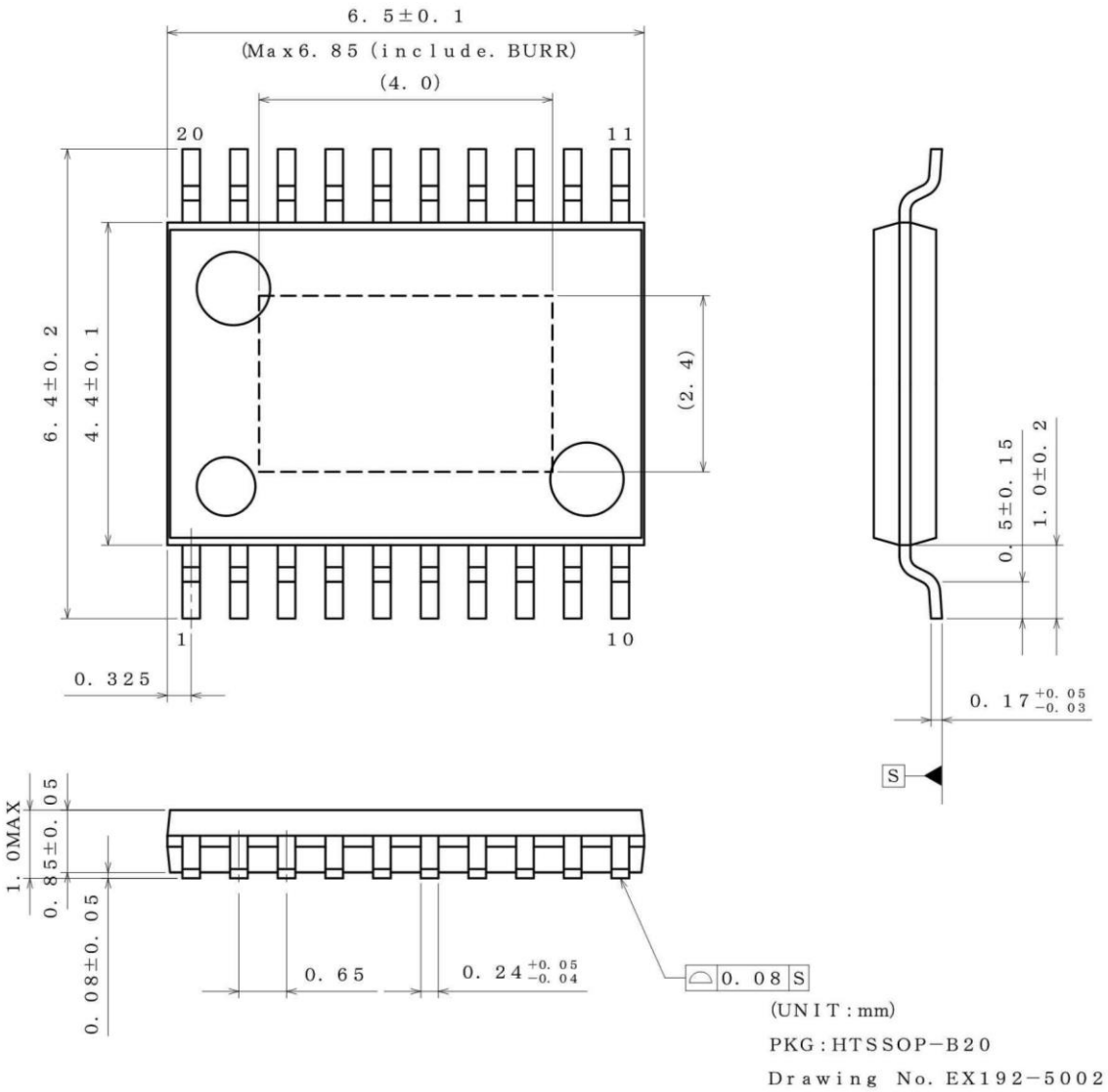
Marking Diagram



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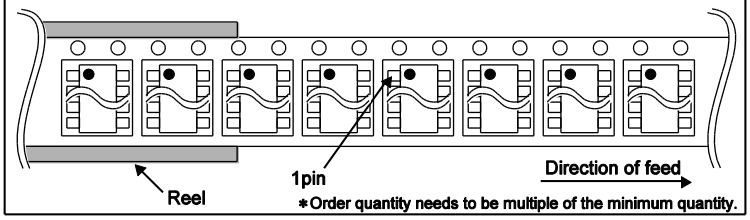
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Revision History

Date	Revision	Changes
02.Nov.2015	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BD3522EFV - Web Page

Buy

Distribution Inventory

Part Number	BD3522EFV
Package	HTSSOP-B20
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes